ELSEVIER

Materials Chemistry and Physics 51 (1997) 195–198

MATERIALS CHEMISTRY AND PHYSICS

Materials Science Communication

Effects of RCA clean-up procedures on the formation of roughened poly-Si electrodes for high-density DRAMs' capacitors

Han-Wen Liu [a,*], Wen-Koi Lai [a], Swei-Yang Yu [b], Stewart C. Huang [b], Huang-Chung Cheng [a]

[a] *Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, ROC*

[b] *Mosel Vitelic Incorporation, Science-Based Industrial Park, Hsinchu 300, Taiwan, ROC*

Received 20 December 1996; revised 19 May 1997; accepted 19 May 1997

Abstract

A novel structure, the phosphorus-implanted poly-Si films treated with phosphoric acid (H_3PO_4) and cleaned by standard RCA cleanup procedures, has been demonstrated as the bottom electrodes of DRAMs' stacked capacitors. After the H_3PO_4 treatment and RCA cleaning process, micro-island structures are formed on the poly-Si surface of the storage electrodes. The $NH_4OH + H_2O_2 + H_2O$ (SC-1) solution in the RCA cleaning procedures is the main component to change the porous surfaces and engraved structures, formed by H_3PO_4 treatment, into micro-islands. Although the electrical properties are slightly degraded compared to the control samples, but they fulfill the requirements of high-density DRAMs, resulting from the increment of cell capacitance. © 1997 Elsevier Science S.A.

Keywords: RCA clean-up procedures; Poly-Si electrodes; High-density Drams' capacitors

1. Introduction

To promote the density of dynamic-random-access-memories (DRAMs), the cell area in DRAMs' structures must be reduced. Reduction of cell capacitance, resulting from the memory cell miniaturization, is one of the most serious problems. Many advanced structures for the stacked capacitor cells have been investigated to enlarge the surface area of the storage electrodes so as to obtain sufficient cell capacitance [1–7]. Cylindrical storage electrodes, spread-stacked electrodes, disk-shaped electrodes, micro villus patterning (MVP) electrodes, honeycomb-shaped electrodes engraved by the reactive-ion-etching (RIE) and uneven electrodes with hemispherical-grained (HSG) Si were demonstrated to meet this purpose of enlargement of effective surface area of the storage-node. However, it is difficult to carry out these complicated storage-node structures by use of conventional processes. Recently, Watanabe et al. [8] reported a new technique, in which in-situ phosphorus-doped poly-Si could be changed into a porous-Si through hot phosphoric acid (H_3PO_4) treatment. In this article, we observed that after H_3PO_4 etching and RCA cleaning processes, the phosphorus-implanted and activated poly-Si is changed into micro-island structures and the RCA clean-up procedures are the main cause to form these novel structures.

* Corresponding author.

0254-0584/97/$17.00 © 1997 Elsevier Science S.A. All rights reserved
PII S0254-0584(97)01989-5

2. Experimental procedures

Capacitors with doped poly-Si bottom electrodes were fabricated on Si substrate covered with 3000 Å-thick SiO_2 which was grown at 1050°C in a steam ambient. Double poly-Si layers were used in this work to avoid the poly-Si lines broken when they were immersed into hot phosphoric acid (H_3PO_4). A 1000 Å-thick LPCVD poly-Si was deposited at 620°C and then phosphorus-implanted with 30 KeV, 4×10^{15} cm^{-2}. After being annealed at 850°C for 30 min, the native oxide was removed by diluted HF solutions and a 2000 Å-thick poly-Si was deposited again. These wafers were phosphorus-implanted with 30 KeV, 6×10^{15} cm^{-2} and annealed at 850°C for 30 min. After the native oxide was removed, some wafers were etched by 85% phosphoric acid (H_3PO_4) at 120°C for 150 min. Some of these wafers etched by H_3PO_4 were cleaned by standard RCA procedures and some were only cleaned by $H_2SO_4 + H_2O_2$ (SPM), $NH_4OH + H_2O_2 + H_2O$ (SC-1), $HCl + H_2O_2 + H_2O$ (SC-2) respectively. The morphology of bottom electrodes were inspected by SEM. The capacitors being used to extracting electrical properties were formed by the following processes. Prior to the dielectric films formation, all of these wafers which were etched and unetched by H_3PO_4 were cleaned by standard RCA clean-up procedures. A 60 Å-thick nitride films were deposited at 750°C by LPCVD using the SiH_2Cl_2/NH_3 mixture and then all of these samples were oxidized at 850°C for 30 min in O_2

ambient. A 2700 Å-thick poly-Si was deposited as the top electrodes and then $POCl_3$-doped at 850°C for 40 min and the sheet resistance which were measured by the four point probe was 40 ~ 50 Ωsq. Three-mask procedures were used to form the interpoly-Si capacitors and the cross-sectional structure was shown in Fig. 1. The electrical properties were measured by HP4156 and Keithly CV systems.

3. Results and discussion

Figs. 2 and 3 show the plain-view SEM micrographs of the phosphorus-implanted poly-Si electrodes without and with H_3PO_4 treatments, respectively. It was observed that after H_3PO_4 treatment, porous surfaces and engraved structures are formed on poly-Si grain surface and grain boundaries, respectively. But these structures cannot effectively increase the surface areas of the storage-nodes. The SEM micrograph of the samples etched by H_3PO_4 and cleaned by RCA clean-up procedures is shown in Fig. 4. It was found that micro-islands were formed on the poly-Si surface of the electrodes and there is a very big difference between Figs. 3 and 4. These micro-island structures can efficiently enlarge the surface areas of the storage electrodes. In order to distinguish which solutions in RCA clean-up procedures are the main causes, the H_3PO_4-etched samples are cleaned by $H_2SO_4+H_2O_2$ (SPM), $NH_4OH+H_2O_2+H_2O$ (SC-1), and $HCl+H_2O_2+H_2O$ (SC-2) respectively, and the SEM images are shown in Figs. 5–7, accordingly. It can be seen that the images in Figs. 4 and 6 are almost the same shape, micro-islands on the surface of the electrodes. The coral-shaped poly-Si on the surface of the electrodes, which were only cleaned by $H_2SO_4+H_2O_2$ or SC-2 respectively, are shown in Figs. 5 and 7. Because, in $H_2SO_4+H_2O_2$ and SC-2 solutions, oxidation of poly-Si occurs on the surface owing to the component of H_2O_2 which has strong oxidizing capability. In SC-1 solution, not only oxidizing capability but also etching capability will attack to the H_3PO_4-etched surface of the poly-Si electrodes owing to the component of NH_4OH which will etch the silicon. The SC-1 is the dominant solution which change the porous-Si into micro-islands and increase the capacitance, resulting from the surface area enhancement of the storage-nodes. From *C–V* measurements, the capacitors with roughened and flat poly-Si possess the capacitance 18.17 fF μm^{-2} and 5.77 fF μm^{-2}, respectively. The roughened poly-Si electrode can achieve the surface enlargement of 3.15 times. The electrical properties of the capacitors with these micro-islands as the bottom electrodes are shown in Figs. 8 and 9. The area of the testing capacitors is 3.14×10^{-4} cm^{-2}. The leakage current density, which is defined as the leakage current divided by mask area, at +1.65 V and −1.65 V are 7.2×10^{-8} A cm^{-2} and -3.3×10^{-8} A cm^{-2}, correspond-

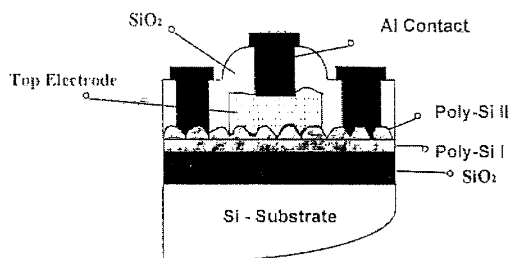

Fig. 1. Cross-sectional device structure for interpoly capacitor with roughened poly-Si as the bottom electrodes.

Fig. 3. SEM image of the phosphorous-implanted poly-Si electrode with H_3PO_4 treatment.

Fig. 2. SEM image of the phosphorous-implanted poly-Si electrode without H_3PO_4 treatment.

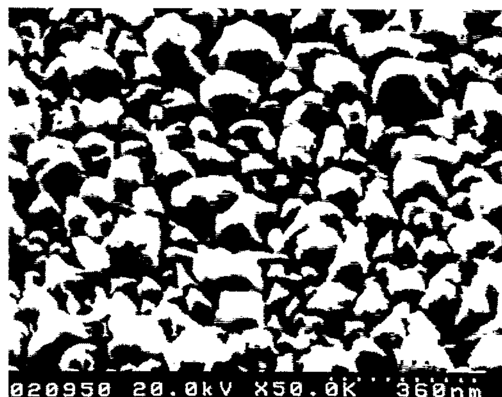

Fig. 4. SEM image of the phosphorous-implanted poly-Si electrode etched by H_3PO_4 and cleaned by RCA cleanup procedures.

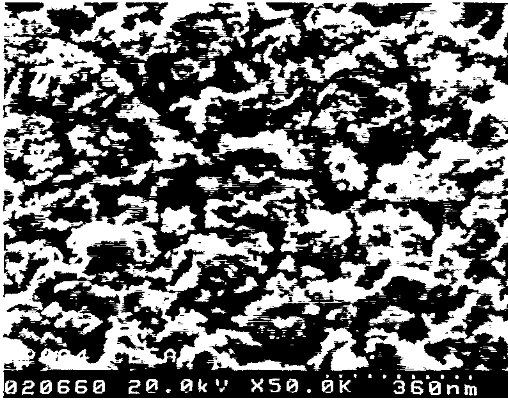

Fig. 5. SEM image of the phosphorous-implanted poly-Si electrode etched by H_3PO_4 and cleaned by H_2SO_4:H_2O_2 (SPM).

Fig. 6. SEM image of the phosphorous-implanted poly-Si electrode etched by H_3PO_4 and cleaned by NH_4OH:H_2O_2:H_2O (SC-1).

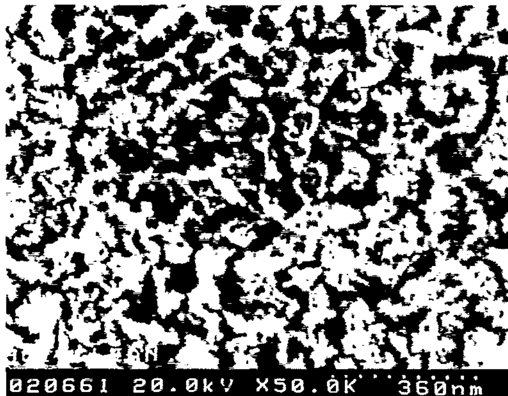

Fig. 7. SEM image of the phosphorous-implanted poly-Si electrode etched by H_3PO_4 and cleaned by HCl:H_2O_2:H_2O (SC-2).

ingly. The electrical properties are some degradation, as compared to the control samples, which result from the enlargement of surface area and the effect of field enhanced by the tips of micro-islands structures. However, they fulfill the requirements of future high-density DRAMs, owing to the large increase of cell capacitance. Weibull plots of TZDB characteristics under ramping voltage test also show some degradation, as compared to the control samples, but they exhibit high enough breakdown voltage which is larger than the operating voltage of future high-density DRAMs.

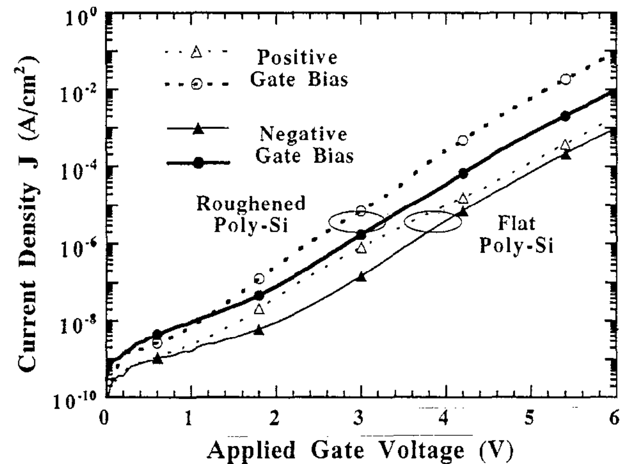

Fig. 8. *J–V* characteristics of the capacitors with the roughened and flat poly-Si as the bottom electrodes.

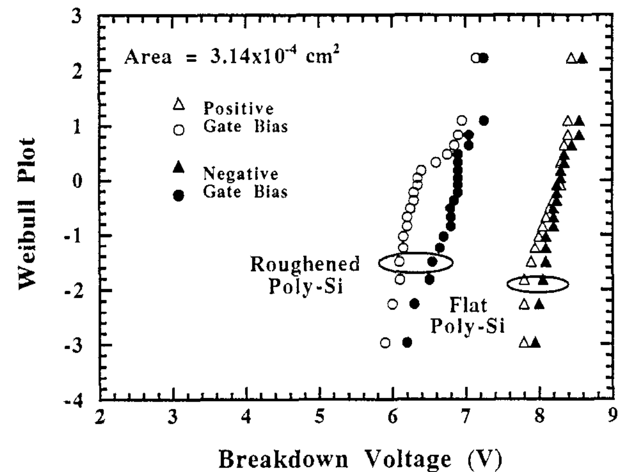

Fig. 9. TZDB characteristics of the capacitors with the roughened and flat poly-Si as the bottom electrodes.

4. Conclusions

In conclusion, the phosphorus-implanted poly-Si films etched by 85% phosphoric acid (H_3PO_4) and then cleaned with standard RCA clean-up procedures can simply and easily increase the surface areas of DRAMs' capacitors, i.e. increase the capacitance. The electrical properties, including leakage current density and TZDB characteristics, show some degradation, resulting from the enlargement of surface area and the effect of field enhanced by the tips of micro-islands structures. But owing to the much increment of cell capacitance, these capacitors could be used in future high-density DRAMs and those electrical properties could fulfill the requirements. The SC-1 is the dominant solution which changes the porous-Si into micro-islands. Therefore, this technique is promising for the future high-density DRAMs' applications.

Acknowledgements

This work was supported in part by the Republic Of China National Science Council (ROC, NSC) under Contract NSC-

85-2215-E-009-035. The authors thank the National Nano Device Laboratory (NDL) of R.O.C. NSC and the Semiconductor Research Center (SRC) of National Chiao Tung University for technical support.

References

[1] J.H. Ahn, Y.W. Park, J.H. Shin, S.T. Kim, S.P. Shim, S.W. Nam, W.M. Park, H.B. Shin, C.S. Choi, K.T. Kim, D. Chin, O.H. Kwon and C.G. Hwang, Micro Villus Patterning (MVP) Technology for 256 Mb DRAM Stack Cell, Symp. on VLSI Tech. Dig. of Technical Papers, 1992, pp. 12–13.

[2] S. Yu, K. Chun and J.D. Lee, The honeycomb-shape capacitor structure for ULSI DRAM, IEEE Electron Dev. Lett., 8 (1993) 369–371.

[3] H. Watanabe, N. Aoto, S. Adachi and T. Kikkawa, Device application and structure observation for hemispherical-grained Si, J. Appl. Phys., 71 (1992) 3538–3543.

[4] M. Yoshimaru, J. Miyano, N. Inoue, A. Sakamoto, S. You, H. Tamura and M. Ino, Rougged surface poly-Si electrode and low temperature deposited Si_3N_4 for 64 Mbit and beyond STC DRAM cell, IEDM Tech. Dig., (1990) 659–662.

[5] Y. Hayahide, H. Miyatake, J. Mitsuhashi, M. Hirayama, T. Higaki and H. Abe, Fabrication of storage capacitance-enhanced capacitors with a rough electrode, Jpn. Appl. Phys. Lett., 29 (1990) L2345–L2348.

[6] H. Itoh, Y. Miyatake, M. Takahashi, Y. Kimira, A. Endoh, Y. Nagatomo, M. Yoshimaru, F. Ichikawa and M. Ion, Two step deposited rugged surface (TDRS) storagenode and self aligned bitline-contact penetrating cellplate (SABPEC), Symp. on VLSI Tech. Dig. of Technical Papers, 1991, pp. 9–10.

[7] P.C. Fazan, V.K. Mathews, H.C. Chan and A. Ditali, Ultrathin oxide/nitride dielectrics for rugged stacked DRAM capacitors, IEEE Electron Dev. Lett., 2 (1992) 86–88.

[8] H. Watanabe, I. Honma, S. Ohnishi and H. Kitajima, A novel stacked capacitor with porous-Si electrodes for high density DRAMs, Symp. on VLSI Tech. Dig. of Technical Papers, 1993, pp. 17–18.