A Novel Driving Scheme for FLCD

Jiin-chuan Wu and Chi-Chang Wang

Department of Electronics Engineering
National Chiao Tung University
Hsinchu, Taiwan, R.O.C.

ABSTRACT

A frame change data driving scheme(FCDDS) for ferroelectric LCD(FLCD) of matrix-addressing is developed which uses only positive voltages for the row and column waveforms to achieve bipolar driving waveforms on the FLCD pixels. Thus the required supply voltage for the driver chips is half that of the conventional driving scheme. Each scan line is addressed in only twice the switching time τ (minimum response time of FLC) so that this scheme is suitable for high duty ratio panels. In order to meet this bistable electro-optic effects of FLCD and zero net DC voltage across each pixel of the liquid crystal, turning on and turning off pixels are done at different time slot and frame slot. This driving scheme can be easily implemented using commercially available STN LCD drivers plus a small external circuit or by making an ASIC which is a slight modification of the STN driver. Both methods are discussed.

Keyword: FLCD, matrix-addressing, bistable, frame change data driving scheme

1. INTRODUCTION

Liquid crystal display(LCD) is becoming more and more widely used in the display field[1]. The extremely low power consumption, low voltage operation, readability in glaring sunlight, compactness and flexible size are just some of the distinctive features which make LCDs preferable over other types of displays. LCDs consume the least amount of power among all displays and thus are the natural choice for portable and battery operated equipment. Another important factor contributing to this rapid growth is the capability of LCDs to interface directly with the integrated circuits which have revolutionized the electronics industry and substantially cut the cost and size of consumer and professional equipment. LCDs are truly flat panel and do not emit any harmful radiation which are their additional advantage over CRTs.

The matrix addressing method is suitable and popular for large pixels flat panel displays which permit the combination of simplicity of construction with high complexity, high resolution and large aperture ratio. However the supertwisted nematic(STN) panels are limited in its ultimate complexity[2] by the need for the applied waveforms to maintain an on level of RMS bias on selected pixels and an off level of RMS bias on unselected pixels. As the number of lines increases, this discrimination becomes poorer and hence STN panels are limited to about 480 lines, beyond which angle of view becomes very poor due to low contrast ratio.

The electro-optic effect in thin layers of ferroelectric smectic C materials[3] is fast, bistable, and response time-voltage characteristic, thus providing a route to high information content displays which overcomes the limitations of root mean square(RMS) matrix addressing displays. The development of high resolution FLCD not only depends on the optimization of such important cell parameters like the liquid crystal material and alignment layer but also on efficient matrix addressing method. Several papers[4-7] on FLC matrix addressing method have been published so far. In this paper, a novel driving scheme for FLCD of matrix-addressing is developed. This driving scheme uses the conventional response time-voltage characteristic(τ-V constant) and only positive voltages for the row and column waveforms to achieve bipolar driving waveforms on the FLCD pixels. Thus the required supply voltage for the driver chips is half that of the conventional driving scheme. Each scan line is addressed in only twice the switching time τ (minimum response time of FLC) so that this scheme is suitable for high duty ratio panels.

In order to meet this bistable electro-optic effects of FLCD, reversal of electric field with enough amplitude is required to switch the FLC between the two stable states. Furthermore, the net DC voltage across each pixel should be zero to prevent electrochemical breakdown of the liquid crystal. To meet these requirements, turning on and turning off pixels are done at different time slot and frame slot. This driving scheme is called as frame change data driving

0-8194-2025-5/96/$6.00

scheme(FCDDS) and can be easily implemented using commercially available STN LCD drivers plus a small external circuit or by making an ASIC which is a slight modification of the STN driver. Both methods are discussed.

2. PROPERTIES OF FLC DEVICES

Designing FLC matrix addressing schemes has to be related to the basic properties of FLC devices:

1. Bistable characteristic: Unlike TN and STN LCD's, which response to the RMS value of the applied field, FLCD responses to the absolute value and polarity of the applied field. The ferroelectric switching torque is linear in the electric field. Switching of the two basic states with the spontaneous polarization up and down is controlled by the polarity of the applied voltage which is shown in Fig.1[3]. The down state represents the optical on state which shall be obtained by application of a positive voltage. Similarly, the polarization up state to the optical off state at a negative voltage. This is the fundamental reason for the improved viewing angle in the FLC.

2. Response time-voltage(τ-V) characteristic: There is a switching threshold on application of a voltage pulse with increasing area τV, where τ is the length of the pulse and V is the amplitude of the pulse. Driving schemes fall into two categories, those designed to work with materials having a conventional response time-voltage characteristic(τ-V constant) and those showing a minimum in their switching characteristic(τ-V minimum). These characteristics are illustrated in Fig.2[5]. The 'τ-V min' mode of operation has been shown to give fast switching speeds, high contrast and a wide operating range. The operation voltage of 'τ-V constant' mode is lower than that of 'τ-V min' mode.

3. Zero DC bias characteristic: The matrix addressing schemes are designed to ensure that there is no net zero DC voltage across each pixel to prevent electrochemical breakdown of the liquid crystal. The FLC device offers bistability characteristic, hence the minimum of the line address period and switching portion need two time slots wide for each scan which also obtain net zero DC bias across each pixel.

4. Relaxed states and crosstalk characteristic: The main causes of the contrast of FLCD reduction are the lack of full bistability and crosstalk. Figure 3(a)[3] illustrates a typical optical response to a switching pulse of amplitude V_s and duration τ After reaching the desired maximum or minimum for the duration of the switching pulse, the transmission then relaxes to intermediate levels. The corresponding reduction in contrast may be diminished through the application of an AC electric field which couples to the dielectric tensor but is of too high a frequency to couple to P_s. In a real device, however, the AC signal is usually provided by the data waveform. This leads to the conflicting requirements of a high V_d to AC stabilize the high contrast of the fully switched states but which is sufficiently low to prevent crosstalk, Fig.3(b)[3]; this is particularly difficult for fast materials.

3. THE FRAME CHANGE DATA DRIVING SCHEME

Figure 4 is the fame change data driving scheme. To meet bistable and net zero DC bias requirements, turning off and turning on pixels are done at different time slot and frame slot which are shown in Fig.4(e) and (f). In this driving scheme frame reversal is used, all the pixels with data=1 will be turned on in one frame scanning time(called '1' frame) and all the pixels with data=0 will be turned off in the next frame scanning time(called '0' frame). In every frame, the rows of the panel are selected one by one, so that data are updated row by row. Assume 1/3 bias is used, then let V_0=0, V_1=Vcc/3, V_2=2*Vcc/3, and V_3=Vcc, where Vcc is the supply positive voltage.

First, let's consider the '0' frame. On the selected row which is shown in Fig.4(a), a voltage of V_1 is applied for a duration of τ(switching time), then V_3 is applied for another τ, the line scanning time is thus 2τ. For the other non-selected rows which is shown in Fig.4(b), V_1 is applied for 2τ. On the columns, if the display data is 0 which is shown in Fig.4(c), V_2 is applied followed by V_0; if the data is 1 which is shown in Fig.4(d), V_0 is applied followed by V_2. The voltage applied on each pixel is the difference between the row and column voltages. Thus, on the selected rows, the '0' pixels will see a voltage of $-V_1$ followed by V_3, the '1' pixels will see a V_1 voltage for 2τ time. So, the '0' pixel will be turned off by the V_3 voltage and the '1' pixels will remain in their previous states because a V_1 voltage does not change their states. However, the DC voltage of the applied voltage is not zero at this point. On the nonselected rows, independent of the data value, all the pixels will see a voltage of V_1 and -V which is shown in Fig.4(g) and (h), thus their states do not change and the DC value of the applied voltage is zero.

During the '1' frame, the row voltage is simply Vcc-(row voltage in '0' frame), i.e., for the selected row, the voltage is V_2 followed by V_0, and for the non-selected rows is V_2. The column voltage is also Vcc-(column voltage in '0' frame), i.e., for data=0, the voltage is V_3 and V_1; for data=1, the voltage is V_1 and V_3. Thus, on the selected rows, the '1' pixels will see a voltage of V1 followed by $-V_3$, the '0' pixels will see a -V1 voltage for 2τ time. So, the '1' pixels will see a voltage of V_1 followed by $-V_3$, the '0' pixels will see a $-V_1$ voltage for 2τ time. So, the '1' pixel will be turned on by the $-V_3$ voltage and the '0' pixels will remain in their previous states because a $-V_1$ voltage does not change their states. When we combine the applied voltages of the '0' and '1' frame, the net DC voltage on the selected row is now zero. On the non-selected rows, all the pixels still see a voltage of V_1 and $-V_1$, thus their states do not change and the net DC value of the applied voltage is zero.

From above discussion, a bipolar voltage of Vcc and -Vcc can be applied to the pixel from a single Vcc supply in FCDDS which is half that of conventional driving scheme. Note that only four different voltages appear on the row and column, this is very similar to the STN LCD driving scheme except some minor difference in voltage selection logic. Each scan line is addressed in only twice the switch time τ which is minimum response time of FLC, so this driving scheme is suitable for high duty ratio panels. The FCDDS operates in the τ-V constant mode, however the operating voltage is lower than that of the τ-V min mode. Furthermore, the swtiching voltage(V_s) is Vcc and the non-switching voltage(V_d) is Vcc/3 which obtained better discrimination and lower crosstalk and relaxed than that of conventional driving scheme operating in the τ-V constant mode.

4. IMPLEMENT THE FCDDS

The frame change data driving scheme can be implemented by the STN LCD drivers and ASIC which is illustrated as following.

4.1. Implemented by STN drivers

The row and column waveforms of FCDDS only need four different voltages, so this scheme can be easily implemented using commercially available STN LCD drivers plus a small external circuit. Figure 5 is a block diagram of the FCDDS for a 640*400 dots panel of FLC. The HD66106F LCD driver[8], the commercial product of HITACHI, has a high duty ratio and 80 outputs for driving a large capacity dot matrix LCD panel. This chip can be used as column and row drivers, so only 13 drivers are enough to drive an LCD panel of 640*400 dots. It also easily interfaces with various LCD controllers because of its internal automatic chip enable signal generator. The maximum of power supply for LCD driving circuits is 37 voltage. By Fig.3, the switching time(τ) is about 20μs and the maximum number of scan line is 400 for 60Hz frame frequency.

In Fig.5, the HD64645F LCTC[8] which is 80 family CPU interface is a control LSI for large size dot matrix liquid crystal displays. The LCTC is software compatible with the HD6845 CRTC[7], since its programming method of internal registers and memory addresses is based on the CRTC. A display system can be easily converted from a CRT to a LCD. Finally, an external voltage generator is designed in Fig.6, where R is resistance, F is '0' frame high state, and $\overline{F}$ is '1' frame high state. This circuit can generate four different voltages(0, Vcc/3, 2*Vcc/3, and Vcc) and 7 outputs which are applied to row and column drivers. The voltage of VH always is Vcc and is connected to V_{LCD} pin of row and column drivers which supplies power to the LCD drive circuit. The outputs O_1 and O_6 are connected to V_1 and V_2 pins of row and column drivers, the outputs O_2 and O_4 are connected to V_3 and V_4 pins of column drivers, and the outputs O_3 and O_5 are connected to V_3 and V_4 pins of row drivers.

4.2. Implemented by ASIC

When the operating voltage of FLC is higher than that of commercially available STN LCD drivers, the FCDDS is implemented by making ASIC. To reduce the complexity of Fig.6, the 7 outputs circuit is deleted and the circuit of HD66106F LCD driver is slightly modificated. Let '0' frame slot is low, '1' frame slot is high, first switching time slot is low, and second switching time slot is high, then the state tables of row and column are obtained by Fig.4 and are shown in Table 1(a) and (b) where F is frame slot, S is switching time slot(display operating frequency), R is scan line signal, C is display data. Now, Boolean equation is defined as

$$M = F \cdot \overline{CH1} + (F \cdot S + \bar{F} \cdot \bar{S}) \cdot CH1, \text{ and} \quad (1)$$

$$D = F \cdot R \cdot \overline{CH1} + (\bar{F} \cdot \bar{S} \cdot C + \bar{F} \cdot S \cdot \bar{C} + F \cdot \bar{S} \cdot \bar{C} + F \cdot S \cdot C) \cdot CH1,$$

where CH1 is the selection driver function of HD66106F. The chip is used as a column driver when CH1=1, and row driver when CH1=0. By Eq.(1), Table 1(a) and (b) can be reformed as Table 2(a) and (b) which are same as row and column state tables of STN LCD driver. Some control logic circuit of HD66106F is modified which is shown in Fig.7.

5. CONCLUSION

The frame change data driving scheme for FLCD has been described which uses conventional response time-voltage characteristic(τ-V constant) operation. Since only four different voltages appear on the row and column, this is very similar to the STN LCD driving scheme except some minor difference in voltage selection logic. This driving scheme is based only on positive voltages for the row and column waveforms to achieve bipolar driving waveforms on the FLCD pixels. Thus the required supply voltage for the driver chips is half that of the conventional driving scheme. Each scan line is addressed in only twice the switch time τ (minimum response time of FLC), so that this scheme is suitable for high duty ratio panels. A 640*400 dots panel of FLC is implemented using commercially available STN LCD drivers plus a voltage generator and by making an ASIC which is a slight modification of the STN driver.

ACKNOWLEGMENT

This work was supported by Material Research Laboratory of Industrial Technology Research Institute, Republic of China.

REFERENCES

1. B. Bahadur, *Liquid Crystal Displays*, Science Publishers, Inc., 1984.

2. J. Nehring and A. R. Kmetz, "Ultimate limits for matrix addressing of RMS-responding liquid-crystal displays", IEEE Trans. Electron Devices, Vol. 26, No.5, pp.795-802, 1979.

3. J. C. Jones, M. J. Towler, and J. R Hughes, "Fast, High-Contrast Ferroelectric Liquid Crystal Displays and the Role of Dielectric Biaxiality", ", Displays, Vol.14, No. 2, pp.86-93, 1993.

4. P. W. H. Surguy, et al., "The JOERS/Alvey Ferroelectric Multiplexing Scheme", Ferroelectrics, 122, pp.63-79, 1991.

5. J. R Hughes and E. P. Raynes, "A New Set of High Speed Matrix Addressing Schemes for Ferroelectric Liquid Crystal Displays" Liquid Crystals, 13, pp.597-601, 1993.

6. T. Numao and M. Koden, "Driving Waveforms of Partial Writing Scheme for FLCD" ", Displays, Vol.14, No. 3, pp.139-143, 1993.

7. J. R Hughes, et al., "A High-Resolution Ferroelectric Liquid Crystal Display", Displays, Vol.15, No. 2, pp.117-123, 1994.

8. HITACHI, *HITACHI LCD Controller/Driver LSI*, Mar., 1992.

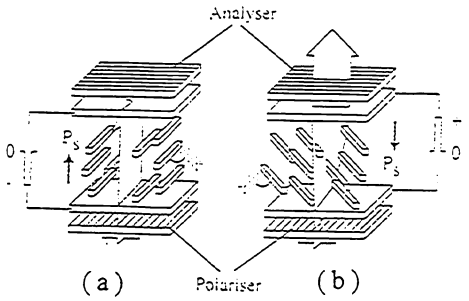

Fig.1 Schematic respresentation of a FLC used as an optical shutter. (After Jones, Towler, and Hughes, Ref. 3)

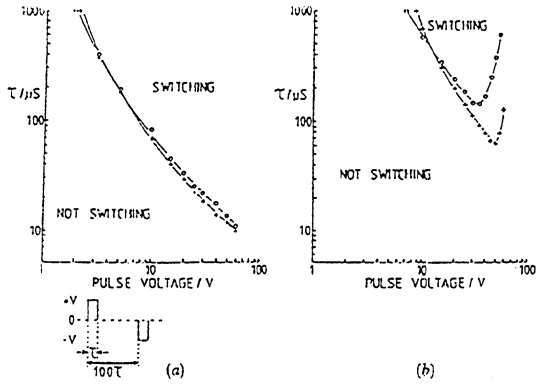

Fig.2 Response time as a function of voltage required to switch the device between states using a simple mono-pulse with a superimposed AC bias(50kHz square wave) to simulate the effect of column voltages encountered during matrix addressing.(a) τ-V constant;material SCE12(E. Merck Ltd.), with 0V r.m.s. AC bias(+), 7.5V r.m.s. AC bias(o). (b) τ-V minimum; material SCE8(E> Merck Ltd.), with 0V r.m.s. AC bias(+), 10V r.m.s. AC bias(o). (After Surguy, et al, Ref. 4)

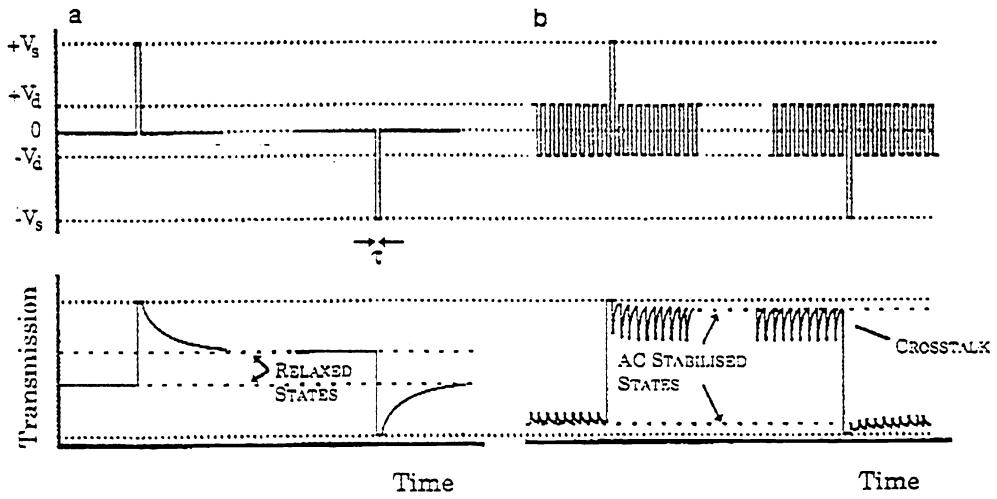

Fig.3 Typical electro-optic response to switching pulses Vs, either (a) without or (b) with an applied data signal Vd represented by a constant frequency(1/τ). (After Jones, Towler, and Hughes, Ref. 3)

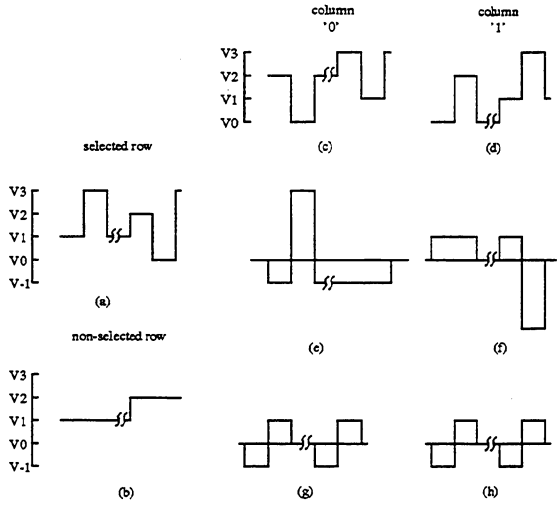

Fig.4 The frame change data driving scheme

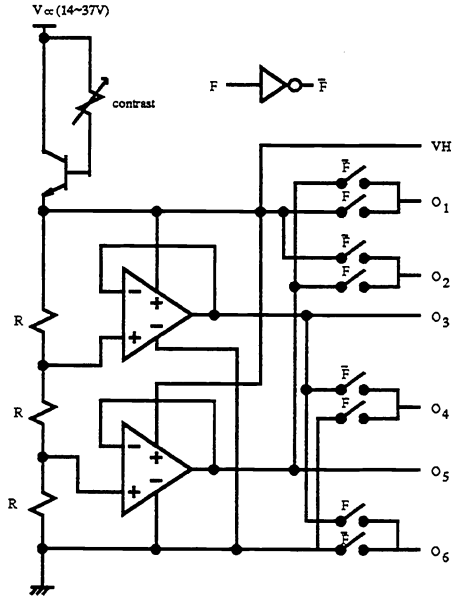

Fig.6 The circuit diagram of voltage generator

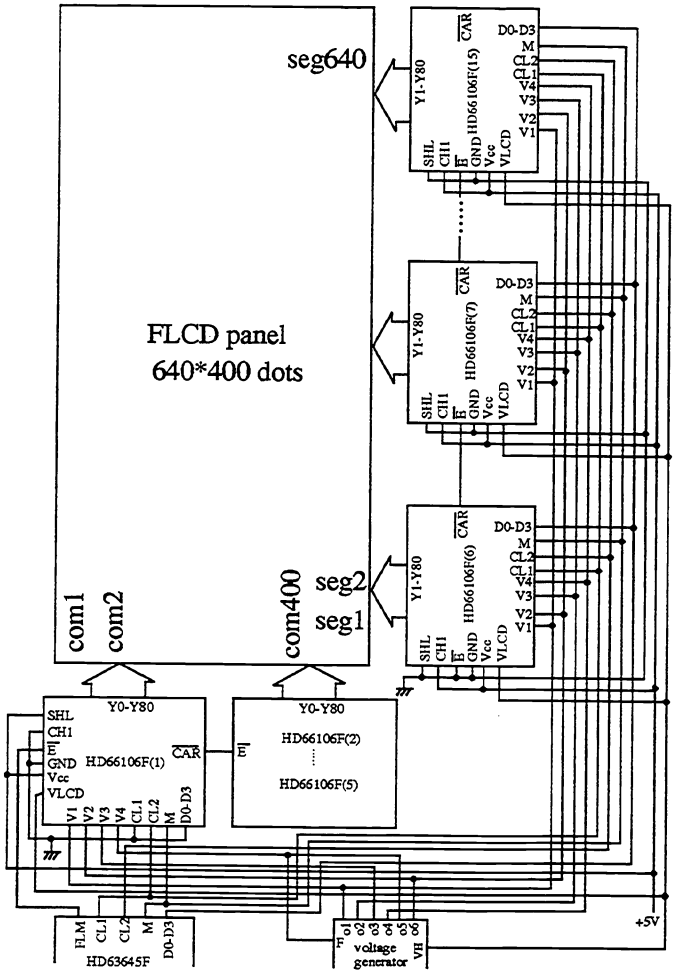

Fig.5 The block diagram of the FCDDS for FLC panel

Table 1(a) Row state table of FCDDS

F	S	R	Vrow
0	0	0	V_1
0	0	1	V_1
0	1	0	V_1
0	1	1	V_3
1	0	0	V_2
1	0	1	V_2
1	1	0	V2
1	1	1	V_0

Table 1(b) Column state table of FCDDS

F	S	C	Vcol
0	0	0	V_2
0	0	1	V_0
0	1	0	V_0
0	1	1	V_2
1	0	0	V_3
1	0	1	V_1
1	1	0	V1
1	1	1	V_3

Table 2(a) New row state table of Table 1(a)

M	D	Vrow
0	0	V_1
0	1	V_3
1	0	V_2
1	1	V_0

Table 2(b) New column state table of Table 1(b)

M	D	Vcol
0	0	V_1
0	1	V_0
1	0	V_2
1	1	V_3

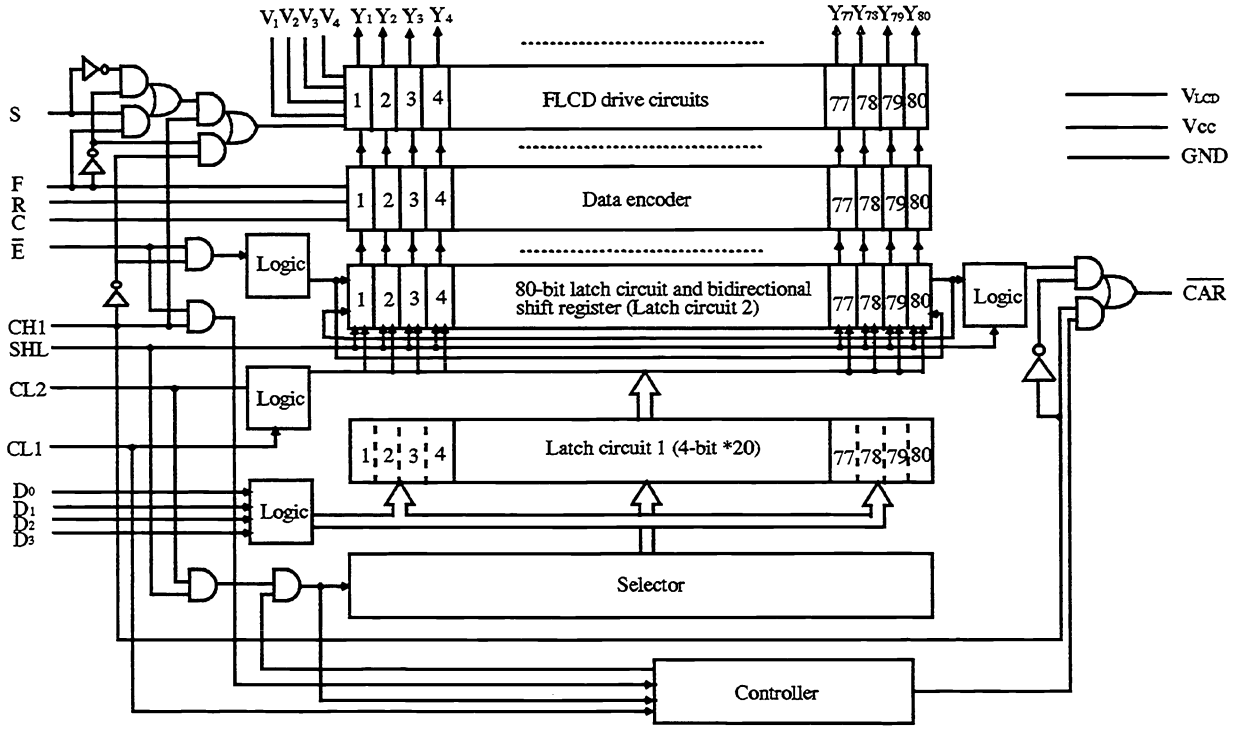

Fig.7 The block diagram of FLCD driver