Improving Safe Operating Area of nLDMOS Array With Embedded Silicon Controlled Rectifier for ESD Protection in a 24-V BCD Process

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***Abstract*—In high-voltage technologies, silicon-controlled rectifier (SCR) is usually embedded in output arrays to provide a robust and self-protected capability against electrostatic discharge (ESD). Although the embedded SCR has been proven as an excellent approach to increasing ESD robustness, mistriggering of the embedded SCR during normal circuit operating conditions can bring other application reliability concerns. In particular, the safe operating area (SOA) of output arrays due to SCR insertion has been seldom evaluated. In this paper, the impact of embedding SCR to the electrical SOA (eSOA) of an n-channel LDMOS (nLDMOS) array has been investigated in a 24-V bipolar CMOS–DMOS process. Experimental results showed that the nLDMOS array suffers substantial degradation on eSOA due to embedded SCR. Design approaches, including a new proposed poly-bending (PB) layout, were proposed and verified in this paper to widen the eSOA of the nLDMOS array with embedded SCR. Both the high ESD robustness and the improved SOA of circuit operation can be achieved by the new proposed PB layout in the nLDMOS array.**

***Index Terms*—Electrostatic discharge (ESD), poly-bending (PB) layout, reliability, safe operating area (SOA), silicon-controlled rectifier (SCR).**

I. Introduction

DUE TO stringent operating environments, reliability has become one of the critical factors to high-voltage (HV) integrated-circuit products. Among the various reliability specifications, on-chip electrostatic discharge (ESD) protection has been known as one of the important but challenging issues in HV ICs [1]. For output drivers designed to drive a considerable amount of current (output arrays), ESD design rules were usually not applied to minimize their layout area in the silicon chip. These output arrays, therefore, were not capable of being self-protected against ESD stresses, and some additional ESD design techniques were needed to provide adequate capabilities to survive the general ESD specification of the 2-kV human body model (HBM) ESD test for commercial products [2]. Additional ESD protection circuit in parallel to the output array is one of the possible design solutions, but trigger competition between the ESD protection circuit and the output array can usually lead to an upset result on the ESD protection level [3]. As a result, self-protected output arrays are preferable to HV technologies. The silicon-controlled rectifier (SCR) inserting into HV output arrays has been reported as an area-efficient method to equip HV output arrays with superior ESD robustness [4]–[8].

Although embedding SCR in HV output arrays is very effective in improving ESD robustness, mistriggering of the embedded SCR imposes new reliability concerns during normal circuit operating conditions, particularly in some applications that require both high-current and high-drain-to-source voltages $V_{\rm DS}$ at the same time. In [7] and [8], it was reported that inserting SCR to an HV output array can diminish the current–voltage boundaries where the output array can be safely operated within, i.e., safe operating area (SOA) [9], [10]. It is therefore important to have a deeper investigation on the impact of the embedded SCR structure to the SOA of HV output arrays. In this paper, different layout parameters and device configurations have been studied for optimization on SOA and ESD robustness of n-channel (nLDMOS) arrays in a 24-V bipolar CMOS–DMOS (BCD) process.

II. Test Structures of an HV nLDMOS

Layout top and device cross-sectional views of the nLDMOS in the given process are shown in Fig. 1(a) and (b), respectively. The optional PBI layer in Fig. 1(b) is an additional P-type Boron Implantation provided by foundry. To emulate the high-current driving requirement of output arrays in the practical IC products, devices in this paper were drawn in large arrays with total effective width W of 4800 μm (48 fingers). Width and channel length of a single finger are kept the same in layout for all studied devices, i.e., 100 μm and 0.35 μm, respectively.

To study the impact on the electrical SOA (eSOA) due to the embedded SCR structure, the layout top view of an nLDMOS array with the embedded SCR (SCR-nLDMOS) is shown in

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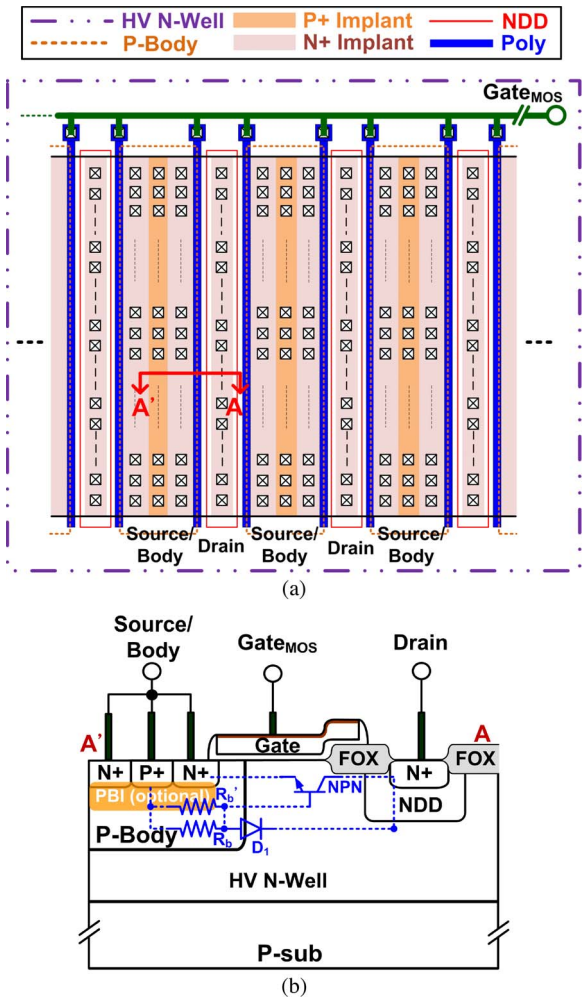

Fig. 1. (a) Layout top view and (b) cross-sectional view along the A-A′ line of the nLDMOS without the embedded SCR.

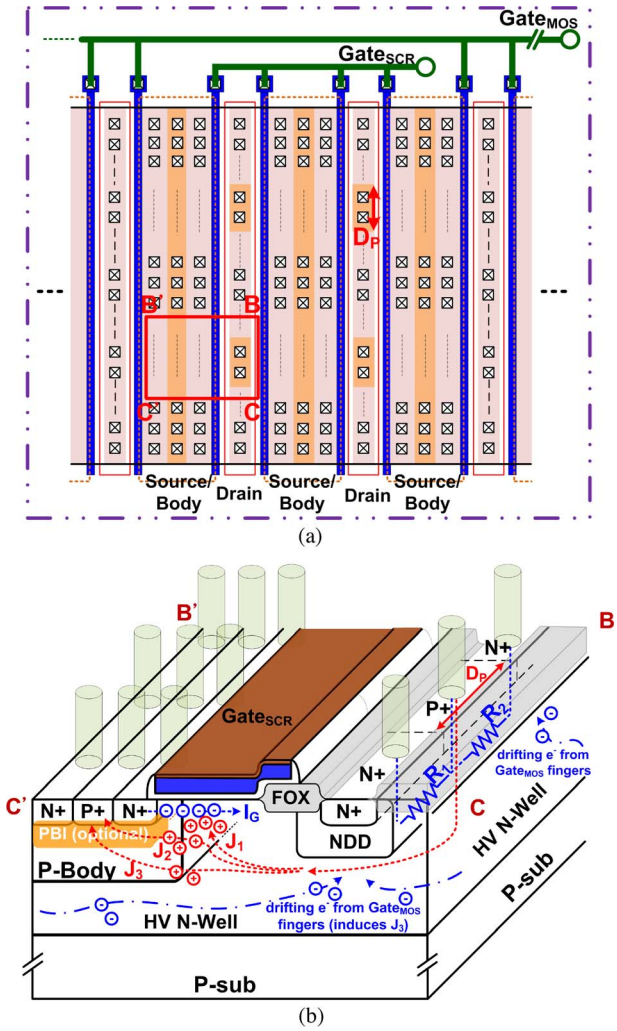

Fig. 2. (a) Layout top view and (b) cross-sectional view along the B-B′ – C-C′ region of the nLDMOS with the embedded SCR.

Fig. 2(a). The embedded SCR was centralized within the central four fingers of nLDMOS arrays by replacing a part of drain implantation from N+ to P+. The four fingers that contain the embedded SCR are referred to as Gate$_{SCR}$ fingers, and the rest of the 44 fingers that do not have the SCR structure are referred to as Gate$_{MOS}$ fingers in this paper. Total effective widths of SCR-nLDMOS arrays were kept the same to those of nLDMOS arrays, i.e., 4800 μm. A device cross-sectional view along the B-B′ – C-C′ square in Fig. 2(a) is shown in Fig. 2(b). P+ implantation at drain regions is the anode of a p-n-p-n SCR structure, and the SCR current path is P+—(NDD/HV n-well)—P-body—N+ source. Gate connection for Gate$_{SCR}$ fingers was intentionally separated from Gate$_{MOS}$ fingers for further investigation, which was either internally short circuited to Gate$_{MOS}$ or internally short circuited to source/body (grounded). The width of a drain P+ implantation is defined as D_P width. All studied SCR-nLDMOS arrays have the same total effective SCR anode width of 200 μm in the four Gate$_{SCR}$ fingers. As a result, SCR-nLDMOS with D_P of 10 μm means that there are 5 P+ segments in each finger, and each P+ segment is 10-μm wide. The five P+ segments are evenly spread along the 100-μm finger width. Three different D_P widths of 50, 10, and 5 μm were studied in this paper.

III. eSOA of nLDMOS and SCR-nLDMOS Arrays

To analyze the impact of the embedded SCR structure to device ruggedness under normal circuit operating conditions, an eSOA with the measurement setup shown in Fig. 3 was used throughout this paper. A device under test (DUT) was biased under a direct-current gate bias, and a transmission line pulsing (TLP) system with a 100-ns pulsewidth was used to deliver pulses to stress the DUT until the DUT snaps back [9], [11]. This test procedure was repeated under different gate biases, and the eSOA is acquired by connecting the last I–V points under different gate biases before snapback. All measurements in this paper were conducted under the room temperature of 300 K.

A. PBI Layer to eSOA of an nLDMOS

In an nLDMOS, there is a parasitic n-p-n BJT inherent in its device structure. As indicated in Fig. 1(b), this parasitic n-p-n BJT consists of the (N+/NDD/HV n-well)—P-body—N+ source. R_b in Fig. 1(b) denotes the parasitic resistor from the P-body without the optional PBI layer, whereas R_b' denotes the parasitic resistor from the PBI layer. The resistance of R_b' is

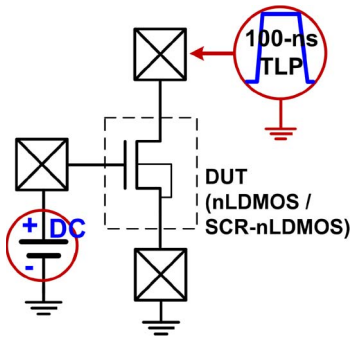

Fig. 3. Measurement setup of eSOA tests with the 100-ns TLP system.

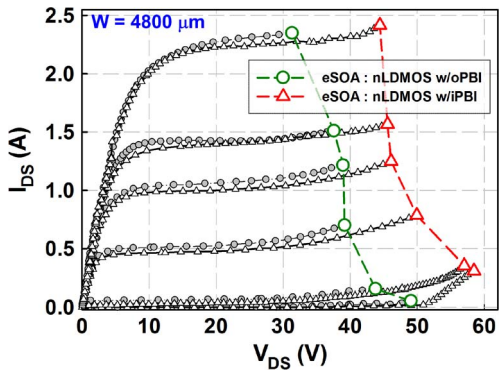

Fig. 4. Measured eSOA of the nLDMOS with and without the PBI layer. DUTs with $I_{\rm DS}$ from low to high were measured under gate biases of 0, 3, 6, 9, 12, and 16 V.

smaller than that of R_b due to the higher doping concentration of the PBI layer. When gate bias is zero and the $V_{\rm DS}$ across the nLDMOS is high enough to initiate avalanche breakdown, a current starts to flow from the D_1 junction diode to the grounded P+ body contact through R_b and R_b'. This builds up a voltage on the P-region underneath the N+ source of the nLDMOS due to R_b and R_b'. Once the built voltage is high enough to forward bias the P-body/N+ source, the parasitic n-p-n BJT is triggered on to initiate a snapback. When the gate voltage is biased above 0 V, channel electrons entering a high electric field region due to a high $V_{\rm DS}$ voltage can undergo the carrier multiplication process, which accelerates the electron–hole pair generation and usually leads to a reduced bipolar trigger voltage. Once the parasitic BJT is triggered on, gate control over the nLDMOS is lost so that the eSOA boundary is defined by the highest $V_{\rm DS}$ ratings under different gate biases without triggering on the parasitic BJT. In other words, SOA defines the region where a DUT can be safely operated without losing control or causing catastrophic destruction [9].

TLP-measured I–V characteristics under different gate biases and the eSOA of nLDMOS arrays with and without the PBI layer are shown in Fig. 4. Because the PBI layer introduces a R_b' resistor in parallel with the P-body resistor R_b, as shown in Fig. 1(b), the base–emitter junction of the parasitic n-p-n BJT becomes harder to be forward biased. The nLDMOS with the PBI layer therefore shows a wider eSOA in Fig. 4 than the nLDMOS without the PBI layer [10]. Under the gate bias of

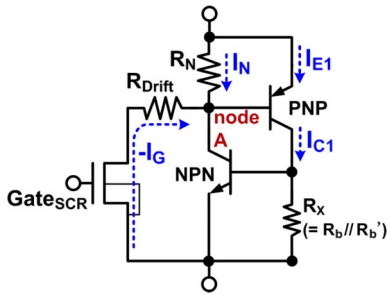

Fig. 5. Equivalent circuit of the embedded SCR in nLDMOS arrays.

0 V (gate grounded), the measured leakage current of both nLDMOS arrays in Fig. 4 immediately increased from picoampere range to over 1 μA after snapback. The measured bipolar trigger currents I_{t1} in Fig. 4 are 311 and 53 mA for the gate-grounded nLDMOS with and without the PBI layer, respectively. Because both nLDMOS arrays failed immediately after snapback, the measured I_{t1} values are equal to their secondary breakdown currents I_{t2}. Both nLDMOS arrays (with and without PBI) possess a virtual zero HBM ESD protection level; therefore, the embedded SCR structure becomes a necessity to provide self-protected ESD protection capability to these two nLDMOS arrays.

B. SCR-nLDMOS and D_P Width to eSOA ($\rm Gate_{SCR}$ Internally Short Circuited to $\rm Gate_{MOS}$)

With the SCR embedded in an nLDMOS array (SCR-nLDMOS), parasitic devices become more complicated than that of the nLDMOS without embedded SCR. The equivalent circuit of the embedded SCR is shown in Fig. 5. The equivalent circuit in Fig. 5 resembles an insulated gate bipolar transistor (IGBT) [12], except for the R_N connecting emitter and base of p-n-p BJT. The R_N resistor comes from the N+ regions next to D_P, i.e., R_1 and R_2 in parallel, as shown in Fig. 2(b). Therefore, SCR-nLDMOS with a smaller D_P width has a smaller equivalent R_N.

It should be noted that in a HV technology, where an IGBT is a dedicated power device, the regenerative feedback of parasitic SCR in the IGBT is carefully suppressed to avoid latch up under normal circuit operating conditions [13]–[15]. However, for HV technologies with relatively low-voltage ratings (typically $<$ 200 V processes so that the studied process in this paper is included too), an IGBT is usually not a dedicated device, and an SCR is used for an ESD protection purpose. SCR structures in these technologies are made up of parasitic BJTs without being particularly suppressed during process development. As a result, the sum of open-base current gains of parasitic p-n-p $\alpha_{\rm PNP}$ and n-p-n $\alpha_{\rm NPN}$ BJTs in these technologies can be higher than 1 to initiate regenerative feedback even under normal circuit operating conditions [16].

The measured TLP I–V curves of SCR-nLDMOS without and with the PBI layer are shown in Fig. 6(a) and (b), respectively. The gate bias for DUTs in Fig. 6 was 0 V, and leakage currents were measured under the drain bias of 24 V. In Fig. 6(a), both SCR-nLDMOS arrays with D_P of 10 and 50 μm can sustain 100-ns TLP stresses higher than

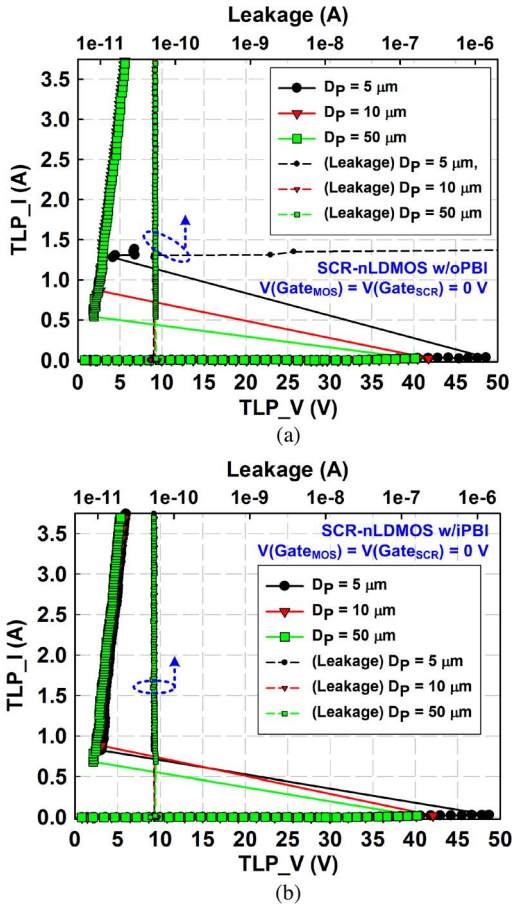

Fig. 6. Measured TLP I–V characteristics of SCR-nLDMOS: (a) without PBI and (b) with PBI. The gate bias for all DUTs was 0 V, and leakage currents were measured under 24-V drain bias.

the limitation of the TLP system used, i.e., 3.75 A. For SCR-nLDMOS with D_P of 5 μm, because a smaller D_P width results in a smaller R_N resistor, the emitter–base junction of p-n-p BJT becomes harder to be forward biased. As a result, D_P of 5 μm in Fig. 6(a) exhibits the highest measured trigger voltage V_{t1} of 48.62 V. Measured V_{t1} for nLDMOS without PBI in Fig. 4 is 49.04 V. These two measured V_{t1} values of 48.62 and 49.04 V show that when D_P is as small as 5 μm, trigger competition can easily happen between the four fingers with the embedded SCR (Gate_{SCR} fingers) and the other 44 fingers without the embedded SCR (Gate_{MOS} fingers). As a result, instead of showing a high TLP-measured I_{t2}, SCR-nLDMOS with D_P of 5 μm failed (leakage current increased over 10 times) at 1.31 A in Fig. 6(a). Because the failure arises from trigger competition between the Gate_{SCR} and Gate_{MOS} fingers, a virtual zero ESD protection level on SCR-nLDMOS without PBI under D_P of 5 μm is possible.

For SCR-nLDMOS with PBI, because the measured V_{t1} for the gate-grounded nLDMOS with PBI in Fig. 4 is increased to 58.47 V, trigger competition between the Gate_{SCR} and Gate_{MOS} fingers is averted. All DUTs in Fig. 6(b) therefore have I_{t2} higher than the equipment limitation of 3.75 A. The effectiveness on the embedded SCR to improve ESD robustness, therefore, has been verified through measurement results in Fig. 6.

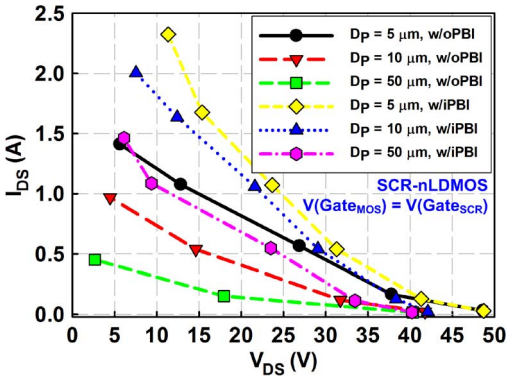

Fig. 7. Measured eSOA of SCR-nLDMOS with Gate_{SCR} short circuited to Gate_{MOS}. The corresponding gate biases for I_{DS} from low to high were 0, 3, 6, 9, 12, and 16 V, respectively. Some measured DUTs have less than 6 data points because these DUTs under high gate biases were directly driven into SCR operation without manifesting distinct snapback to determine their eSOA boundaries.

When the potential of Gate_{SCR} is pulled high to induce a channel current I_G, electrons are provided from the N+ source and holes emitting from the P+ anode of SCR can be recombined with these electrons. This is shown as J_1 current flow in Fig. 2(b). However, instead of being recombined with electrons, part of the emitting holes from P+ anode is drawn to the vicinity of channel due to the negative charge of electrons and then be swept to the grounded P+ body contacts through the P-body/PBI [J_2 current flow in Fig. 2(b)]. These holes traveling through P-body/PBI develop a voltage drop across the base–emitter junction of n-p-n BJT, which will eventually trigger on n-p-n BJT and lead to positive regenerative feedback of SCR during normal circuit operating conditions. This can also be understood from the equivalent circuit shown in Fig. 5 where the I_G current serves as the base current of p-n-p BJT, that can further induce the I_{C1} collector current [17]. Once the base–emitter junction of n-p-n BJT in Fig. 5 is forward biased, SCR is triggered on and latch up happens.

The measured eSOA for SCR-nLDMOS without and with the PBI layer is shown in Fig. 7. DUTs in Fig. 7 have Gate_{SCR} internally connected to Gate_{MOS} so that when a positive gate bias is applied to DUTs in Fig. 7, the Gate_{SCR} potential is pulled high along with the Gate_{MOS} potential. Comparing eSOAs shown in Figs. 4 and 7, a substantially narrowed eSOA due to the embedded SCR is observed. This means that by inserting SCR into the nLDMOS arrays for ESD protection purpose, the SOA boundary is changed from triggering of n-p-n BJT to triggering of SCR due to the strong positive regenerative feedback of the p-n-p-n structure.

Comparing measurement results in Fig. 7 with the same D_P width, SCR-nLDMOS with the PBI layer constantly shows a better eSOA performance than SCR-nLDMOS without the PBI layer. This is due to the fact that the PBI layer not only suppresses bipolar beta gain of n-p-n BJT β_{NPN} but also makes the base–emitter junction of n-p-n BJT harder to be forward biased. The measurement results in Fig. 7 also reveal strong dependence of the eSOA to the D_P width. Under the same gate and anode voltages, a smaller R_N (shorter D_P) helps keep the node A voltage in Fig. 5 at a relatively higher potential. This diminishes the emitting holes from the P+ SCR anode by

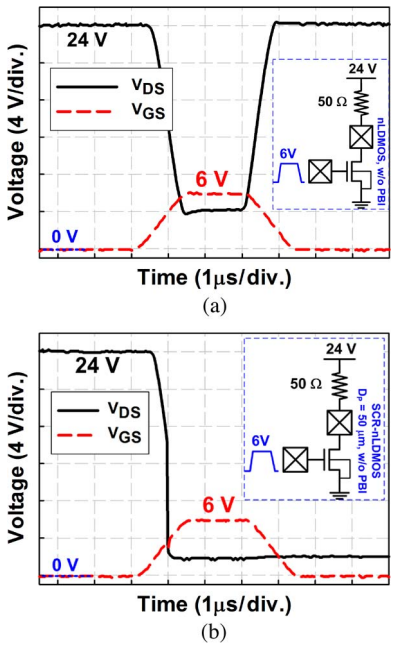

Fig. 8. Measured voltage waveforms when switching a 50-Ω resistive load under a 24-V power supply voltage and a 0-to-6- V voltage pulse on the gate. DUTs are (a) nLDMOS without the embedded SCR and (b) SCR-nLDMOS with D_P of 50 μm. Both measured DUTs do not have the PBI layer. Gate_{SCR} in the measured SCR-nLDMOS is short circuited to Gate_{MOS}.

reducing the voltage difference across the emitter–base junction of p-n-p BJT. With the number of holes emitting from the P+ anode being suppressed, J_2 current in Fig. 2(b) to forward bias the base–emitter junction of n-p-n BJT is reduced as well. Accordingly, SCR-nLDMOS with a shorter D_P width showed a better eSOA performance in Fig. 7. However, combining the information in Figs. 6(a) and 7, although reducing the D_P width when embedding SCR to an nLDMOS array is beneficial to the eSOA, there is a limitation on the smallest applicable D_P width, which comes from the condition of trigger competition between the Gate_{SCR} and Gate_{MOS} fingers.

Importance of the substantially narrowed SOA to the device reliability for circuit operation is shown in Fig. 8(a) and (b). In Fig. 8(a), an nLDMOS (without PBI) was used to drive a 50-Ω resistive load, which is common in analog circuit applications. As the measurement setup shown in the inset in Fig. 8(a), the 50-Ω resistor was biased at 24 V, and a 0-to-6-V V_{GS} pulse was applied to turn on and turn off the DUT. The measured V_{DS} and V_{GS} waveforms in Fig. 8(a) show that the nLDMOS without PBI can safely drive the 50-Ω resistive load. However, when doing the same 50-Ω resistive load test on SCR-nLDMOS with D_P of 50 μm (without PBI), the DUT was burned out after the measurement. As the measurement results shown in Fig. 8(b), the measured V_{DS} drops to the holding voltage of the embedded SCR (~2 V) when the DUT starts to conduct current. The SCR is triggered on during circuit switching so that the latchup-like failure happens, and the DUT can no longer be controlled by the gate bias. Accordingly, although inserting SCR to nLDMOS has been proven to substantially increase ESD robustness, the degraded SOA should be carefully examined to avoid device failure under normal circuit operating conditions.

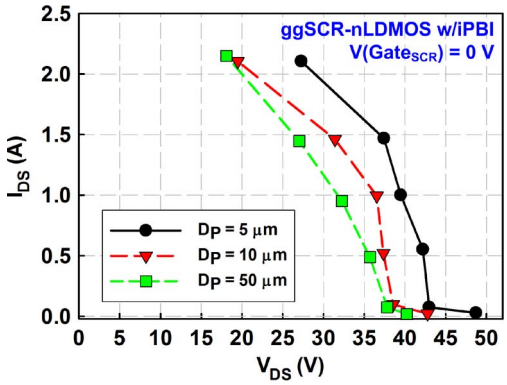

Fig. 9. Measured eSOA of ggSCR-nLDMOS (Gate_{SCR} internally short to source/body). The corresponding gate biases for the I_{DS} from low to high were 0, 3, 6, 9, 12, and 16 V, respectively.

C. Gate_{SCR} Bias to the eSOA of SCR-nLDMOS (ggSCR-nLDMOS)

Because channel current I_G, which induces J_1 and J_2 currents in Fig. 2(b), has been identified as one of the major sources to trigger SCR, metal connection of Gate_{SCR} was changed from being internally short circuited to Gate_{MOS} to the source/body (ggSCR-nLDMOS). This keeps I_G equal to zero during normal circuit operating conditions and thus eliminates J_1 and J_2 in Fig. 2(b). The disadvantage of this ggSCR-nLDMOS configuration is obviously the reduced current driving capability, but since the embedded SCR was centralized within only 4 out of 48 fingers, the reduced current driving capability can be easily compensated by increasing the total number of fingers in the output array. As the measurement results shown in Fig. 9, a substantial improvement on the eSOA was achieved simply by changing the Gate_{SCR} connection. When Gate_{SCR} was connected to Gate_{MOS} (see Fig. 7), the measured maximum V_{DS} ratings under the 12-V gate bias for SCR-nLDMOS with PBI and D_P of 5, 10, and 50 μm are 15.37, 12.41, and 6.11 V, respectively. By changing the Gate_{SCR} connection to the source/body, the measured maximum V_{DS} ratings under the 12-V gate bias for D_P of 5, 10, and 50 μm in Fig. 9 are substantially increased to 37.42, 31.4, and 27.05 V, respectively.

Despite that Gate_{SCR} has been grounded to eliminate the J_1 and J_2 currents, the measured eSOA boundaries in Fig. 9 still show strong dependence to the gate biases. Moreover, a faster rolloff on the measured V_{DS} ratings is observed under high gate biases. For example, the measured V_{DS} ratings in Fig. 9 for D_P of 10 μm decrease only from 38.53 to 36.53 V, when the gate bias was increased from of 3 and 9 V. However, the V_{DS} ratings suffer much severer degradation from 31.4 to 19.47 V, when the gate bias was increased from of 12 and 16 V. This suggests the existence of another factor to induce triggering of embedded SCR, and this factor manifests stronger under high gate biases. In fact, because all fingers of an output array were drawn in a same HV n-well, part of avalanche-generated electrons from the Gate_{MOS} fingers can drift through the shared HV n-well. Since the N+ drain regions in the Gate_{SCR} fingers possess the same potential to the drain of the Gate_{MOS} fingers, these drifting electrons can be collected by the N+ drain in the Gate_{SCR} fingers. These drifting electrons collected by the N+ drain in

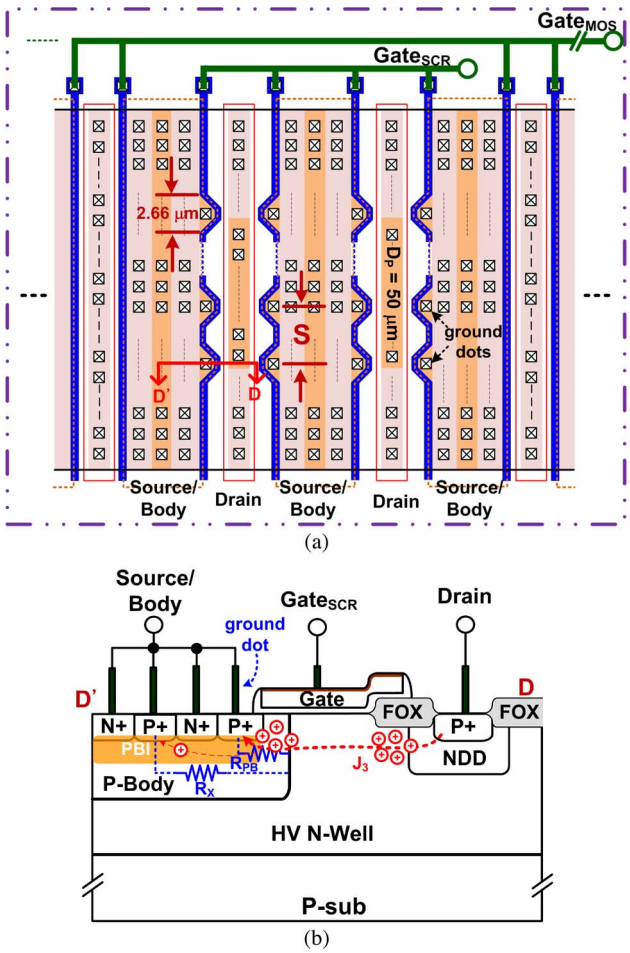

Fig. 10. (a) Layout top view and (b) cross-sectional view along the D-D′ line of SCR-nLDMOS with the proposed poly-bending structure. Widths and spacing in figures are not drawn to scale.

Gate_{SCR} fingers, as labeled in Fig. 2(b), therefore induce a voltage drop underneath the P+ anode of the embedded SCR, allowing holes to emit from the P+ anode. These emitting holes are illustrated as the J_3 current flow in Fig. 2(b). J_3 can be easily swept to grounded P+ body contacts to build up a voltage across the base–emitter junction of the parasitic n-p-n BJT because of a wide depletion region in HV n-well under high-V_{DS} voltages. For example, ggSCR-nLDMOS with D_P of 50 μm in Fig. 10 has the measured V_{DS} rating of 18.08 V under the 16-V gate bias, which is high enough to create a wide depletion region in HV n-well in the studied 24-V process and help sweep the J_3 current toward grounded P+ body contacts.

For HV nLDMOS, it has been reported that the effectiveness of the channel current to accelerate the carrier multiplication process under high-V_{DS} voltages can be relatively weak when gate biases are low. This comes from the mismatch on locations of the maximum current density and the maximum electric field under low gate biases. When the gate bias is high enough to induce channels underneath field oxide, coinciding of the channel current and the strong electric field start to accelerate the electron–hole pair generation. Therefore, it was observed that V_{t1} of HV nMOS only starts to significantly rolloff under high gate biases [18], [19]. Accordingly, the effect of this J_3 current due to drifting electrons becomes weak under low gate biases. Triggering of the embedded SCR under low gate biases mainly comes from avalanche-generated electron–hole pairs in the Gate_{SCR} fingers themselves. The device breakdown voltage (I_{DS} at 1 μA when V_{GS} is 0 V) measured by a 4155 parameter analyzer is ~35 V, and such measurement results show that this device breakdown voltage is irrelevant to the D_P width. Under high gate biases, the effect of J_3 becomes stronger because of a higher number of drifting electrons from the Gate_{MOS} fingers, and the measured V_{DS} ratings start to rolloff below 35 V with a faster speed, as shown in Fig. 9.

IV. Poly-Bending Structure to SCR-nLDMOS

Despite a remarkably wider eSOA that has been achieved by eliminating the J_1 and J_2 currents through connecting Gate_{SCR} to ground, the J_3 current still causes some degradation on eSOA performance, particularly under high gate biases. To further improve the eSOA and alleviate degradation due to J_3, a new poly-bending (PB) layout structure for SCR-nLDMOS arrays (PB-SCR-nLDMOS) has been proposed. For all studied PB-SCR-nLDMOS in this paper, the D_P width was kept at 50 μm, and devices were drawn with the PBI layer.

In the PB layout, Gate_{SCR} has been modified from a straight poly line from top to bottom of drain regions to part of a straight poly line in parallel with the N+ drain but several trapezoids in parallel with P+ drain, as the layout top view of a PB-SCR-nLDMOS shown in Fig. 10(a). By bending the poly gate in the layout, additional P+ diffusion regions filling trapezoids can be inserted at the source side. Each trapezoid region was drawn with one contact (ground dot) connecting to the source/body. The bottom length of every trapezoid is 2.66 μm (top edge of P+ to bottom edge of P+), and the pitch between two adjacent ground dots is defined as S in the layout of Fig. 10(a).

The device cross-sectional view along the D-D′ line in Fig. 10(a) is shown in Fig. 10(b). When the emitting holes from the P+ anode are swept toward the ground potential (the J_3 current flow), most of the emitting holes are collected by the ground dot because its parasitic resistance R_{PB} is smaller than the parasitic resistance R_X from the P-body/PBI to the P+ body contact, as shown in Fig. 10(b). Moreover, holes collected by the ground dots do not build up the voltage underneath the N+ source, i.e., do not help forward bias the base–emitter junction of n-p-n BJT. Accordingly, only a small part of J_3 that is not collected by the ground dot can help trigger the embedded SCR, which, in turn, substantially alleviates degradation on the eSOA due to the J_3 current flow.

The measured eSOA for PB-SCR-nLDMOS arrays is shown in Fig. 11. For comparison, the measured eSOA of ggSCR-nLDMOS with D_P of 50 μm in Fig. 9 is also included in Fig. 11 and labeled as ggSCR-nLDMOS. In Fig. 11, PB structures that have Gate_{SCR} connected to Gate_{MOS} show narrower eSOA boundaries compared to those of ggSCR-nLDMOS when S are 10 and 15 μm. When S is reduced to 5 μm, the PB structure (with Gate_{SCR} connected to Gate_{MOS}) shows a better eSOA performance than that of ggSCR-nLDMOS in Fig. 11. In the studied PB structures, because the bottom length of a trapezoid is 2.66 μm, S of 15 μm indicates that there is a 12.34-μm-long straight poly line between two ground dots to induce the J_1 and

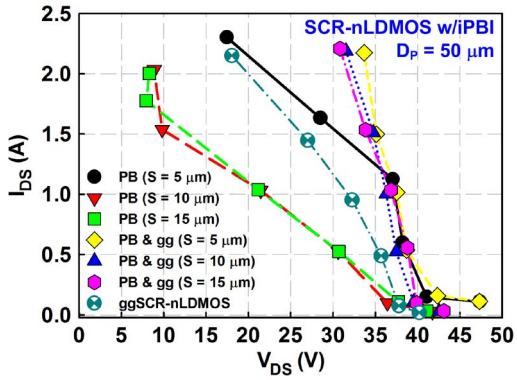

Fig. 11. Performance of the poly-bending structure on eSOA of SCR-nLDMOS. The "PB" devices have the poly-bending structure with Gate_{SCR} internally connected to Gate_{MOS}. The "PB & gg" devices have the poly-bending structure with Gate_{SCR} internally connected to source/body. The corresponding gate biases for the I_{DS} from low to high were 0, 3, 6, 9, 12, and 16 V, respectively.

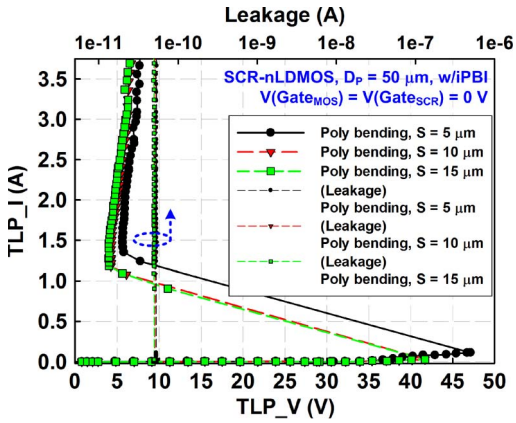

Fig. 12. Measured TLP I–V characteristics of poly-bending SCR-nLDMOS with different S spacing. The gate bias for all DUTs was 0 V, and the leakage currents were monitored under a 24-V drain bias.

J_2 currents and to further trigger on the embedded SCR when Gate_{SCR} is connected to Gate_{MOS}. When S is larger than 5 μm, the J_1 and J_2 currents dominate the triggering mechanism of the embedded SCR so that measurement results for PB with S of 10 and 15 μm are inferior to ggSCR-nLDMOS in Fig. 11. However, by comparing the eSOA of SCR-nLDMOS with 50-μm D_P and PBI in Fig. 7 and the eSOA of PB-SCR-nLDMOS with S of 10 and 15 μm in Fig. 11, improvement on eSOA by using the PB layout structure is still noticeable. This result comes from the fact that the ground dots introduce another parasitic resistor R_{PB} in parallel with the R_X resistor in Fig. 5, which widens the eSOA boundary by making the base–emitter junction of parasitic n-p-n BJT harder to be forward biased. When S is reduced to 5 μm, the straight poly line between two adjacent ground dots, which can induce the J_1 and J_2 currents is greatly reduced to 2.34 μm. Note that there is no channel current flowing widthwise along the trapezoidal regions because of the P+ region in ground dots to cutoff electron current flow [see Fig. 10(b)]. A better eSOA performance is therefore observed when S is reduced to 5 μm.

When Gate_{SCR} is connected to the source/body to rule out the effects from J_1 and J_2, effectiveness of the PB structure on suppressing J_3 starts to clearly manifest. Substantially widened eSOA boundaries, particularly under high gate biases, have been observed from the measurement results in Fig. 11 (PB & gg devices). Measured V_{DS} ratings for PB & gg devices in Fig. 11 under the 16-V gate bias are 30.81, 31.52, and 33.67 V for S of 15, 10, and 5 μm, respectively. In summary, grounding the Gate_{SCR} fingers not only blocks the J_1 and J_2 currents but also benefits from the reduced surface field (RESURF) effect of poly-field plate in the Gate_{SCR} fingers. The additional P+ ground dots in the PB structure further reduce the bipolar beta gain and lower the base resistance of parasitic n-p-n BJTs. With the aforementioned reasons, the eSOA of SCR-nLDMOS can be greatly improved by using the PB layout structure with the grounded Gate_{SCR} fingers.

TLP-measured I–V characteristics for PB-SCR-nLDMOS with D_P of 50 μm are shown in Fig. 12. All measured devices in Fig. 12 have I_{t2} higher than the equipment limitation of 3.75 A. Measured holding voltages V_h for PB-SCR-nLDMOS with S of 15, 10, and 5 μm in Fig. 12 are 3.99, 4.26, and 5.67 V, respectively. Measured V_h for SCR-nLDMOS with D_P of 50 μm in Fig. 6(b) is 2.14 V. Accordingly, from the viewpoint of power dissipation during ESD stresses, the PB structure is expected to have some negative impact on the ESD robustness. However, because the measured HBM ESD robustness for all DUTs in Fig. 12 is higher than 8 kV, the PB-SCR-nLDMOS arrays are still extremely robust against ESD stresses.

V. Conclusion

In HV technologies, output arrays with an embedded SCR are usually adopted for on-chip ESD protection. However, a substantially narrowed eSOA has been found in this paper due to the insertion of SCR into HV nLDMOS. Embedding SCR, therefore, may jeopardize the reliability of output arrays during normal circuit operating conditions, although it provides superior ESD robustness to protect an output array. Experimental results showed that SCR insertion with small but multiple P+ segments can help alleviate degradation on eSOA. By grounding the gates of fingers in the embedded SCR, eSOA can be substantially widened. However, drifting electrons due to the carrier multiplication process from adjacent conducting fingers can still result in a rolloff on the maximum V_{DS} rating, particularly under high gate bias conditions. Through the proposed PB structure, impact from these drifting electrons can be mitigated, and a further widened eSOA has been achieved. With the high ESD robustness and greatly widened eSOA boundaries shown in this paper, the PB layout structure with a proper gate connection has been verified as a promising design technique to enhance reliability of HV output arrays with the embedded SCR.

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