Layout-Dependent Stress Effect on High-Frequency Characteristics and Flicker Noise in Multifinger and Donut MOSFETs

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***Abstract*—The impact of MOSFET layout-dependent stress on high-frequency performance and flicker noise has been investigated. The proposed donut MOSFETs demonstrate the advantages over the standard multifinger MOSFETs, such as the lower flicker noise $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ in the low-frequency domain and the higher cutoff frequency f_T in the very high-frequency region. The elimination of the transverse stress $\sigma_\perp$ from shallow trench isolation (STI) and the suppression of interface traps along the STI edge are proposed as the primary factors responsible for the enhancement of the effective mobility μ_{eff}, as well as f_T, and the reduction of flicker noise. The significantly lower flicker noise realized by donut devices suggests the reduction of STI-generated traps and the suppression of mobility fluctuation due to eliminated transverse stress. The former is applied to n-channel MOS in which the flicker noise is determined by the number-fluctuation model. The latter is responsible for p-channel MOS whose flicker noise is dominated by the mobility-fluctuation model.**

***Index Terms*—Cutoff frequency, donut, flicker noise, longitudinal stress, mobility, shallow trench isolation (STI), transverse stress.**

I. Introduction

With the advancement of CMOS technology to the nanoscale regime, the stress introduced from the materials and the process becomes more sensitive to the device layout and topography. The shallow trench isolation (STI) process will induce compressive stress and traps, which may have impact on flicker noise (i.e., $1/f$ noise) in both nMOS and pMOS devices [1]–[4]. Fantini and Ferrari investigated the influence of compressive stress from STI on low field mobility and the impact on $1/f$ noise for nMOS and pMOS [3]. This paper is restricted to wide-channel devices in which the longitudinal stress $\sigma_{//}$ can be modulated by varying the distance of the STI edge to the poly-gate edge, i.e., SA, but the effect of transverse stress $\sigma_\perp$ remains unknown. Their experimental results indicate that the electron mobility is degraded, whereas the hole mobility is enhanced under increasing compressive $\sigma_{//}$ by shrinking SA [3]. The increase in compressive $\sigma_{//}$ can benefit pMOS with higher hole mobility but leads to the penalty of increasing $1/f$ noise. Wang *et al.* reported the STI-edge effect on the random-telegraph-signal noise and proposed ring transistors as the structure, trying to eliminate the STI-edge effect [4]. Their study is limited to nMOS, and the ring transistors demonstrate a lower noise factor than the standard one when scaling the channel width below 1.5 μm. In contrast with the work by Fantini *et al.*, this paper limits the focus on the effect of $\sigma_\perp$, which is varied by channel widths, and assumes a $\sigma_{//}$ constant under fixed SA. Both of them adopted a single-finger MOSFET with fixed SA as the standard device and left the impact of STI stress on high-frequency performance as an open question.

Recently, layout-dependent STI stress and its impact on high-frequency characteristics, as well as flicker noise, have been investigated but limited to the nMOS [5], [6]. A minor layout modification, i.e., edge extension, was implemented to reduce the stress and traps introduced by STI [5]. However, the edge-extended layout cannot prevent from the gate-to-STI-edge overlap region and leaves the STI stress an impact factor. Again, a ring transistor was proposed, trying to solve the mentioned problem and identify the influence of the transverse stress $\sigma_\perp$ on flicker noise [4], [6]. However, the impact on high-frequency performance is not understood. Furthermore, both studies of edge-extended and ring-transistor layouts did not cover pMOS, which is even more important than nMOS for low-phase-noise design in RF and analog applications.

In this paper, a new MOSFET layout, i.e., the donut layout, is proposed to create the devices free from the STI transverse stress $\sigma_\perp$ along the width direction to explore the impact on transconductance G_m, the effective mobility μ_{eff}, the cutoff frequency f_T, and flicker noise. Meanwhile, an extensive investigation is performed on both nMOS and pMOS to explore the STI-stress effect on the channel current I_{DS}, f_T, and flicker noise. For each device structure under a specified bias, the flicker noise is averaged from multiple dies to represent the statistics of die-to-die variation. This paper is aimed to identify the impact from STI stress on high-frequency characteristics as well as flicker noise, and the results can guide MOSFET layout optimization for RF and analog circuit design.

II. Device Fabrication and Characterization

In this paper, the devices were fabricated in a 90-nm low-leakage CMOS process, with the drawn gate length L_{drawn} of

Manuscript received April 19, 2011; revised May 22, 2011; accepted June 2, 2011. Date of publication July 12, 2011; date of current version August 24, 2011. This work was supported in part by the National Science Council under Grant NSC98-2221-E009-166-MY3. The review of this paper was arranged by Editor Z. Celik-Butler.

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Digital Object Identifier 10.1109/TED.2011.2159223

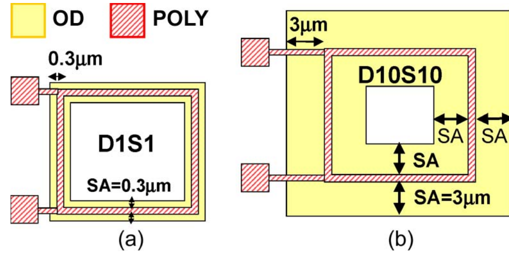

Fig. 1. Brief layout of donut MOSFET (a) D1S1, SA $= 0.3$ μm and (b) D10S10, SA $= 3$ μm with two major layers, such as active region (OD) and poly gate (PO).

80 nm and the gate-oxide thickness T_{ox} of 2.2 nm. Note that the electrical equivalent thickness under strong inversion $T_{\mathrm{ox(inv)}}$ is 3 nm, corresponding to a 2.2-nm T_{ox} and $\mathrm{CoSi}_2/\mathrm{poly}$-Si gate. In order to investigate the stress and interface traps generated near the STI edge, two types of MOSFET layouts, i.e., standard and donut, are designed and implemented. The total gate width W_{tot} is fixed at 64 μm: 2 μm $\times$ 32 for the multifinger MOSFET and 16 μm $\times$ 4 for the donut MOSFET. Note that the multifinger MOSFET denoted as W2N32 represents the standard device. As shown in Fig. 1, the donut MOSFETs are constructed as four-side polygons in which the corners contribute very little to the channel current [4], [7]. Two layout dimensions, which are denoted as D1S1 and D10S10, were implemented. In Fig. 1(a), D1S1 represents a donut MOSFET in which the space from the poly-gate edge to the STI edge, which is defined as SA, follows the minimum rule, i.e., SA $=$ 0.3 μm, to maximize the compressive stress from STI and along the channel (i.e., the longitudinal stress $\sigma_{//}$). Meanwhile, D10S10 shown in Fig. 1(b) denotes the donut MOSFET with ten times larger space between the poly-gate edge and the STI edge, i.e., SA $= 3$ μm, intentionally to relax $\sigma_{//}$ from STI.

Scattering parameters were measured by an Agilent E8364B network analyzer for high-frequency characterization and the extraction of gate capacitances and cut-off frequency. Open-and-short deembedding was performed to remove the parasitic capacitances from the pads, as well as interconnection lines, and the resistances from all of the metal interconnects. The power spectral density of drain-current noise S_{ID} was measured by low-frequency-noise (LFN) measurement system, consisting of Agilent dynamic signal analyzer (DSA 35670) and low-noise amplifier (LNA SR570). The LFN measurement generally covers a wide frequency range from 4 Hz to 10 kHz. The LFN was measured under various gate overdrive $|V_{\mathrm{GT}}| = 0.1 \sim 0.7$ V and fixed $|V_{\mathrm{DS}}| = 50$ mV for both nMOS and pMOS.

III. Results and Discussion

At first, STI stress introduced in MOSFETs with three different layouts as mentioned (standard W2N32, donut D1S1, and D10S10) is illustrated in Fig. 2 to assist an analysis and an understanding of the layout effect on STI stress and, then, the electrical characteristics. Note that STI stress is classified as longitudinal stress, which is denoted as $\sigma_{//}$, which is in parallel with the channel, and transverse stress, i.e., $\sigma_{\perp}$, which is transverse to the channel. We can see that standard MOSFETs [see Fig. 2(a)] are subject to $\sigma_{//}$ along the channel length and

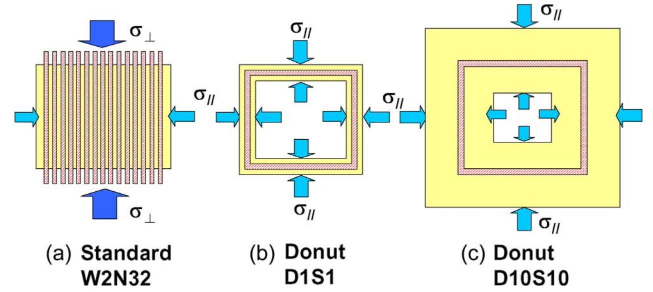

Fig. 2. Schematics of STI stress in MOSFETs with three different layouts (a) standard multi-finger device W2N32 (b) donut device D1S1 (c) donut device D10S10. Longitudinal stress : $\sigma_{//}$ in parallel with the channel, transverse stress: $\sigma_{\perp}$ transverse to the channel.

TABLE I
Stress Favorable for Mobility Enhancement in NMOS and PMOS Along Longitudinal and Transverse Directions [8]

Directions	Stress favorable for mobility enhancement	
	NMOS	PMOS
Longitudinal ($\sigma_{//}$)	Tensile	Compressive
Transverse ($\sigma_{\perp}$)	Tensile	Tensile

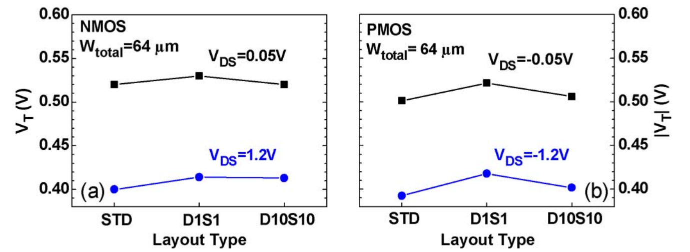

Fig. 3. Threshold voltage V_T measured for standard and donut devices under linear and saturation bias conditions (a) NMOS (b) PMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

$\sigma_{\perp}$ along the gate width. On the other hand, donut MOSFETs are free from $\sigma_{\perp}$. Regarding the stress favorable for mobility enhancement, it has critical dependence on the device types and orientations, as shown in Table I [8]. For nMOS, tensile stress, i.e., either $\sigma_{//}$ or $\sigma_{\perp}$, can improve μ_{eff}. As for pMOS, compressive stress in $\sigma_{//}$ or tensile stress in $\sigma_{\perp}$ is the right one for μ_{eff} enhancement.

A. Layout Effects on Threshold Voltage V_T: Standard and Donut MOSFETs

Fig. 3(a) and (b) presents the threshold voltage V_T measured in linear and saturation regions for nMOS and pMOS with standard multifinger and donut layouts (D1S1 and D10S10), respectively. As shown in Fig. 3(a), the standard nMOS (W2N32) indicates a smaller V_T value, which is 10–15 mV lower than that of D1S1 and nearly the same as that of D10S10. A similar layout effect on V_T is demonstrated for pMOS, as shown in Fig. 3(b), where the V_T lowering from D1S1 to W2N32 is around 18–20 mV for both linear and saturation regions. The results suggest that V_T rolls off due to the narrow-width effect, i.e., the inverse narrow-width effect, which is a minor effect for W2N32 compared with donut devices. In this paper, the gate

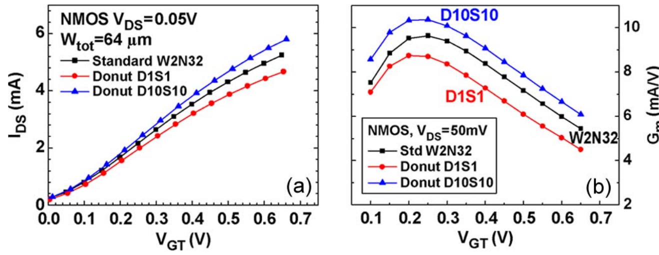

Fig. 4. Drain current $I_{\rm DS}$ and transconductance G_m in linear region for standard NMOS W2N32 and donut NMOS D1S1, D10S10 (a) $I_{\rm DS}$ versus $V_{\rm GT}$ (b) G_m versus $V_{\rm GT}$. $V_{\rm GT} = V_{\rm GS} - V_T$, $V_{\rm DS} = 0.05$ V.

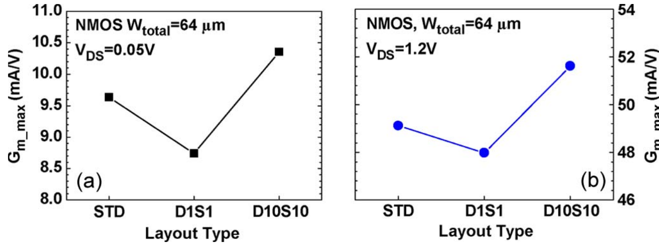

Fig. 5. Maximum transconductance $G_{m_\max}$ measured from standard and donut NMOS in (a) linear region $V_{\rm DS} = 0.05$ V and (b) saturation regions $V_{\rm DS} = 1.2$ V. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

overdrive $V_{\rm GT} = V_{GS} - V_T$ is used to replace the gate bias V_{GS} to offset the V_T variation from different layouts.

B. Layout Dependence of $I_{\rm DS}$, G_m, and $\mu_{\rm eff}$: Standard and Donut nMOS

Fig. 4(a) and (b) presents the channel current $I_{\rm DS}$ and transconductance G_m measured from nMOS under various $V_{\rm GT}$ in the linear region ($V_{\rm DS} = 50$ mV). As shown in Fig. 4(a), the donut nMOS D10S10 can offer the highest $I_{\rm DS}$, but D1S1 suffers the lowest one, as compared with the standard nMOS (W2N32). G_m shown in Fig. 4(b) just follows the same trend of layout dependence as that of $I_{\rm DS}$, i.e., D10S10 gains the highest G_m but D1S1 suffers the worst one. Fig. 5(a) and (b) makes a comparison of maximum G_m ($G_{m,\max}$) between three different layouts, i.e., standard (W2N32), D1S1, and D10S10 for nMOS in linear and saturation regions ($V_{\rm DS} = 50$ mV and 1.2 V). The results indicate that $G_{m,\max}$ of D10S10 is enhanced by 7.5% but that of D1S1 is degraded by around 9.7%, as compared with the standard nMOS (W2N32). The experimental result suggests that compressive $\sigma_{//}$ from STI, which is maximized in D1S1 due to the minimum SA, is the primary factor responsible for $G_{m,\max}$ degradation. As for D10S10, the much lower $\sigma_{//}$ due to ten times larger SA and eliminated $\sigma_\perp$ from the donut layout contributes to the $G_{m,\max}$ improvement.

The influence on $\mu_{\rm eff}$ shown in Fig. 6 reveals exactly the same trend as that of $G_{m,\max}$. The donut nMOS D10S10 gains an enhancement of 7.45%, whereas D1S1 suffers 9.2% degradation in $\mu_{\rm eff}$, i.e., compared with the standard nMOS. The results justify the mechanism that the layout dependence of $G_{m,\max}$ is originated from the effect of STI stress $\sigma_{//}$ and $\sigma_\perp$ on electron mobility summarized in Table I.

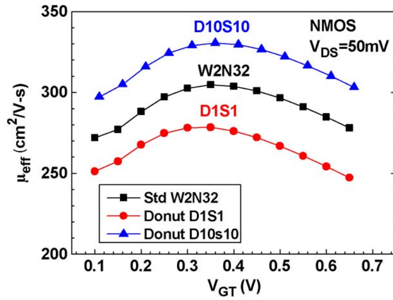

Fig. 6. Effective mobility $\mu_{\rm eff}$ extracted from linear I–V for standard and donut NMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

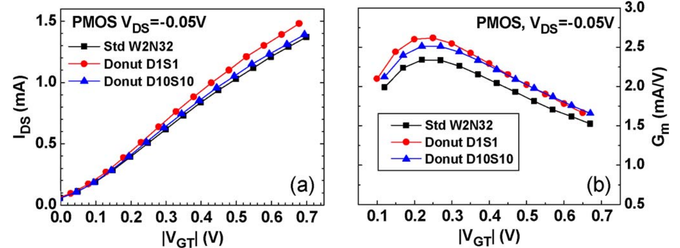

Fig. 7. Drain current $I_{\rm DS}$ and transconductance G_m in linear region for standard PMOS W2N32 and donut PMOS D1S1, D10S10 (a) $I_{\rm DS}$ versus $|V_{\rm GT}|$ (b) G_m versus $|V_{\rm GT}|$. $V_{\rm GT} = V_{\rm GS} - V_T$, $V_{\rm DS} = -0.05$ V.

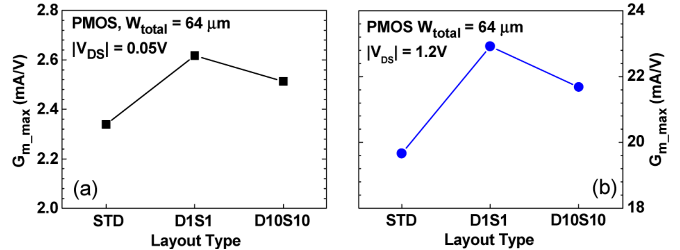

Fig. 8. Maximum transconductance $G_{m_\max}$ measured from standard and donut PMOS in (a) linear region $V_{\rm DS} = -0.05$ V and (b) saturation regions $V_{\rm DS} = -1.2$ V. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

C. Layout Dependence of $I_{\rm DS}$, G_m, and $\mu_{\rm eff}$: Standard and Donut pMOS

As for pMOS with the mentioned three layouts (W2N32, D1S1, and D10S10), the measured $I_{\rm DS}$ and G_m shown in Fig. 7(a) and (b) indicate the best performance in donut pMOS D1S1, whereas the worst one in standard pMOS (W2N32). The results from pMOS are very different from those demonstrated for nMOS. Again, Fig. 8 presents a comparison of $G_{m,\max}$ between three different layouts for pMOS. We can see that the donut pMOS D1S1 and D10S10 demonstrate 12.2% and 7.6% higher $G_{m,\max}$ in the linear region than that of standard pMOS (W2N32). The effective mobility $\mu_{\rm eff}$ extracted from linear $I-V$, as shown in Fig. 9, just reveal the same trend of layout dependence as that of $G_{m,\max}$. The donut pMOS D1S1 and D10S10 present a $\mu_{\rm eff}$ enhancement of 12.5% and 6.3%, respectively, compared with the standard pMOS. According to Table I, it can be explained that D1S1 with the minimum SA, resulting the highest compressive $\sigma_{//}$ and minimized $\sigma_\perp$, can benefit the most in hole mobility. The standard pMOS (W2N32) with relieved $\sigma_{//}$ in the multifinger structure and the largest $\sigma_\perp$ along the narrow width suffer the worst hole mobility.

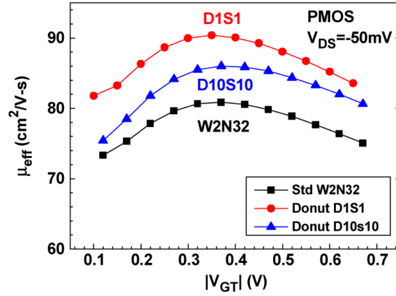

Fig. 9. Effective mobility μ_{eff} extracted from linear I–V for standard and donut PMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

The significant difference of μ_{eff} revealed in the donut MOSFETs with various SA, such as SA $= 3$ μm for D10S10 and SA $= 0.3$ μm for D1S1, can be used to extract the average $\sigma_{/\!/}$. Regarding the extraction of average $\sigma_{\perp}$, single-finger MOSFETs with various channel widths and different gate orientations such as x and y are required to make a one-to-one comparison with the donut MOSFETs, which can eliminate $\sigma_{\perp}$ and act as the reference device. In this paper, single-finger MOSFETs are not available, and the extraction of $\sigma_{\perp}$ is considered as an interesting topic for future work. The method of stress extraction can be referred to our previous work [9] and applied to the donut MOSFETs as follows:

$$\frac{\Delta\mu}{\mu_0} = -(k_{\perp}\sigma_{\perp} \pm k_{/\!/}\sigma_{/\!/}) \tag{1}$$

where

μ_0 mobility of the reference device, free from $\sigma_{/\!/}$ and $\sigma_{\perp}$;

$\Delta\mu$ mobility variation due to STI stress, $\sigma_{/\!/}$ and $\sigma_{\perp}$;

$k_{/\!/}$ first order of coefficient for mobility variation from $\sigma_{/\!/}$ + for nMOS and − for pMOS;

$k_{\perp}$ first order of coefficient for mobility variation from $\sigma_{\perp}$.

For donut MOSFETs, $\sigma_{\perp}$ is negligibly small, and (1) can be reduced to

$$\frac{\Delta\mu}{\mu_0} \cong -(\pm k_{/\!/}\sigma_{/\!/}). \tag{2}$$

Assume that both $\sigma_{/\!/}$ and $\sigma_{\perp}$ are negligibly small in donut D10S10 and the μ_{eff} extracted from D10S10 is defined as μ_0. Then, component $k_{/\!/}\sigma_{/\!/}$ can be extracted from the mobility variation $\Delta\mu$ compared with the μ_0 of the reference (D10S10), which is given by (2), and $\sigma_{/\!/}$ is determined by (3) as a function of the ratio between SA_{ref} of the reference and the SA of the specified device as follows:

$$\sigma_{/\!/} = k \cdot \log\left(\frac{\text{SA}_{\text{ref}}}{\text{SA}}\right). \tag{3}$$

From (2) and (3)

$$\frac{\Delta\mu}{\mu_0} \cong -\left[\pm k_{/\!/}k \cdot \log\left(\frac{\text{SA}_{\text{ref}}}{\text{SA}}\right)\right] \tag{4}$$

$$\Delta\mu = \mu_{\text{eff}}(\text{SA}) - \mu_0 \tag{5}$$

$$\mu_0 = \mu_{\text{eff}}(\text{SA}_{\text{ref}}). \tag{6}$$

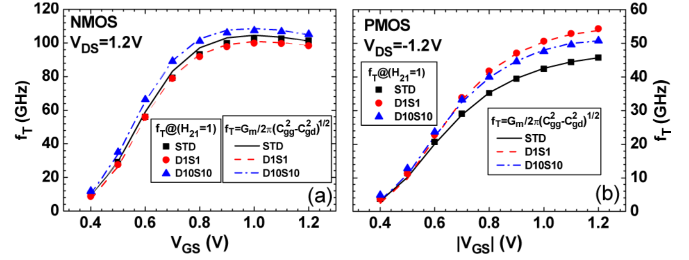

Fig. 10. Measured and calculated f_T versus V_{GS} ($|V_{\text{DS}}| = 1.2$ V) for standard and donut MOSFETs (a) NMOS (b) PMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

Factor $k_{/\!/}k$ can be extracted from (4)–(6), with $\text{SA}_{\text{ref}} = 3$ μm for D10S10 and SA $= 0.3$ μm for D1S1. Hereafter, the mobility variation from $\sigma_{/\!/}$ for donut MOSFETs with various SA ($\leqq \text{SA}_{\text{ref}}$) values can be predicted by (4).

D. High-Frequency Performance of Donut and Standard MOSFETs

The impact of layout-dependent STI stress on high-frequency performance is of special concern, and the cutoff frequency f_T is recognized as the key performance parameter for RF devices and circuits design. Fig. 10(a) and (b) illustrates the measured and calculated f_T for nMOS and pMOS with donut and standard layouts. Note that f_T is extracted from the extrapolation of $|H_{21}|$ to unity gain and defined as $f_T = f(|H_{21}| = 1)$. For nMOS shown in Fig. 10(a), the donut D10S10 gains an improvement of 5% in the maximum f_T compared with the standard and D1S1. The benefit from the donut layout becomes particularly larger for pMOS. As shown in Fig. 10(b), the donut pMOS D1S1 presents the best performance with the highest f_T and realizes a 28% increase in the maximum f_T than the standard pMOS.

The improvement of f_T measured from donut MOSFETs can be explained consistently by the enhancement of μ_{eff} and G_m, according to the f_T calculated by the analytical model as a function of G_m and gate capacitances C_{gg} and C_{gd}, which is given by (7) [10] in the following:

$$f_T = \frac{G_m}{2\pi\sqrt{C_{gg}^2 - C_{gd}^2}} \tag{7}$$

$$C_{gg} = \frac{\text{Im}(Y_{11})}{\omega} \tag{8}$$

$$C_{gd} = -\frac{\text{Im}(Y_{12})}{\omega}. \tag{9}$$

A good match between the measured and calculated f_T, as shown in Fig. 10(a) and (b), for both nMOS and pMOS with different layouts (W2N32, D1S1, and D10S10) justifies the accuracy of the proposed analytical model. According to (7), it is predicted that f_T is proportional to G_m and the enhancement of G_m can boost f_T under fixed gate capacitances (i.e., C_{gg} and C_{gd}). The gate capacitances C_{gg} and C_{gd} can be extracted from two-port Y-parameters according to (8) and (9). The results shown in Fig. 11(a) and (b) for nMOS and pMOS indicate negligibly small difference in C_{gg} and C_{gd} between the donut

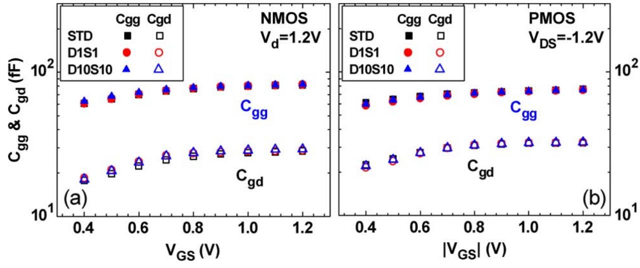

Fig. 11. Gate capacitances C_{gg} and C_{gd} versus V_{GS} extracted from $\mathrm{Im}(Y_{11})$ and $\mathrm{Im}(Y_{12})$ for standard and donut MOSFETs (a) NMOS (b) PMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

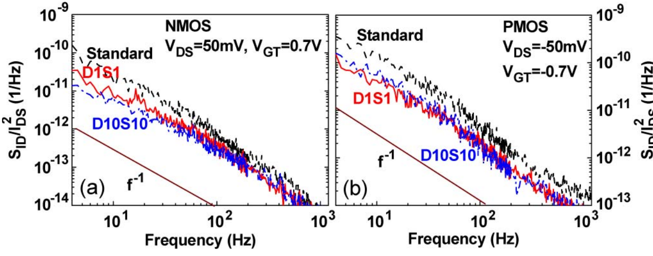

Fig. 12. Low frequency noise $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ versus frequency ($|V_{\mathrm{DS}}| = 0.05$ V, $|V_{\mathrm{GT}}| = 0.7$ V) measured from the standard and donut MOSFET (a) NMOS (b) PMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

and standard layouts, as compared with that of G_m (see Figs. 5 and 8). Therefore, the layout dependence of f_T just follows that of G_m, i.e., the higher f_T corresponding to the larger G_m. Regarding other RF performance parameters such as the maximum oscillation frequency $f_{\max}$ and the noise figure $\mathrm{NF}_{\min}$ (not shown), the donut MOSFETs may suffer certain degree of degradation due to inherently larger gate resistances than the standard multifinger MOSFETs. The experimental results suggest that an innovative donut device layout is required to cover all of the RF and analog performance.

E. LFN of Standard and Donut MOSFETs

Fig. 12(a) and (b) makes a comparison of LFN in terms of S_{ID}/I_D^2 between the standard and donut layouts for nMOS and pMOS, respectively. The noise spectrum follows the $1/f$ function over a wide frequency range from 4 to 10 kHz. It means that the measured LFN is typical flicker noise. The standard device (W2N32) reveals nearly twice larger S_{ID}/I_D^2 compared with the donut devices (D1S1 and D10S10) for both nMOS and pMOS, under the specified gate overdrive voltage $|V_{\mathrm{GT}}| = 0.7$ V. In contrast, the donut device D10S10 with the most extended gate-to-STI-edge distance indicates the lowest S_{ID}/I_D^2. The results can be explained consistently by the fact that D10S10 can keep free from $\sigma_\perp$, as well as interface traps near the STI edge, and the smallest $\sigma_{//}$ due to ten times larger space away from the STI edge compared with D1S1.

To explore the mechanism responsible for the LFN, $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ measured at 50 Hz and various $|V_{\mathrm{GT}}|$ (0.1–0.7 V) are plotted versus $(G_m/I_{\mathrm{DS}})^2$ for three different layouts (W2N32, D1S1, and D10S10), as shown in Fig. 13. For nMOS shown in Fig. 13(a), measured $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ reveals a linear increasing function of $(G_m/I_{\mathrm{DS}})^2$ for all three devices. As for pMOS

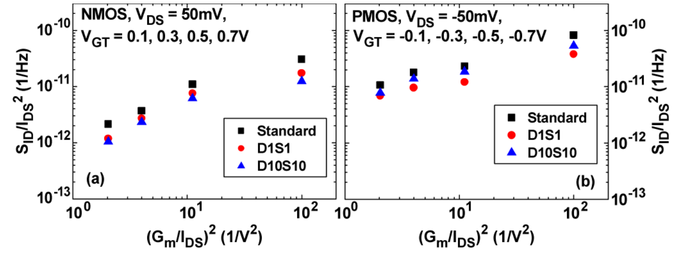

Fig. 13. Low frequency noise $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ versus $(G_m/I_{\mathrm{DS}})^2$ under various $|V_{\mathrm{GT}}|$ ($0.1 \sim 0.7$ V) for standard and donut devices (a) NMOS (b) PMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

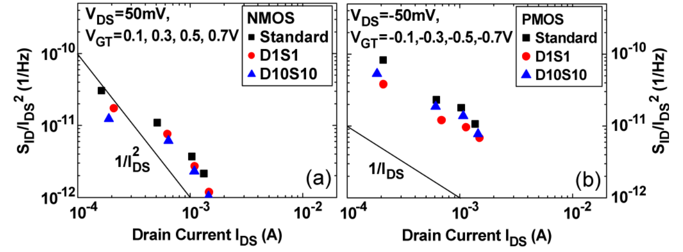

Fig. 14. Low frequency noise $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ versus I_{DS} under varying $|V_{\mathrm{GT}}|$ ($0.1 \sim 0.7$V) for standard and donut devices (a) NMOS (b) PMOS. Standard : multi-finger W2N32. Donut : D1S1 and D10S10.

shown in Fig. 13(b), measured $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ indicates weak dependence on $(G_m/I_{\mathrm{DS}})^2$ in the strong inversion region ($|V_{\mathrm{GT}}| = 0.3-0.7$ V) and a minor increase under weak inversion at the lowest $|V_{\mathrm{GT}}| = 0.1$ V. Referring to the drain-current fluctuation model proposed in [11], as given by (10), the first term represents the carriers number fluctuation, and the second term denotes the correlated mobility fluctuation. $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ measured from nMOS [see Fig. 13(a)], revealing a good linear function of $(G_m/I_{\mathrm{DS}})^2$, is dominated by the first term in (10), i.e., the carriers number fluctuation. As for the pMOS, measured $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ [see Fig. 13(b)], showing nearly a constant independent of $(G_m/I_{\mathrm{DS}})^2$, suggests the dominance of the second term in (10), i.e., the correlated mobility fluctuation.

To verify further the mechanism, measured $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ is plotted versus I_{DS}, as shown in Fig. 14. For nMOS, $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ shown in Fig. 14(a) indicates a good match with the number-fluctuation model given by (11) in which $S_{\mathrm{ID}}/I_{\mathrm{DS}}^2$ under various V_{GT} is proportional to N_t/I_{DS}^2, and that predicts the increase in flicker noise with increasing the traps' density N_t [12]. It is believed that the gate-to-STI-edge overlap region will suffer the most severe compressive strain, as well as the interface traps N_t, and the donut devices can eliminate these effects along the gate width, i.e., in the transverse direction. According to a previous study, the stress-generated traps may aggravate the scattering effect and increase the flicker noise [13]. The mentioned mechanism can explain why the donut MOSFETs, which are free from the gate-to-STI-edge overlap region can achieve the lowest flicker noise.

$$\frac{S_{\mathrm{ID}}}{I_{\mathrm{DS}}} = \frac{q^2 k_B T \lambda N_t}{f^\gamma W L C_{\mathrm{ox}}^2} W L C_{\mathrm{ox}}^2 \left(1 + \alpha \mu_{\mathrm{eff}} C_{\mathrm{ox}} \frac{I_{\mathrm{DS}}}{G_m}\right)^2 \left(\frac{G_m}{I_{\mathrm{DS}}}\right)^2 \quad (10)$$

$$\frac{S_{\mathrm{ID}}}{I_{\mathrm{DS}}^2} = \frac{q^2 k_B T \lambda N_t}{f^\gamma} \frac{W \mu_{\mathrm{eff}}^2 V_{\mathrm{DS}}^2}{L^3} \frac{1}{I_{\mathrm{DS}}^2} \quad (11)$$

N_t : the density of traps at the quasi-Fermi level.

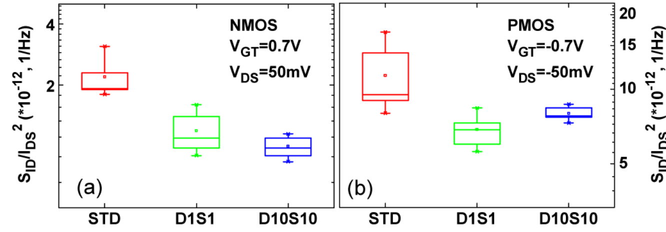

Fig. 15. Statistical distribution of $S_{\rm ID}/I_{\rm DS}^2$ ($|V_{\rm DS}| = 0.05$ V, $|V_{\rm GT}| = 0.7$ V) measured from standard (W2N32) and donut (D1S1, D10S10) devices (a) NMOS and (b) PMOS.

As for the pMOS shown in Fig. 14(b), measured $S_{\rm ID}/I_{\rm DS}^2$ follows a simple power law of $1/I_{\rm DS}$ and manifests itself governed by the mobility-fluctuation model, according to the Hooge empirical formula expressed in (12) [14]. In addition, the model for $S_{\rm ID}/I_{\rm DS}^2$ can be expressed as a function of $V_{\rm GT}$, which is given by (13). Note that the Hooge parameter α_H is dimensionless and may vary with biases and process technologies. The reduction of flicker noise measured from the donut pMOS suggests the suppression of mobility fluctuation due to the eliminated compressive $\sigma_\perp$. Furthermore, the increase in $|V_{\rm GT}|$ can help suppress the flicker noise in terms of $S_{\rm ID}/I_{\rm DS}^2$.

$$\frac{S_{\rm ID}}{I_{\rm DS}^2} = \frac{1}{f}\frac{\alpha_H \mu_{\rm eff}}{L^2}\frac{qV_{\rm DS}}{I_{\rm DS}} \qquad (12)$$

$$\frac{S_{\rm ID}}{I_{\rm DS}^2} = \frac{q}{f}\frac{1}{WLC_{\rm ox}} \times \frac{\alpha_H}{V_{\rm GT}}, V_{\rm GT} = (V_{GS} - V_T) \qquad (13)$$

α_H: the Hooge parameter.

Fig. 15 makes a comparison of the flicker noise in terms of $S_{\rm ID}/I_{\rm DS}^2$ between three different device layouts, incorporating die-to-die variations. For nMOS shown in Fig. 15(a), the standard device (STD: W2N32) reveals 85% higher $S_{\rm ID}/I_{\rm DS}^2$ in the mean value than donut devices (D1S1 and D10S10), and D10S10 manifests itself the best one with the minimum $S_{\rm ID}/I_{\rm DS}^2$. All of the three layouts present similar standard variation in the statistical distribution. The results justify that the donut layout can keep the MOSFETs free from $\sigma_\perp$, as well as interface traps near the STI edge, and then achieve lower $S_{\rm ID}/I_{\rm DS}^2$. For D10S10 compared with D1S1, ten times larger space away from the STI edge can effectively suppress $\sigma_{//}$ and push the flicker noise $S_{\rm ID}/I_{\rm DS}^2$ to a lower value. Similar results are demonstrated for pMOS in Fig. 15(b), but the standard pMOS (W2N32) reveals significantly higher $S_{\rm ID}/I_{\rm DS}^2$ in mean and standard variation, and the difference between two donut pMOS devices (D1S1 and D10S10) is very minor. As a result, the proposed STI stress and excess traps can explain the layout dependence of the flicker noise for both nMOS and pMOS.

To explore the mechanism responsible for the lower flicker noise in donut nMOS, the interface-trap density N_t appearing in the number-fluctuation model (11) was extracted from measured $S_{\rm ID}/I_{\rm DS}^2$ for nMOS with various layouts. Note that the tunneling attenuation length λ is specified as 1 Å and the frequency exponent γ is 1.7 for the Si/SiO_2 system [15]. The extracted trap density, as shown in Fig. 16, affirms that N_t can be reduced significantly by around twice for donut nMOS,

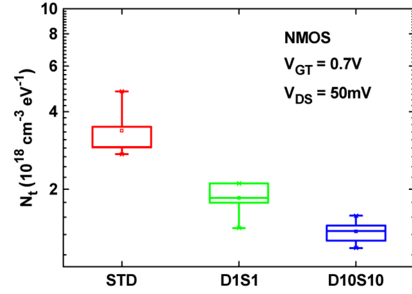

Fig. 16. Statistical distribution of interface trap density N_t extracted from number fluctuation model of LFN for standard (W2N32) and donut (D1S1, D10S10) NMOS. $V_{\rm DS} = 0.05$ V, $V_{\rm GT} = 0.7$ V.

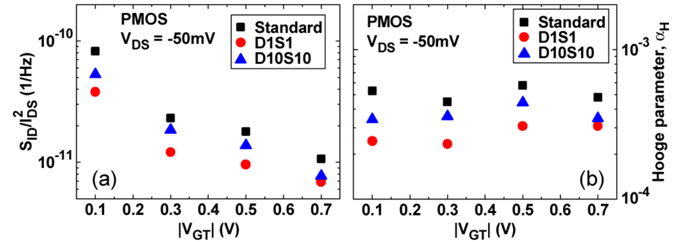

Fig. 17. (a) $S_{\rm ID}/I_{\rm DS}^2$ versus $V_{\rm GT}$ (b) Hooge parameter α_H versus $V_{\rm GT}$ for standard (WN32) and donut (D1S1, D10S10) PMOS. α_H is extracted from mobility fluctuation model.

as compared with standard nMOS. Furthermore, D10S10 has lower N_t, as compared with D1S1, due to the suppression of STI stress in both longitudinal and transverse directions, i.e., $\sigma_{//}$ and $\sigma_\perp$.

As for pMOS, the flicker noise is dominated by the mobility-fluctuation model described by (12) and (13) in which the Hooge parameter α_H appears as the key parameter to be determined. Fig. 17(a) presents $S_{\rm ID}/I_{\rm DS}^2$ under various $V_{\rm GT}$ values, which are measured from pMOS with specified three layouts (STD: W2N32, D1S1, and D10S10). The higher $|V_{\rm GT}|$ can help reduce $S_{\rm ID}/I_{\rm DS}^2$, which is attributed to an increase in inversion carriers and, then, higher $I_{\rm DS}$, as shown in (12) and (13). Note that the standard pMOS (W2N32) suffers the largest $S_{\rm ID}/I_{\rm DS}^2$, whereas the donut pMOS D1S1 indicates the lowest $S_{\rm ID}/I_{\rm DS}^2$, which may be attributed to the G_m and $\mu_{\rm eff}$ enhancement. According to measured $S_{\rm ID}/I_{\rm DS}^2$ and extracted $\mu_{\rm eff}$ (see Fig. 9), α_H can be determined from (12) or (13) under varying $I_{\rm DS}$ or $V_{\rm GT}$. The result shown in Fig. 17(b) indicates that α_H is weakly dependent on $V_{\rm GT}$ and its layout dependence just follows that of $S_{\rm ID}/I_{\rm DS}^2$. The standard pMOS reveals the largest α_H, and the donut pMOS D1S1 indicates the smallest α_H. The reduction of α_H and the resulted suppression of $S_{\rm ID}/I_{\rm DS}^2$ in donut pMOS suggest that the elimination of STI transverse stress $\sigma_\perp$ can reduce carrier scattering as well as mobility fluctuation and then lead to smaller α_H, which is determined by mobility fluctuation from multiple-scattering mechanisms [16].

IV. Conclusion

The proposed donut MOSFETs demonstrate the advantages over the standard multifinger MOSFETs, such as the lowest $S_{\rm ID}/I_{\rm DS}^2$ in the low-frequency domain (1–10 kHz) and higher f_T in the very high-frequency region (100/50 GHz for

N/P MOS). The elimination of STI stress and the suppression of interface traps along the gate width are validated as the primary mechanism responsible for the enhancement of $\mu_{\rm eff}$, as well as f_T, and the reduction of flicker noise. Both nMOS and pMOS can benefit from the donut layout, although their flicker noise is dominated by different mechanisms such as the number-fluctuation model and the mobility-fluctuation model, respectively. The layout dependence of STI stress and interface-trap density can explain consistently the advantages from the donut devices. An innovative donut MOSFET layout for solving the potential degradation of $f_{\max}$ and $\mathrm{NF}_{\min}$ emerges as an interesting and important topic in the future work for RF and analog applications.

Acknowledgment

The authors would like to thank the Chip Implementation Center for the device fabrication and Nano Devices Laboratory for the noise measurement.

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