Mechanisms of Interface Trap-Induced Drain Leakage Current in Off-State n-MOSFET's

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***Abstract*—An interface trap-assisted tunneling and thermionic emission model has been developed to study an increased drain leakage current in off-state n-MOSFET's after hot carrier stress. In the model, a complete band-trap-band leakage path is formed at the Si/SiO_2 interface by hole emission from interface traps to a valence band and electron emission from interface traps to a conduction band. Both hole and electron emissions are carried out via quantum tunneling or thermal excitation. In this experiment, a 0.5 μm n-MOSFET was subjected to a dc voltage stress to generate interface traps. The drain leakage current was characterized to compare with the model. Our study reveals that the interface trap-assisted two-step tunneling, hole tunneling followed by electron tunneling, holds responsible for the leakage current at a large drain-to-gate bias (V_{dg}). The lateral field plays a major role in the two-step tunneling process. The additional drain leakage current due to band-trap-band tunneling is adequately described by an analytical expression $\Delta I_d = A \exp(B_{it}/F)$. The value of B_{it} about 13 mV/cm was obtained in a stressed MOSFET, which is significantly lower than in the GIDL current attributed to direct band-to-band tunneling. As V_{dg} decreases, a thermionic-field emission mechanism, hole thermionic emission and electron tunneling, becomes a primary leakage path. At a sufficiently low V_{dg}, our model reduces to the Shockley–Read–Hall theory and thermal generation of electron-hole pairs through traps is dominant.**

I. Introduction

GATE induced drain leakage (GIDL) current which is attributed to direct band-to-band tunneling has been recognized as a major drain leakage mechanism in off-state MOSFET's [1], [2]. Recently, the effects of hot carrier stress on the GDL [3]–[7] have attracted considerable interest since they may impose a limiting factor on the scaling of a MOSFET. Hot-carrier stress effects on the GIDL are realized due to oxide trapped charge and generated interface traps. It is found that oxide charge shifts the flat-band voltage and results in an enhancement of the GIDL current [5]. In addition, generation of interface traps may introduce an additional band-trap-band leakage mechanism and lead to a significant increase in a drain leakage current.

Various characterization and modeling techniques have been proposed to study the interface trap effects. Hori characterized the additional drain leakage current by assuming a band-to-defect tunneling mechanism [6]. In his model, electrons are thermally excited from a valence band to interface traps followed by tunneling into a conduction band. The electron occupation of interface traps is assumed to be the equilibrium Fermi–Dirac distribution. This trap-assisted leakage mechanism is only appropriate under certain drain-to-gate biases (V_{dg}). For example, if V_{dg} is sufficiently large, which usually occurs in EEPROM programming, a significant band-bending results and causes the quasi-Fermi level to be much below the interface traps. Thus, thermal excitation is no longer a responsible mechanism for electron occupation in interface traps. Instead, a two-step tunneling process, hole tunneling from interface traps to a valence band (step 1) and electron tunneling from the traps to a conduction band (step 2), forms a complete and major leakage path. The concept of two-step tunneling was proposed by Fossum *et al.* to explain an anomalous leakage current via grain-boundary traps in polysilicon MOSFET's [8]. More recently, Hurkx *et al.* developed a modified recombination model which also includes both hole tunneling and electron tunneling in heavily doped grated-diodes [9]. Rigorously speaking, these models are to deal with bulk traps which are near interface, not exactly interface traps in MOSFET's. As a matter of fact, hole tunneling from interface traps to a valence band in a deep-depleted channel region is strictly restricted to the channel

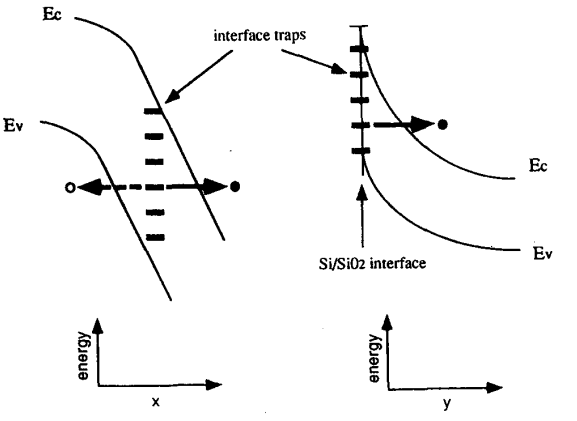

Fig. 1. Illustration of band-bending in the x-direction (along the channel) and in the y-direction (perpendicular to the channel), respectively, in the deep depleted region of a MOSFET. Note that hole tunneling (thick dashed line) occurs only in the x-direction while electron tunneling (thick solid lines) occurs in both x and y directions.

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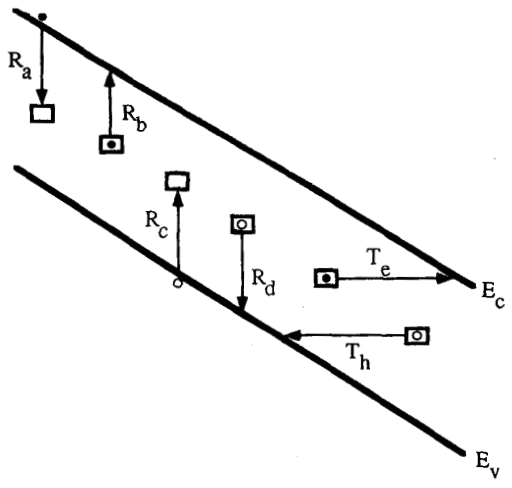

Fig. 2. Various electron and hole transition mechanisms through interface traps. R_a, R_b, R_c, R_d are thermionic emission and capture rates of electrons and holes. F_a, F_b, F_c, F_d represent electron and hole tunneling rates outward and inward.

direction. Fig. 1 shows the band diagrams in the lateral direction (x-direction) and in the vertical direction (y-direction), respectively, in the deep-depleted region of a MOSFET. The two-step tunneling mechanism through interface traps is also illustrated. Note that hole tunneling (represented by a thick dashed line) occurs only in the lateral direction. The reason is that the valence band bends upward at interface and hole tunneling in the vertical direction is not allowable from a viewpoint of energy conservation. Consequently, the hole tunneling rate is enhanced by a lateral field while electron tunneling from interface traps to a conduction band can be enhanced by both lateral and vertical fields. This feature is considerably different from bulk trap-assisted tunneling in the previous models [8], [9].

In addition to tunneling, hole and electron emissions may be carried out via thermal excitation. The thermal effect becomes especially prominent at a low V_{dg} when tunneling is relatively weak. In our model, thermal generation current described by the Shockley–Read–Hall (SRH) theory [10] is incorporated. Thus, both electron and hole transitions can be made through quantum tunneling or thermal excitation. The strength of each individual transition mechanism is evaluated under different operating conditions.

The drain leakage current in a polysilicon gate LATID n-MOSFET [11] was characterized. The gate length is 0.5 μm. The gate oxide thickness, spacer width, and channel width are 150 Å, 0.15 μm, and 50 μm, respectively. The threshold voltage adjustment was performed by 60 keV BF_2 ions with a dose of 4×10^{12} cm^{-2}. The LATID n^- dose and implant energy are 3.0×10^{13} cm^{-2} and 60 keV phosphorus with a tilt angle of 45°. The overlap between the gate and the n^- region is about 0.075 μm. The 80 keV arsenic was implanted in the source/drain at a dose of 3.0×10^{15} cm^{-2}. The device was stressed at a drain bias of 6.5 V and a gate bias of 2.5 V for 500 sec. Under the stress condition, a roughly maximum interface trap generation rate was obtained [12].

II. Drain Leakage Current Model

Various carrier transition processes are illustrated in Fig. 2. $G_e(= R_a - R_b)$ and $G_h(= R_d - R_c)$ stand for the thermionic emission rates for electrons and holes. $T_e(= F_a - F_b)$ and $T_h(= F_d - F_c)$ denote the tunneling rates for electrons and holes. From the SRH theory [10], G_e and G_h are expressed below,

$$G_e = v_{th}\sigma_n\left[n_i \exp\left(\frac{E_t - E_i}{kT}\right) f_t - n_s(1 - f_t)\right] \quad (1a)$$

$$G_h = v_{th}\sigma_p\left[n_i \exp\left(\frac{E_i - E_t}{kT}\right)(1 - f_t) - (p_s f_t)\right], \quad (1b)$$

where v_{th} is the thermal velocity, n_i is the intrinsic carrier density, f_t is the electron occupation factor of interface traps, E_i is an intrinsic Fermi level, E_t is the trap energy, σ_n and σ_p are the capture cross-sections of electrons and holes, and n_s and p_s are the electron and hole densities at the interface. The tunneling rates T_e and T_h for electrons and holes are shown below,

$$T_e = (f_t - f_c)/\tau_e \quad (2a)$$

$$T_h = ((1 - f_t) - (1 - f_v))/\tau_h, \quad (2b)$$

where τ_e and τ_h are time constants for electron tunneling and hole tunneling. f_c and $(1 - f_v)$ are electron and hole occupation factors in the conduction band and in the valence band, respectively. According to the Fermi-Golden rule, the dependence of τ_e and τ_h on electric field at trap level E_t is obtained [13].

$$\tau_e(E) = \tau_{0c} \exp\left[\frac{4}{\hbar}(2m_n)^{1/2}\frac{(E_c - E_t)^{3/2}}{3qF}\right] \quad (3)$$

$$\tau_h(E) = \tau_{0v} \exp\left[\frac{4}{\hbar}(2m_p)^{1/2}\frac{(E_t - E_v)^{3/2}}{3qF_1}\right], \quad (4)$$

where m_n and m_p are the effective masses for electrons and holes. τ_{0v} and τ_{0c} are effective transit times in the valence band and in the conduction band. In this work, a constant electric field is assumed in tunneling. It should be emphasized again that only the lateral field F_1 is involved in the expression of τ_h while a total field F is used in τ_e. For $F_1 < F$, the lateral field plays a more important role in the interface trap-assisted tunneling process. Here, we use $m_n = m_p = 0.2m_0$ [8], $\tau_{0v} = \tau_{0c} = 0.1$ ps and $\sigma_n = \sigma_p = 10^{-13}$ cm^2 [14] in the calculation.

In a steady state, the total hole emission rate is equal to the total electron emission rate for the number of trapped electrons remains constant. The following equality holds:

$$G_e + T_e = G_h + T_h. \quad (5)$$

Substituting (1) and (2) into (5), the electron occupation factor f_t is derived (see (6) shown at the bottom of next page). Once f_t is obtained, the additional drain leakage current through interface traps can be evaluated as follows:

$$\Delta I_d = qW \int_{\text{channel}} \int_{\text{bandgap}} \Delta N_{it}(x, E_t)(G_e + T_e)\, dE_t\, dx, \quad (7)$$

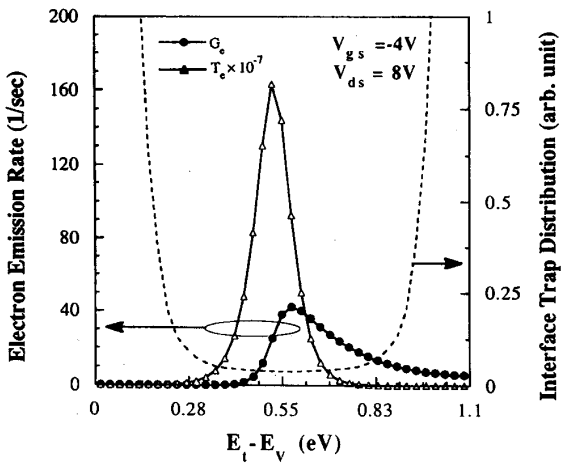

Fig. 3. Typical distributions of electron emission rates via tunneling (T_e times 1×10^{-7}) and thermal generation (G_e). The interface trap distribution in energy is from measurement [16].

where ΔN_{it} is the hot carrier stress generated interface trap distribution and W is the channel width. Previous studies have shown that ΔN_{it} has a sharp distribution in space and the full width at half-maximum (FWHM) is about 300 Å [15]. Therefore, we can approximate it by a δ-function. Moreover, G_e and T_e also exhibit narrow distributions in energy with a peak in the vicinity of the intrinsic Fermi-level E_i. Typical distributions of G_e and T_e are plotted in Fig. 3. Also plotted in the figure is the U-shape distribution of interface traps from measurement [16]. As a result, we assume a uniform distribution of ΔN_{it} near the E_i and (7) is further simplified.

$$\Delta I_d \propto \int_{\text{bandgap}} G_e(E_t, x_t)\, dE_t + \int_{\text{bandgap}} T_e(E_t, x_t)\, dE_t = (G'_e + T'_e), \tag{8}$$

where x_t is the position of the ΔN_{it} peak and G'_e and T'_e represent the integration of G_e and T_e from the valence band to the conduction band.

At a large V_{dg}, the tunneling mechanism T'_e is much faster than the thermal generation G'_e. ΔI_d in (8) is reduced to an analytical expression,

$$\Delta I_d = A \exp\left(-B_{it}(E'_t)/F\right) \tag{9}$$

with

$$B_{it} = \frac{4}{\hbar}(2m_n)^{1/2}\frac{(E_c - E'_t)^{3/2}}{3q} \tag{10a}$$

$$E'_t = \frac{E_v + (F_1/F)^{2/3}E_c}{1 + (F_1/F)^{2/3}} \tag{10b}$$

where E'_t is the energy level of interface traps which are most effective in the two-step tunneling process. Detailed derivation and explanations of (9) and (10) are given in the Appendix. It should be pointed out that if the lateral field is much greater than the vertical field, F_1 is close to F. In this condition, $E'_t = 0.5(E_c + E_v)$ is the midgap trap and the corresponding B_{it} has a minimum value of 13 MV/cm. In the other extreme, if the vertical field is much larger than the lateral field, B_{it} has a maximum value of 36 MV/cm which is the same as the direct band-to-band tunneling incurred drain leakage current [17]. A in (9) is weakly dependent on electric field and is treated as a fitting parameter in the comparison of simulation and measurement.

Various leakage paths are studied in the current model including hole tunneling followed by electron tunneling (ΔI_{tt}), hole tunneling followed by electron thermionic emission (ΔI_{tg}), hole thermionic emission followed by electron tunneling (ΔI_{gt}) and hole thermionic emission followed by electron thermionic emission (ΔI_{gg}). In this way, the total drain leakage current via interface traps can be expressed as a summation of these four components:

$$\Delta I_d = \Delta I_{gg} + \Delta I_{gt} + \Delta I_{tg} + \Delta I_{tt}. \tag{11}$$

The magnitude of each component can be immediately derived,

$$\Delta I_{gg} = \Delta I_d \cdot \left(\frac{G'_h}{G'_e + T'_e}\right) \cdot \left(\frac{G'_e}{G'_e + T'_e}\right) \tag{12a}$$

$$\Delta I_{gt} = \Delta I_d \cdot \left(\frac{G'_h}{G'_e + T'_e}\right) \cdot \left(\frac{T'_e}{G'_e + T'_e}\right) \tag{12b}$$

$$\Delta I_{tg} = \Delta I_d \cdot \left(\frac{T'_h}{G'_e + T'_e}\right) \cdot \left(\frac{G'_e}{G'_e + T'_e}\right) \tag{12c}$$

$$\Delta I_{tt} = \Delta I_d \cdot \left(\frac{T'_h}{G'_e + T'_e}\right) \cdot \left(\frac{T'_e}{G'_e + T'_e}\right). \tag{12d}$$

In the calculation, electric field and carrier densities in the measured device are obtained from a general-purpose two-dimensional device simulator, Silvaco PISCES IIB.

III. Results and Discussions

Fig. 4 shows the measured drain leakage currents before and after hot carrier stress. The increased drain leakage currents due to interface traps from measurement (solid lines) and calculation are plotted in Fig. 5. The dotted lines are obtained from (8) and the dashed lines are calculated from (9) with A equal to 2.2×10^{-7} Amp. The reader should be reminded that the two-step tunneling is a dominant leakage mechanism in the entire region of the gate bias in Fig. 5. The calculated electric field distributions along the Si/SiO_2 interface in both lateral and vertical directions are shown in Fig. 6 at $V_{ds} = 8$ V and $V_{gs} = -4$ V. The gate edge is located at $x = 0.5$ μm. The spatial distribution of interface traps is calculated from a numerical simulation [18]. The lateral field in the interface trap region is much higher than the vertical field

$$f_t = \frac{v_{th}[\sigma_n n_s + \sigma_p n_i \exp\left((E_i - E_t)/kT\right)] + \frac{f_c}{\tau_e} + \frac{f_v}{\tau_h}}{v_{th}\sigma_n(n_s) + n_i \exp\left((E_t - E_i) + v_{th}\sigma_p(p_s + n_i \exp\left((E_i - E_t)/kT\right)\right)) + \frac{1}{\tau_e} + \frac{1}{\tau_h}} \tag{6}$$

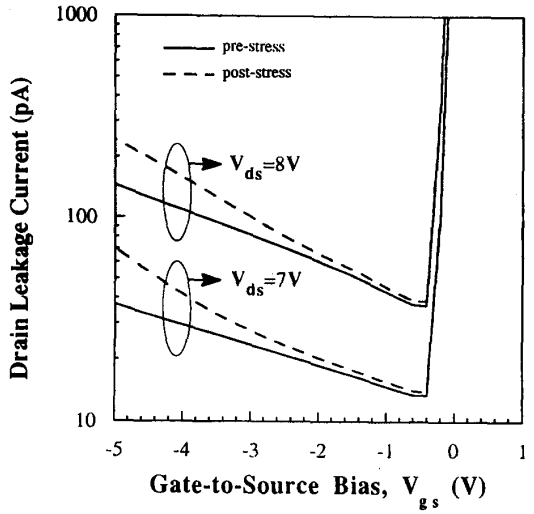

Fig. 4. Measured drain leakage current characteristics before and after hot carrier stress.

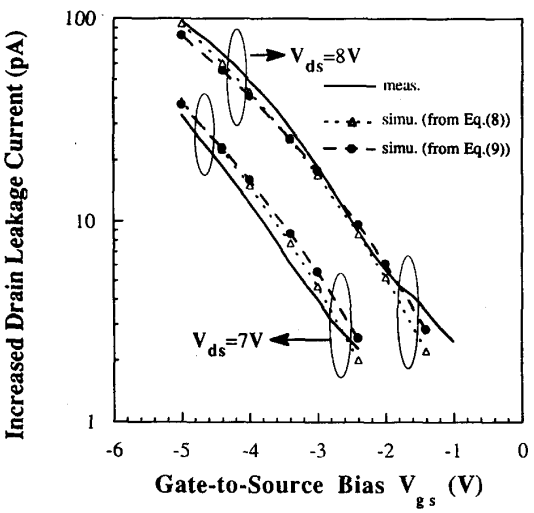

Fig. 5. Calculated and measured additional drain leakage current due to interface traps.

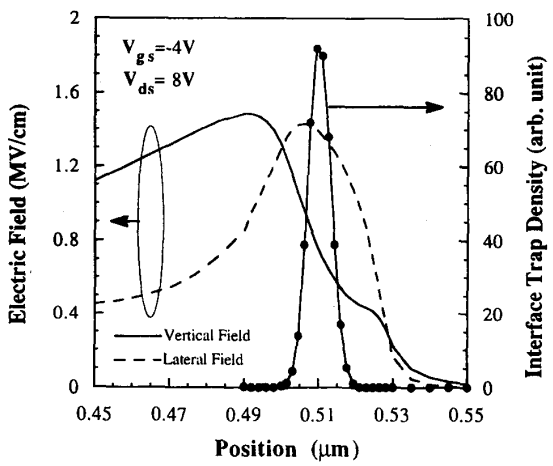

Fig. 6. Lateral and vertical field distributions along the interface at $V_{ds} = 8$ V and $V_{gs} = -4$ V. The interface trap density is also plotted.

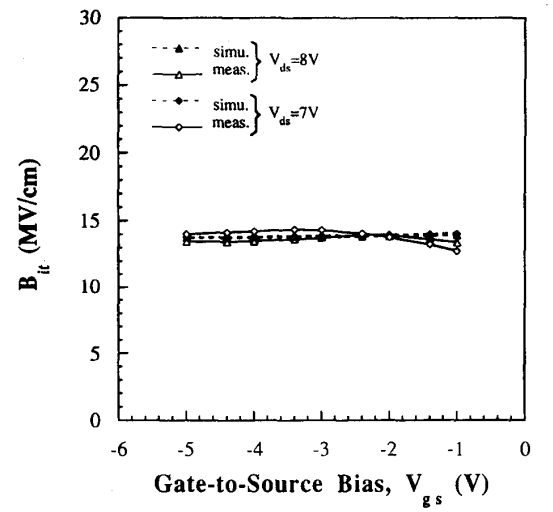

Fig. 7. Measured and calculated B_{it} versus gate bias.

in the current device structure. According to (10), E_t' is about $(E_c + E_v)/2$ and the B_{it} should be close to its minimum value. The measured and calculated B_{it} versus gate bias are shown in Fig. 7. The obtained B_{it} value about 13 MV/cm in the stressed MOSFET is significantly lower than previously reported measurement results for the GIDL current ranging from 23 MV/cm [5] to 36 MV/cm [19]. In reality, the B_{it} reflects a potential barrier height in tunneling and the minimum B_{it} obtained from the measurement is a clear evidence of midgap trap-assisted tunneling. Furthermore, we shift the ΔN_{it} along the channel in a tunneling dominant domain (high field region), where B_{it} is meaningful, to investigate the sensitivity of the B_{it} to the interface trap position in Fig. 8. The corresponding E_t' is also drawn. There exists a window in the channel in Fig. 8 in which near midgap trap-assisted tunneling is dominant. This implies that once the generated interface traps are located in the window, a theoretically lower limit of the B_{it} should be obtained.

To compare the various leakage paths, we calculate the four components of the drain leakage current at $V_{ds} = 3$ V in Fig. 9. Also indicated are the dominant regions of the two-step tunneling, the thermionic-field emission and the SRH thermal generation, respectively. The feature of the calculated current is quite consistent with the measured characteristics (Fig. 4 in [6]). Apparently, the interface trap assisted two-step tunneling (ΔI_{tt}) holds responsible for $V_{dg} > 6$ V in the current device structure. As V_{dg} decreases ($4\ V < V_{dg} < 6$ V), a thermionic-field emission (ΔI_{gt}) becomes a major leakage path. In this region, the rates of the various carrier transition processes in (1) and (2) have the following relationship $T_e \geq G_h > T_h \gg G_e$. It is interesting to note that the mechanism accounting for ΔI_{gt} is actually the same as the band-to-defect

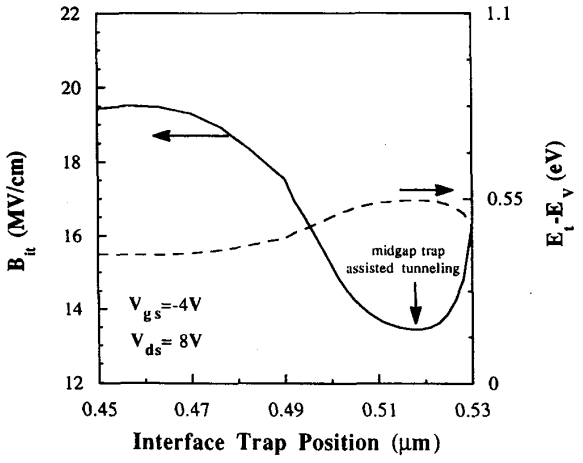

Fig. 8. The dependence of B_{it} and E_t' on the interface trap position, x_t.

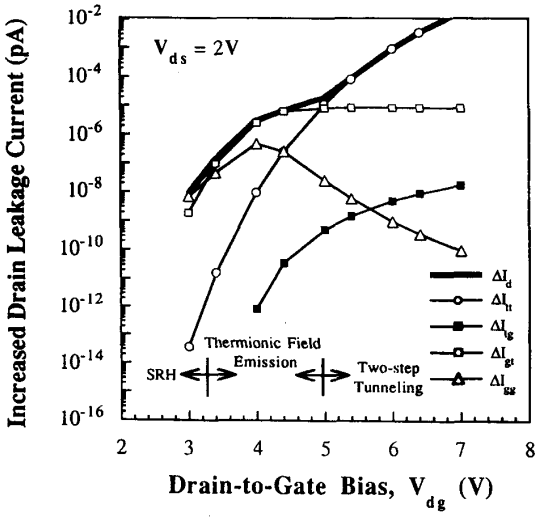

Fig. 9. Comparison of the four leakage current components at $V_{ds} = 3$ V.

model proposed by Hori [6]. At an extremely low V_{dg}, our result reduces to the SRH model and thermal generation of electron-hole pairs via traps (ΔI_{gg}) is dominant.

IV. Conclusion

In this work, we have developed an interface trap-assisted tunneling and thermionic emission model to describe the increased drain leakage current ΔI_d in a 0.5 μm LATID n-MOSFET. The difference between interface trap-assisted tunneling and bulk-assisted tunneling has been addressed. Electric field in the lateral direction is found to play a major role in the two-step tunneling process. In a band-trap-band tunneling dominant condition, the measured B_{it} of the ΔI_d in the hot carrier stressed device is about 13 MV/cm. This value is much lower than ever reported for the direct band-to-band tunneling current and agrees well with the lower limit predicted from our model. The effects of various leakage mechanisms of ΔI_d are compared under different bias conditions.

V. Appendix

At a large V_{dg}, tunneling is more pronounced than thermal excitation due to a large channel field. In other words, $1/\tau_e$ and $1/\tau_h$ are sufficiently large in comparison with other terms in (6). In addition, one can reasonably assume that f_c and $(1-f_v)$ are negligible in a deep-depleted region. Hence, we have

$$f_t = \frac{\tau_e}{\tau_e + \tau_h} \tag{13}$$

and

$$\Delta I_d \propto \int_{\text{bandgap}} \Delta N_{it}(E_t)(f_t(E_t)/\tau_e(E_t))\,dE = \int_{\text{bandgap}} \Delta N_{it}(E_t)/(\tau_h(E_t) + \tau_e(E_t))\,dE. \tag{14}$$

From (3) and (4), τ_h and τ_e vary exponentially with $E_t^{3/2}$. The integrand in (14) becomes a sharply peaking function of E_t. The peak occurs at E_t' when $\tau_h(E_t') = \tau_e(E_t')$, that is,

$$E_t' = \frac{E_v + (F_1/F)^{2/3}E_c}{1 + (F_1/F)^{2/3}}. \tag{15}$$

Since τ has a function form of $\exp(B_{it}(E_t')/F)$ in (3), (14) can be rewritten as

$$\Delta I_d \propto \Delta N_{it}(E_t')/(\tau_h(E_t') + \tau_e(E_t')) = \Delta N_{it}(E_t')/(2\tau_e(E_t')) = A\exp(-B_{it}(E_t')/F). \tag{16}$$

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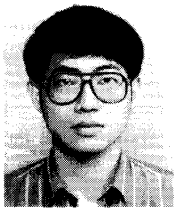

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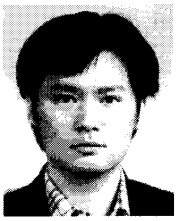

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