An Isolated Full-Bridge DC–DC Converter With 1-MHz Bidirectional Communication Channel

Ru-Shiuan Yang, *Student Member, IEEE*, Lon-Kou Chang, and Hung-Chi Chen, *Member, IEEE*

***Abstract*—This paper presents a novel isolated full-bridge dc/dc converter with bidirectional communication capability. The transformer in the proposed converter is utilized as an isolation interface for transferring both energy and data. Power delivery and forward data transfer are conducted simultaneously by modifying the full-bridge switching phase. Backward data transfer is realized by manipulating the amplitude of the resonant signal through modulating the impedance of the resonant tank at the secondary side of the transformer. Finally, the operation principle of the proposed converter was verified on a 900-mW prototype operating at 1 MHz from a 12-V dc input.**

***Index Terms*—Bidirectional communication, data transmission, full-bridge converter, isolation, LLC, resonance, transformer.**

I. Introduction

IN NUMEROUS applications, such as telephony [1]–[3], electricity usage meter [4], medical instrument [5], and industrial control system [6], isolated interfaces are required for safety and grounding. In conventional approaches, power conversion and communication function are realized with independent interface circuits. For isolated dc/dc power conversion, a transformer is applied as a power transfer device. For data communication, extra pulse transformers, optocouplers, or high-voltage capacitors are applied as data transfer interface. Some methods combine power supply and data communication in common isolation barrier, like in [7] and [8]. This paper presents a novel isolated full-bridge dc/dc converter with bidirectional communication capability. It provides a high insulation quality and a high integration design with reduced cost and device counts by using a common isolated transformer that facilitates power and data transfer.

Generally, L–C combination resonant technology is employed in power converters [9]–[21] to achieve soft switching for increasing the efficiency. In the proposed design, the resonant operation is developed to achieve "data transmission."

The operations of the proposed converter for providing bidirectional communication are as follows: 1) Power delivery and forward data transfer can be made simultaneous by altering the full-bridge switching phase. A positive or negative voltage phase across the primary winding of the transformer represents a 0 or 1 signal of forward datum, respectively. 2) The backward data transfer is attained by manipulating the amplitude of a resonant signal through modulating the impedance of the resonant tank at the secondary side of the transformer. Therefore, backward datum can be retrieved by detecting the different amplitudes of the resonant signal across the primary winding of the transformer. A low power-loss backward data transfer is achieved through the resonant operation of the transformer after the transformer is fully demagnetized. No additional supplied power is needed to transfer backward data. Via these two data transfer approaches, isolated bidirectional data communication is accomplished.

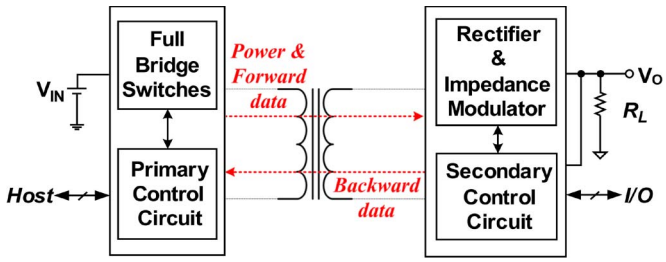

Fig. 1. Block diagram of the proposed power converter.

II. Circuit and Operation Principle

Fig. 1 shows the block diagram of the proposed isolated dc/dc converter, including the converter and data communication stages. The data communication stage includes a primary control circuit and secondary control circuit to achieve bidirectional communication. The primary control circuit is employed to transfer forward data from the *Host* side to the *I/O* side through the transformer and simultaneously transfer power to the load in the *I/O* side. The secondary control circuit is utilized to transfer backward data from the *I/O* side to the *Host* side through the transformer. Additionally, the primary and secondary control circuits are also used for receiving the data transmitted from the opposite sides.

Fig. 2 shows the power conversion stage of the proposed power converter which includes four circuit blocks: 1) an isolated transformer that transfers power and data; 2) a full-bridge switching stage, including transistors Q_1, Q_2, Q_3, and Q_4, that generates a switching signal according to the forward datum TX_1; 3) rectifier diodes D_5, D_6, D_7, D_8 and an output capacitor C_O that provides a supply voltage to the load and the secondary control circuit; and 4) an impedance modulator,

Manuscript received April 7, 2010; revised August 11, 2010; accepted October 6, 2010. Date of publication November 29, 2010; date of current version August 12, 2011. This work was supported by the National Science Council of Taiwan under Contract NSC 96-2221-E-009-239-MY3: "An Isolated Full-Bridge DC/DC Converter with Bidirectional Communication Capability."

R.-S. Yang and H.-C. Chen are with the Department of Electrical Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan (e-mail: rushiuan.ece92g@nctu.edu.tw; lkchang@mail.nctu.edu.tw; hcchen@cn.nctu.edu.tw).

L.-K. Chang is with Macroblock, Inc., Hsinchu 30072, Taiwan.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2010.2095397

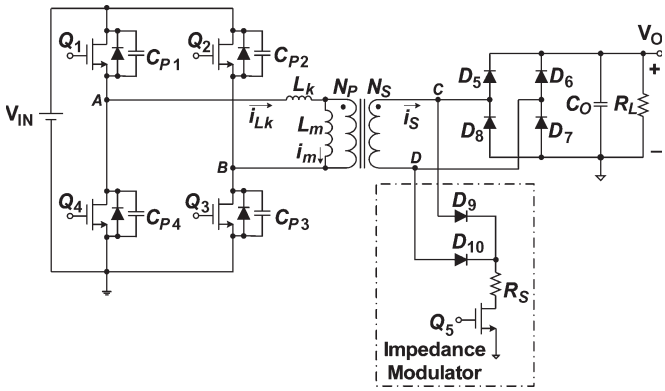

Fig. 2. Proposed dc/dc converter including the impedance modulator.

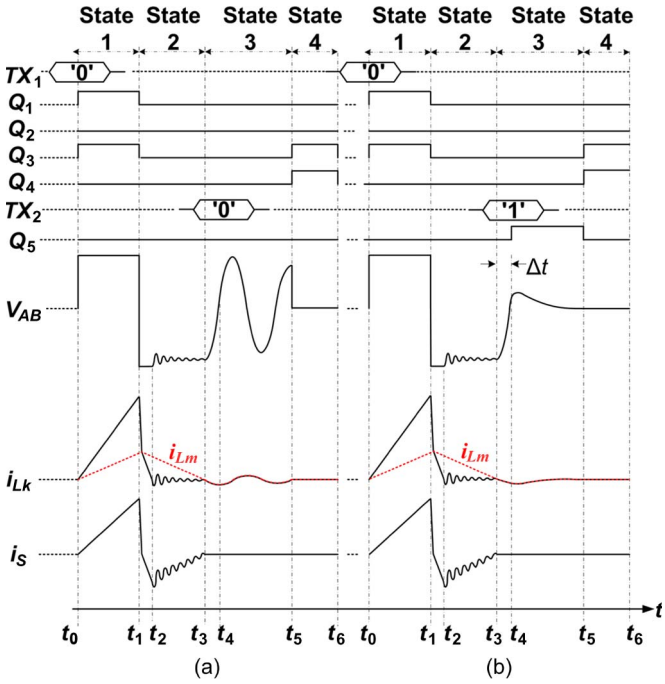

Fig. 3. Key waveforms of the proposed converter.

including diodes D_9 and D_{10} and transistor Q_5, that controls the impedance of the transformer according to the backward datum TX_2.

Fig. 3 shows four operational states (States 1–4) in a switching cycle T_S during bidirectional communication. Table I shows the control table of the on-transistors related to the transmitted forward datum TX_1 and backward datum TX_2 in each operation state.

A. State 1 $[t_0-t_1]$: Duration of Power and Forward Data Transfer

In this state, power is transferred from the input dc bus ($V_{\rm IN}$) to the load through the full-bridge stage and rectifier diodes. According to the transistor switching control shown in Table I, the voltage polarity of the full-bridge converter's output $V_{\rm AB}$ is manipulated by the logic state of forward datum TX_1. Through the voltage polarity control, power and forward datum TX_1 can be transferred simultaneously to the secondary side through the isolated transformer. After rectification, the coupled voltage

TABLE I
CONTROL TABLE OF THE ON-TRANSISTORS RELATED TO THE TRANSMITTED DATUM

Datum \ State	State 1	State 2	State 3	State 4
$TX_1 = 0$	Q_1, Q_3			Q_3, Q_4
$TX_1 = 1$	Q_2, Q_4			Q_3, Q_4
$TX_2 = 0$				
$TX_2 = 1$			Q_5	

$V_{\rm CD}$ across the transformer secondary winding generates the dc output voltage (V_O). Meanwhile, the transferred forward datum is retrieved simply by a level-detect circuit in the transformer secondary side.

When transmitted forward datum TX_1 is 0, transistors Q_1 and Q_3 are turned on, resulting in $V_{\rm AB} = V_{\rm IN}$; otherwise, $V_{\rm AB} = -V_{\rm IN}$ for the case of $TX_1 = 1$. When $V_{\rm AB} = V_{\rm IN}$, rectifier diodes D_5 and D_7 are turned on. The current of the secondary winding $i_{L_s}(t) = n^*(i_{L_k}(t) - i_{L_m}(t))$, where n is the turn ratio of the transformer, i.e., $n = N_P/N_S$. The increasing rate of the magnetizing current of the transformer is given by

$$\frac{di_{L_m}(t)}{dt} = \frac{n(V_O + 2V_D)}{L_m} \tag{1}$$

where V_O is the average output voltage and V_D is the forward conduction voltage of the rectifier diode.

Since the leakage inductance L_k is much smaller than the magnetizing inductance L_m of the transformer, the voltage across the leakage inductance is low, such that $V_{L_k} \ll V_{L_m}$. The voltage on the magnetizing inductance is approximately equal to input voltage, i.e., $V_{\rm IN} \approx n(V_O + 2V_D)$. Assuming that the condition $\Delta V_{L_k} \ll V_{L_k}$ is satisfied, the voltage across the leakage inductor V_{L_k} can be seen as a constant. Therefore, the switching current of the leakage inductance i_{L_k} in State 1 increases linearly. It can be expressed as

$$i_{L_k}(t)\Big|_{t_0}^{t_1} = \frac{V_{\rm IN} - n(V_O + 2V_D)}{L_k} \times t. \tag{2}$$

B. State 2 $[t_1-t_3]$: Duration of Transformer Demagnetization

The case of $TX_1 = 0$ is assumed for illustrating the circuit operation. If the current through an inductor is forced to change rapidly, a very high voltage will be induced to resist the current change. When $t = t_1$, all of the full-bridge transistors are turned off, a very high negative voltage is induced across the leakage inductor, and it forces the body diodes of transistors Q_2 and Q_4 to turn on. The leakage inductor is demagnetized rapidly until i_{L_k} decreases to $i_{L_m}(t_1)$, i.e.,

$$i_{L_m}(t_1) = i_{L_m}(t_0) + \frac{n(V_O + 2V_D)D_{r1}T_S}{L_m} \tag{3}$$

where D_{r1-4}'s denote the duty ratios of States 1–4. While $i_{L_k} < i_{L_m}$, the leakage inductor demagnetized through the

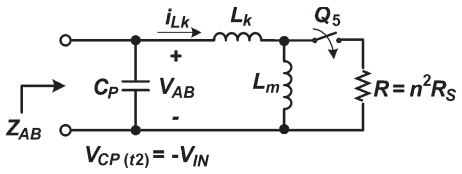

Fig. 4. Equivalent circuit of the proposed converter in State 3.

body diodes of transistors Q_2 and Q_4 until it is fully demagnetized. The switching current of the leakage inductance i_{L_k} in State 2 decreases linearly as the same rate of (2).

In this state, while $i_{L_k} > i_{L_m}$, both the currents i_{L_k} and i_{L_m} flow to the transformer in phase. They will induce an output current i_S to load through the rectifiers. Since L_m is reversely biased, L_m will demagnetize just as shown in (1). While i_{L_k} decays to a value, i.e., $i_{L_k} < i_{L_m}$, some of the energy of the magnetizing inductance L_m will be pumped to the input dc bus, $V_{\rm IN}$, through the leakage inductance L_k. After the leakage inductor is fully demagnetized, i_{L_k} decays to zero, and the body diodes of transistors Q_2 and Q_4 are turned off. Thus, the energy stored in the magnetizing inductance L_m of the transformer will wholly flow to the output V_O through the secondary winding of the transformer and the rectifier diodes D_6 and D_8. The reflected voltage of the primary inductance V_{L_m} is $-n(V_O + 2V_D)$. The magnetizing inductor L_m demagnetizes as the same rate of (1). In contrast, V_{L_m} will be $n(V_O + 2V_D)$ if $TX_1 = 1$, in which the transistors Q_2 and Q_4 switch the transformer.

In this design, the magnetizing current i_{L_m} is in discontinuous conduction mode. The magnetizing inductance L_m is charged in State 1 and then discharged completely in State 2. The voltage across the magnetizing inductor in States 1 and 2 is $|n(V_O + 2V_D)|$. Thus, $\Delta t_{\rm mag} = \Delta t_{\rm dmag}$, where $\Delta t_{\rm mag}$ is the magnetizing period of L_m, i.e., $\Delta t_{\rm mag} = D_{r1}T_S$, and $\Delta t_{\rm dmag}$ is the demagnetizing period of L_m.

At $t = t_2$, the time when $i_{L_k}(t_2)$ decays to zero, the body diodes of transistors Q_2 and Q_4 will not conduct. The leakage inductor L_k starts to resonate along with the equivalent parasitic capacitors C_P. In practice, the resonant amplitude in State 2 decays due to the parasitic resistance along the resonant path. The initial value of V_{L_k} is very small in the beginning of oscillation time. That is why the oscillation amplitude is very small in State 2. The equivalent parasitic capacitor C_P across the terminals A and B includes the following: 1) the parasitic capacitors of the transistors, such as $C_{P1}-C_{P4}$; 2) the parasitic capacitors of the primary winding of the transformer; and 3) the parasitic capacitors between the conduction wires on the printed circuit board.

C. State 3 $[t_3-t_5]$: Duration of L–L–C Resonance and Backward Data Transfer

Fig. 4 shows the equivalent circuit of the proposed converter in State 3. In this state, the resonant quality factor (Q factor) is determined by the ON/OFF state of the transistor Q_5. When $TX_2 = 1$, transistor Q_5 is turned on, and resistor R_S is connected to terminals C and D. The resistor R_S changes the impedance across terminals A and B and results in a low quality factor and high oscillation damping (Fig. 3). Conversely, when $TX_2 = 0$, transistor Q_5 is off at t_4; thus, an approximate infinite Q factor will be obtained, and $V_{\rm AB}$ will have a large oscillation amplitude that is approximate to $V_{\rm IN}$. By detecting the oscillation amplitude of $V_{\rm AB}$, backward datum can be retrieved. Moreover, no extra supplied power is required to transfer backward data.

At $t = t_3$, the transistor Q_5 is off. The magnetizing inductor L_m is demagnetized completely. The rectifier diodes at the secondary side of the transformer are off. At this moment, since the energy stored in the parasitic capacitance C_P starts to transfer to the magnetizing inductance L_m and L_k, a resonant cycle is activated by the resonant tank $L_k-L_m-C_P$. Thus, the resonant frequency can be obtained as

$$\omega_{r1} = \frac{1}{\sqrt{C_p(L_m + L_k)}} \tag{4}$$

where the conduction and core losses of the transformer and the turn-on resistance of the MOSFETs are ignored. Since i_{L_k} and i_{L_m} are 0 at t_3 and transistor Q_5 remains off, the amplitude of the resonant signal $V_{\rm AB}$ in State 3 will be equal to $|V_{\rm AB}(t_3)|$.

As $V_{\rm IN}$ and V_O are the assigned values, t_3 can be estimated or detected by using a current sensor in the secondary side. For assuring obtaining complete demagnetization of the transformer, a short time delay Δt is inserted before activating transistor Q_5 to send the backward datum. At $t = t_4 = t_3 + \Delta t$, transistor Q_5 is turned on/off according to the logic state of transmitted backward datum TX_2 to ensure that the transformer is fully demagnetized. Furthermore, for ensuring that the amplitude of resonant signal is well modulated, Q_5 is better to be turned on before one-fourth resonant cycle when $V_{\rm CD}$ changed its polarity.

D. State 4 $[t_5-t_6]$: Duration of Synchronization

In this state, Q_3 and Q_4 are both on, and voltages across the primary and secondary windings of the transformer will remain 0 until time t_6 which is the end of a switching cycle T_S. At $t = t_6$, $V_{\rm AB}$ has an abrupt edge at the end of State 4, and the operation will return to State 1. This abrupt edge is used to generate the synchronization pulse signal (PLS) in the secondary control circuit shown in Fig. 6.

Fig. 5 shows a feasible primary control circuit of the proposed power converter. The primary control circuit has five circuit blocks: 1) a clock generator that provides a clock signal CK_1 for the primary control circuit; 2) a communication unit and a serial bus interface for receiving/transferring data from/to the *Host* side; 3) a state controller that generates signals $S_{11,12,13, \text{ and } 14}$'s to control operation timing of the proposed converter; 4) a phase-modulation circuit that controls the full-bridge switching phase and transmits the forward datum TX_1; and 5) a threshold-level detector that retrieves the backward datum into RX_2 by detecting the voltage level of the primary winding voltage $|V_{\rm AB}|$ in State 3.

Fig. 6 shows a feasible secondary control circuit for the proposed power converter. It includes the following five blocks: 1) a communication unit and serial bus interface that receives/transfers data from/to the *I/O* side; 2) a regulator that

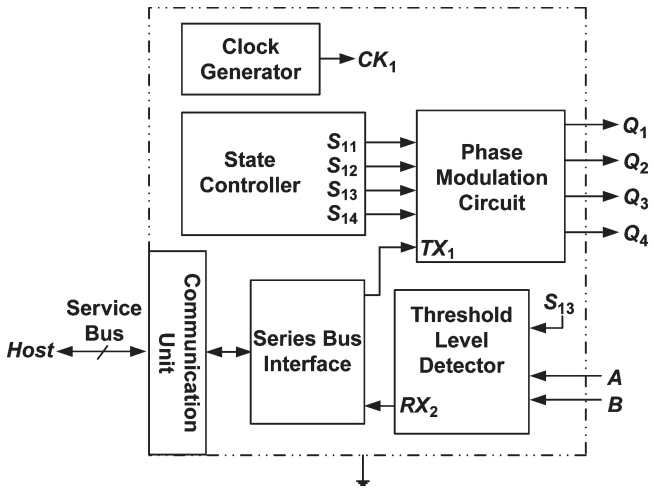

Fig. 5. Primary control circuit.

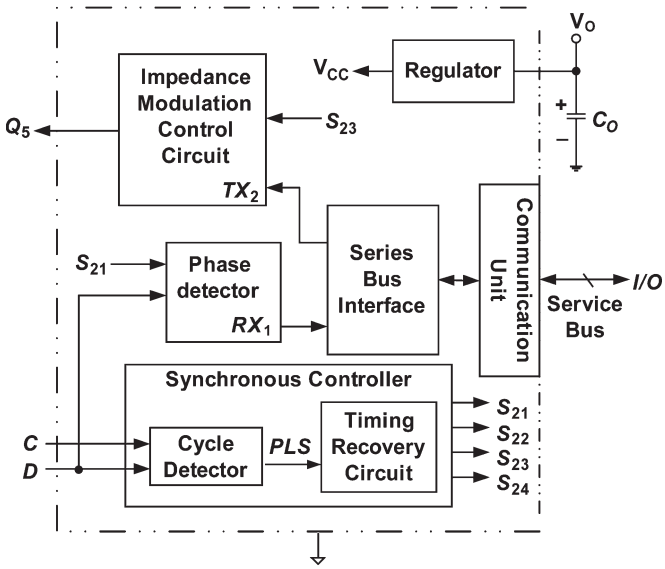

Fig. 6. Secondary control circuit.

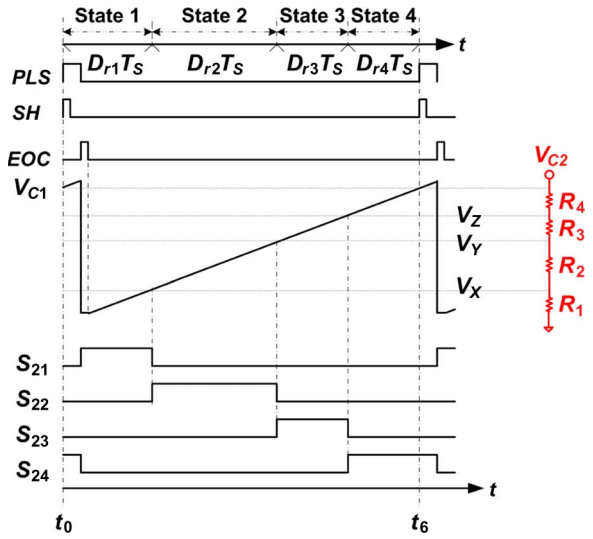

Fig. 7. Associated waveforms of the synchronous controller.

provides a regulated dc voltage to the circuit on the transformer secondary side; 3) a synchronous controller that generates synchronous state signals $S_{21,22,23,\text{ and }24}$'s to synchronize the operation timing between the primary and secondary control circuits; 4) an impedance modulator that transfers the backward datum TX_2; and 5) a phase detector that retrieves the forward datum into RX_1 by detecting the voltage of terminal D on the transformer secondary winding in State 1. When V_D exceeds the reference voltage V_{REF}, then RX_1 is set to 1; otherwise, RX_1 is set to 0.

Proper timing control is important to successfully retrieve the forward data sent from the primary control circuit. Fig. 7 shows the waveforms produced by the timing recovery circuit in the secondary control circuit. The timing recovery circuit in Fig. 6 is utilized to generate the synchronous state signals S_{21-24}'s at the secondary side of the transformer to emulate the timing signals S_{11-14}'s. When State 4 ends, a new switching cycle will start, and the voltage V_{AB} across the primary winding of the transformer will have an abrupt edge. This abrupt edge is used for the synchronization at the transformer secondary side. It causes an edge change to V_{CD}. Through detecting this edge change, the synchronization pulse signal PLS is generated by a cycle detector in the secondary control circuit. This pulse signal PLS is used for performing the synchronization. By sensing the positive and negative edges of the PLS, the timing recovery circuit will generate a sample-and-hold (SH) signal and an end-of-cycle (EOC) signal. Conventionally, the timing recovery circuit can be implemented by using a constant current to charge a capacitor C_1. The EOC signal is coupled to discharge the capacitor C_1, therefore initiating a new switching cycle as shown in Fig. 7.

The duty ratios of the four operational states $D_{r1,2,3,\text{ and }4}$'s, as shown in Fig. 7, are designed as constants by a voltage divider connected to a signal V_{C2}. Signal V_{C2} is the maximum value of V_{C1}, the voltage across the capacitor C_1, sampled by SH. The signal V_{C2} is sampled before the signal V_{C1} is discharged. The duty ratios can be regenerated at the secondary side of the transformer, which is based on the relationship $R_1 : R_2 : R_3 : R_4 = D_{r1} : D_{r2} : D_{r3} : D_{r4}$. Therefore, synchronous state signals $S_{21,22,23,\text{ and }24}$'s of the secondary control circuit can be easily produced by comparing V_{C1} and V_{C2}.

III. Design Considerations

The component parameters of the equivalent circuit in Fig. 4, namely, L_k, L_m, C_P, and R, must be selected carefully to maximize the performance and ensure a reliable backward data transfer. Once the equivalent parasitic capacitor C_P and leakage inductance of transformer L_k are measured, the magnetizing inductance L_m and resistance of the impedance modulator R_S can be derived.

The two cases of the proposed converter operated in State 3 (Fig. 4), according to the logic state of transmitted backward datum TX_2, are discussed as follows.

A. Case 1 (Q_5 OFF)

The Q factor of a resonant circuit is defined as the ratio of maximum stored energy to energy loss per cycle and is further

equivalent to

$$Q = \omega_r \left(\frac{\text{maximum energy stored}}{\text{average power dissipated}} \right). \tag{5}$$

In Case 1, when the transmitted backward data $TX_2 = 0$, Q_5 is turned off. C_P, L_k, and L_m form as an $L - L - C$ resonant tank with resonant frequency $\omega_{r1} = 1/(2\pi\sqrt{(C_p(L_m + L_k)})$. As no resistive element exists in the resonant circuit, the Q factor in Case 1 is infinite. Restated, the amplitude of resonant signal $V_{\rm AB}$ will not decay during the switching cycle period. To ensure that the backward data can be correctly retrieved by the threshold-level detector of the primary control circuit, at least one-half resonant cycle should exist in the duration of State 3. Accordingly, minimum magnetizing inductance L_m can be obtained from

$$D_{r3}T_S > \pi\sqrt{C_p(L_m + L_k)}. \tag{6}$$

B. Case 2 (Q_5 ON)

In Case 2, when the transmitted backward data $TX_2 = 1$, Q_5 is turned on. Resistance R is paralleled to magnetizing inductance L_m, where $R = n^2R_S$. Thus, the resonant frequency and the Q factor of the resonant circuit change. Since the imaginary part of resonant circuit impedance $\mathrm{Im}(Z_{\rm AB})$ is zero at resonance, the resonant frequency in Case 2 can be obtained by

$$\omega_{r2} = \sqrt{\frac{-m + \sqrt{m^2 - 4n}}{2}} \tag{7}$$

where

$$m = \frac{C_pR^2(L_m + L_k)^2 - L_m^2L_k}{C_pL_m^2L_k^2} \quad n = -\frac{R^2(L_m + L_k)}{C_pL_m^2L_k^2}.$$

As a result, the quality factor of the resonant circuit in Case 2, $Q_{\rm CASE2}$, can be obtained from (5) and (7), given as

$$\begin{aligned} Q_{\rm CASE2} &= \omega_{r2}C_p\mathrm{Re}(Z_{\rm AB}) \\ &= \frac{\omega_{r2}^3L_m^2RC_p}{\left[\omega_{r2}^2C_pR(L_m + L_k) - R\right]^2 + \omega_{r2}^2L_m^2\left(\omega_{r2}^2C_pL_k - 1\right)^2}. \end{aligned} \tag{8}$$

There are three possible resonant models in Case 2 according to R value: 1) L–L–C model, in case R approximates to ∞; 2) L–C model, in case R approximates to 0; and 3) L–L–C–R model. As shown in (8), $Q_{\rm CASE2}$ will be ∞ when resistance R is ∞. This result is the same as that in Case 1 since the resonant circuit is the same. Moreover, when setting R value as 0, the resonant tank contains only C_P and L_k, and $Q_{\rm CASE2}$ will be ∞. Thus, $Q_{\rm CASE2}$ has a valley point $(Q_{\rm CASE2,opt}, R_{\rm opt})$ in response to the change of resistance R, which is shown in Fig. 8(b).

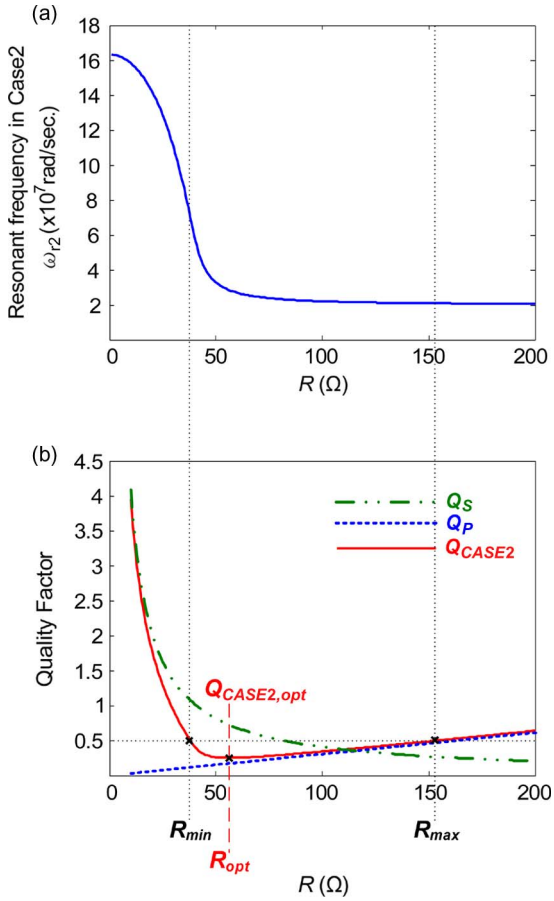

Fig. 8 (a) R versus ω_{r2}. (b) R versus *quality factor*.

To choose an appropriate resistance R value is important for a reliable backward data transfer. When R is connected across the secondary winding of the transformer in State 3, the resonant voltage has a decay function $e^{-\omega t}$, where $\alpha = \omega_r/(2Q)$. When the resonant circuit is operated at a critical damped condition such that $Q = 0.5$, then $e^{-\alpha t}$ will be as small as 0.04 at time $t = \pi/\omega_r$. Therefore, for the design satisfying $Q_{\rm CASE2} < 0.5$, the overdamped condition will ensure that the backward data can be retrieved correctly by the threshold-level detector in the primary control circuit. Similarly, $Q < 0.5$ will generate a good data retrieval capability in Case 2.

An example is given hereinafter. Assume that $C_P = 150$ pF, $L_k = 0.25$ uH, and $L_m = 16$ uH. The curves of $\omega_{r2}(R)$ and $Q_{\rm CASE2}(R)$ with respect to resistance R can be obtained from (7) and (8) and are shown in Fig. 8(a) and (b). It results in a minimum resistance ($R_{\rm min} = 38\ \Omega$) and a maximum resistance ($R_{\rm max} = 153\ \Omega$) to satisfy $Q_{\rm CASE2} = 0.5$. An appropriate value of R is acquired to provide a reliable backward data transfer. For the design optimization, a minimal Q value, $Q_{\rm CASE2,opt}$, is helpful for resonant signal $V_{\rm AB}$ decaying rapidly. The corresponding R value is $R_{\rm opt} = 56\ \Omega$.

Another reliable backward data transfer can also be achieved when the resonant circuit in Case 2 meets the following approximations: 1) If $X_{L_k} \ll |R//jX_{L_m}|$, then the resonant

circuit in Case 2 can be approximated to a second-order parallel $R{-}L_m{-}C_P$ resonant circuit with quality factor $Q_P = (\sqrt{(C_P/L_m)}) * R$, or 2) if $X_{L_m} \gg R$, then the resonant circuit in Case 2 can be approximated to a second-order series $R{-}L_k{-}C_P$ resonant circuit with quality factor $Q_S = (\sqrt{(L_k/C_P)})/R$. This approximation provides a convenient consideration by choosing an R value that is close to $Q_P < 0.5$ or $Q_S < 0.5$. Fig. 8(b) shows the curves for the three types of quality factors with respect to resistance R.

IV. Experimental Results

An experimental prototype has been built to verify the operation principles of the proposed design. The specifications of the prototype are as follows.

1) $V_{\rm IN}$: 12 V.
2) I_O: 0–90 mA.
3) V_O: 10 V (full load) to 12 V (no load).
4) f_S: 1 MHz.
5) $D_{r1} : D_{r2} : D_{r3} : D_{r4} = 9 : 9 : 9 : 5$.

The power conversion stage shown in Fig. 2 consists of the following components.

1) Q_1, Q_2, Q_3, Q_4, Q_5: VN0606 N-channel MOSFETs.
2) High- and low-side drivers for the full-bridge: IR2110.
3) $D_5, D_6, D_7, D_8, D_9, D_{10}$: SB160 diodes.
4) C_O: 1-μF ceramic capacitor.
5) Transformer: $n = N_P/N_S = 1$, $L_m = 15.9$ μH, $L_k = 0.25$ μH, MPP Core, the outer diameter is 13 mm, and the thickness is 5 mm.

First, we choose $L_m = 15.9$ uH. The measurement shows that the resonant period of $V_{\rm AB}$ is 312 ns in State 3. Therefore, the equivalent parasitic capacitor of the switches across the terminals A and B can be estimated as $C_P = 152.68$ pF, and the resonant frequency satisfies the requirement given by (6). Finally, by finding $Q_{\rm CASE2,opt} = 0.25$, the resistance of the impedance modulator $R_S = R/n^2 = 56\ \Omega$ was chosen to achieve an optimized backward data transfer.

Since the transformer is operated at Discontinuous Conduction Mode (DCM), there is no magnetic saturation concern for the transformer. The average output voltage V_O is 10.18 V at the full-load output current of 91.9 mA, and the maximum output voltage is 12 V at no-load condition. The efficiency η of the proposed converter not including the control circuit is 83% at full load in the conditions $TX_1 = 0$ and $TX_2 = 0$ during 5-min operation (Q_5 is always turned off). The efficiency η is 82% at full load for the conditions $TX_1 = 0$ and $TX_2 = 1$ (Q_5 is always turned on). As a result, it shows that the backward data transfer is a low-power-consumption approach.

Fig. 9 shows the experimental results of the proposed converter in four possible data-transmission cases. Fig. 9 also shows the gate signals of transistors Q_1, Q_5 and the voltage across the transformer primary winding ($V_{\rm AB}$). For forward data transmission, the voltage phase of $V_{\rm AB}$ presents the forward datum TX_1 transmitted in State 1. For backward data transmission, the amplitudes of the resonant signal as mentioned in State 3 have also been successfully modulated by the backward datum TX_2 and can be clearly identified by a threshold level as expected. Finally, all the waveforms have well matched the theoretical ones.

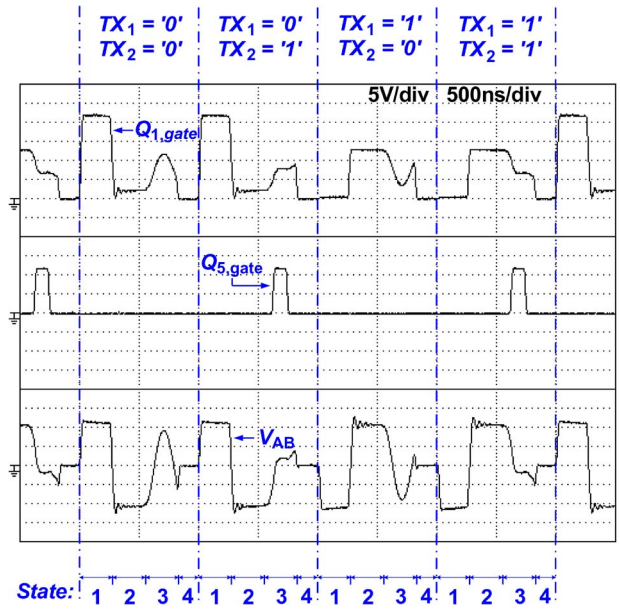

Fig. 9. Experimental waveforms for the proposed design.

V. Conclusion

The isolated full-bridge dc/dc converter with bidirectional communication capability has been presented with illustrations of its operations and analyses. A novel backward data transfer circuit, which is achieved by manipulating the amplitude of the resonant signal, is presented. An efficient approach for finding an appropriate range of modulation resistance to achieve reliable backward data communication is also presented. The experimental results have demonstrated that the proposed converter provides isolated power conversion and bidirectional communication via the same switching cycle. In conclusion, the proposed power converter provides high isolation capability by using an isolated transformer and has a small device footprint.

References

[1] W. C. D'Angelo and J. F. Latu, "Digital isolation barrier as interface bus for modems," U.S. Patent 7 330 544, Feb. 12, 2008.
[2] D. Liu, "Electrical isolation techniques for DSL modem," U.S. Patent 7 269 210, Sep. 11, 2007.
[3] E. R. Worley, "Design of telephone line interface circuits using a two chip opto-coupler with LEDs integrated onto silicon chips," U.S. Patent no. 6 757 381, Jun. 29, 2004.
[4] B. A. Smith, K. Tang, V. Levi, and J. Owens, "High voltage isolation by capacitive coupling," U.S. Patent 7 675 444, Mar. 9, 2010.
[5] D. J. Haupert, C. R. Levan, T. J. Winkler, and J. M. Kruse, "Interface devices for instruments in communication with implantable medical devices," U.S. Patent 6 580 948, Jun. 17, 2003.
[6] J. G. Calvin, "Control system methods and apparatus for inductive communication across an isolation barrier," U.S. Patent 7 684 475, Mar. 23, 2010.
[7] T. J. Dupuis, G. T. Tuttle, J. W. Scott, N. S. Sooch, and D. R. Welland, "Digital access arrangement circuitry and method for connecting to phone lines having a DC holding circuit with programmable current limiting," U.S. Patent 7 515 672, Apr. 7, 2009.
[8] R. Hershbarger and K. Fukahori, "Method and apparatus for synchronization of data in a transformer circuit," U.S. Patent 7 408 996, Aug. 5, 2008.

[9] X. Jin, W. Wu, X. Sun, and J. Liu, "Resonant tank and transformer design in series resonant converter," in *Conf. Rec. IEEE IAS Annu. Meeting*, 2005, pp. 1475–1482.
[10] L. H. S. C. Barreto, E. A. A. Coelho, V. J. Farias, J. C. de Oliveira, L. C. de Freitas, and J. B. Vieira, Jr., "A quasi-resonant quadratic boost converter using a single resonant network," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 552–557, Apr. 2005.
[11] A. Bucher, T. Durbaum, D. Kubrich, and A. Stadler, "Comparison of different design methods for the parallel resonant converter," in *Proc. EPE-PEMC*, 2006, pp. 810–815.
[12] S. Zheng and D. Czarkowski, "Modeling and digital control of a phase-controlled series-parallel resonant converter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 707–715, Apr. 2007.
[13] C. Adragna, S. De Simone, and C. Spini, "A design methodology for LLC resonant converters based on inspection of resonant tank currents," in *Proc. IEEE APEC*, 2008, pp. 1361–1367.
[14] H. Sheng, Y. Pei, and F. Wang, "Impact of resonant tank structures on transformer size for a high power density isolated resonant converter," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 2975–2981.
[15] J. Biela, U. Badstuebner, and J. W. Kolar, "Impact of power density maximization on efficiency of dc–dc converter systems," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 288–300, Jan. 2009.
[16] C. S. Tang, Y. Sun, Y. G. Su, S. K. Nguang, and A. P. Hu, "Determining multiple steady-state ZCS operating points of a switch-mode contactless power transfer system," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 416–425, Feb. 2009.
[17] J. L. Sosa, M. Castilla, J. Miret, L. Garcia de Vicuna, and J. Matas, "Modeling and performance analysis of the dc/dc series–parallel resonant converter operating with discrete self-sustained phase-shift modulation technique," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 697–705, Mar. 2009.
[18] J. M. Kwon, W. Y. Choi, and B. H. Kwon, "Single-switch quasi-resonant converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1158–1163, Apr. 2009.
[19] M. Borage, K. V. Nagesh, M. S. Bhatia, and S. Tiwari, "Design of LCL-T resonant converter including the effect of transformer winding capacitance," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1420–1427, May 2009.
[20] E. H. Kim and B. H. Kwon, "Zero-voltage and zero-current switching full-bridge converter with secondary resonance," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1017–1025, Mar. 2010.
[21] R. Casanueva, C. Brañas, F. J. Azcondo, and F. J. Díaz, "Teaching resonant converters: Properties and applications for variable loads," *IEEE Trans. Ind. Electron.*, vol. 57, no. 10, pp. 3355–3363, Oct. 2010.

Ru-Shiuan Yang (S'07) was born in Taoyuan, Taiwan, in 1981. She received the Associate's degree in electronic engineering from the National Taipei Institute of Technology, Taipei, Taiwan, in 2001 and the B.S. degree in electronic engineering from the National Yunlin University of Science and Technology, Yunlin, Taiwan, in 2003. She is currently working toward the Ph.D. degree in the Institute of Electrical and Control Engineering, National Chiao-Tung University, Hsinchu, Taiwan.

Her research interests include energy conversion, power management, and industrial electronics application.

Lon-Kou Chang received the B.S. degree in electronic engineering from Chung Yuan Christian University, Chung-Li, Taiwan, in 1975, the M.S. degree in electronic engineering from the National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 1977, and the Ph.D. degree in electrical engineering from the University of Maryland, College Park, in 1995.

In 1983, he was with the Department of Control Engineering, NCTU. In 2008, he retired from the NCTU as an Associate Professor. He is currently with Macroblock, Inc., as a Consultant in power IC design.

Hung-Chi Chen (M'06) was born in Taichung, Taiwan, in June 1974. He received the B.S. and Ph.D. degrees from the Department of Electrical Engineering, National Tsing-Hua University, Hsinchu, Taiwan, in 1996 and 2001, respectively.

In October 2001, he was a Researcher with the Energy and Resources Laboratory, Industrial Technology Research Institute, Hsinchu. Since August 2006, he has been with the Department of Electrical Engineering, National Chiao-Tung University, Hsinchu, where he is currently an Associate Professor. His research interests include power electronics, power factor correction, motor and inverter-fed control, and DSP/MCU/FPGA-based implementation of digital control.