Fabrication and characterization of gated Si field emitter arrays with gate aperture below 0.5 μm

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ABSTRACT

High aspect-ratio single-crystal silicon microtips have been fabricated using the semi-anisotropic dry etching technique. After the further oxidation sharpening process, arrays of 50×50 uniform sharp emitter tips has been achieved. The 200 Å-thick Cr metal was also coated on the surface of Si microtips to improve the performance. Furthermore, a modified self-aligned process of the gated field emitter arrays (GFETs) has been successfully developed to reduce the fabrication complexity. Employing this method, the tip radius of Si microemitter is about 200 Å, and the gate aperture can be easily reduced to about 0.3 μm. It will largely decrease the turn-on voltage of the field emission devices.

Keywords: oxidation sharpening, microtips, gated field emitter arrays, silicon pedestal, gate aperture, field emission

1. INTRODUCTION

Micrometer-scale vacuum electronics constructed by solid-state fabrication techniques is attracting increasing interest. Potential applications include flat panel displays[1], ultrahigh-frequency power sources and amplifiers[2], high-speed logic and signal processing circuits, and microsensors[3]. Vacuum microelectronic devices, in fact, have potentially number of remarkable advantages with respect to the presently much more popular "solid state" counterparts: such as carrier transport velocity, temperature insensitivity, and radiation hardness. The most fundamental element of field emission device is a sharp tip used as cold cathode. In our study, the reactive ion etching techniques combined with oxidation-sharpening[4] have been used to form arrays of uniformly sharp cones on a silicon substrate. The shape of cones are adjustable depended on the etching process. After the sharp emitter is formed, a new self-aligned process having more economy steps and flexible has been developed to locate the extraction gate apertures on the vicinity of the emitter apex. Employing this method, the tip radius of Si microemitter is about 200 Å, and the gate aperture can be easily reduced to be about 0.3 μm. This will largely decrease the turn-on voltage of the field emission devices[5].

2. FABRICATION PROCESS

2.1 Formation of sharp tip arrays

1μm thick oxide layer was thermally grown and was then photolithography patterned to form the arrays of circular islands with 1 μm in diameters. The patterns of photoresist were then transformed into underlying oxide using anisotropic reactive ion etching (RIE), as can be seen from Fig. 1 (a). The reactive ion etching od silicon subsequently progressed employing the previously patterned oxide disc as mask. In order to produce the high-aspect-ratio cone-shaped tip, the parameters used in RIE are the gases flow ratio SF_6/Cl_2 of 15/45 (sccm/sccm), the RF power of 50 W and pressure of about 1.4 mTorr. Theis etching process was terminated earlier to reserve the capped oxide unrelieved on the narrow neck of etched silicon pyramids, as shown in Fig. 1 (b). The width of the reserved narrow neck is flexible and typical about 2000~5000 Å. This oxide "capped" silicon pedestal was subsequently exposed to the thermal oxidation ambient. During this process depicted by Fig. 1 (c), the 1 μm-thick capped oxide mask will serve as an oxidation stopper so that the silicon pedestal was laterally oxidized to form a sharp tip at the pedestal's apex. The sharp Si tips is exposed after stripping the thermal-grown

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oxide, as depicted by Fig. 1 (d). Furthermore, some samples of sharpened tip have been overcoated with a 200 Å-thick Cr to evaluate the effect of metal-clad Si tips, as indicated in Fig. 1 (e).

2.2 Gate aperture location employing a self-aligned process

A modified self-aligned process have been successful developed to construct the gated field emitter devices. Referring to Fig. 1 (c), the extraction metal gate is then self-aligned deposited about 2000 Å utilizing sputtering depicted by Fig. 1 (f). During this process, the remaining silicon dioxide caps are not only used to be the lift-off mask but also to be an insulator layer simultaneously to separate the extraction gate from substrate. The typical thickness of as-grown oxide insulator is $0.2 \sim 0.5$ μm majorly depended on the minimum thickness to sharpen and the desirable gate aperture. Following metal gate deposition, the underlying oxide exposed on the discontinuity of metal films was then selective removed using buffer HF (BOE) acid, and the metal-clad oxide caps was simultaneously lift off to expose the buried emitter tips. Figure 1 (g) depicts the completed device structure.

3. RESULTS AND DISCUSSION

3.1 Field emitter arrays (FEA's)

Results of formation the sharp silicon tip as FEA's are shown to Fig. 2. The key parameters of reactive ion etching (RIE) were the choice of reactive gases. Fig. 2 (a) depicts the high aspect-ratio (~ 4.3 μm/1 μm = 4.3) oxide-capped silicon pedestal was achieved by the etching gases mixture of SF_6/Cl_2=1/3. The neck of the conical silicon pedestal is typical about 1000~3000 Å that is determined by etching times. The main problem of RIE etching is the surface roughness caused by tip-etching process in accordance of the SEM micrograph shown in Fig. 2 (a), but can be smoothed by the following oxidation-sharpening treatment. Figure 2 (b) shows the result after only one 950 °C wet-oxidation-sharpening step. The high resolution SEM micrography shown in Fig. 2 (c) indicate that the as-sharpened tip radius is about 200 Å with smooth morphology. This oxidation-sharpening treatment can repeatedly proceed to further reduce the tip radius to be one nm range[4].

3.2 Gated FEA's for vacuum microtriodes

After the oxidation-sharpening process, the 2500 Å-thick-Cr metal is then deposited to be the extraction gate employing sputtering. Since the metal sputtering is an isotropic and conformal deposition process, the metal gate is uniform deposited on the top of oxide layer except the bottom of overhung oxide caps. To complete the emitter fabrication process, the sample after metal-deposition process was immersed by BOE acid to lift off the oxide caps and simultaneously removing the underlying oxide to expose the emitter tips. This process results in a high-aspect-ratio volcano-shaped metal gate with a very small gate aperture surrounding the tip apex region. The gate aperture is then controlled by the grown oxide thickness and neck width of the original Si pedestal. Since the necks etched by RIE will exhibit the non-uniform width distribution in an array, ensuring that all the tips in an array will be completely sharpened by oxidation-stripping process, the minimum requirement of oxidation thickness is determined by the upper limit in the variation of original neck width. For example, Fig. 1 (a) shows RIE etched tip pedestal with neck width about $\sim 2300 \pm 300$ Å. After the 3000 Å-thick-oxide was grown and following the 2500 Å-thick-Cr metal deposition, an uniform gated field emitter array (GFEA) with the gate aperture of 0.33 μm has been achieved, as shown in Fig. 3 (a). Figure 3 (b) is the cross-section view indicates the tip apex is about 0.33 μm recessed to the top plane of gate aperture. Furthermore, Fig. 3 (c) shows that the gate aperture is about 0.26 μm and the tip is nearly at the same level with the top plane of the gate aperture. In both case, the as-fabricated aperture of the volcano-shaped-gate are much smaller than the original pad oxide size of 1μm. This characteristic is superior than the conventional lift-off techniques whose gate aperture is limited by size of oxide cap[6-7]. According to the our previous work in the numerical simulation[5], the more reduced gate aperture means the more increasing in emission current density or the more decreasing the operation voltage at constant current density. Comparing to McGruer et al.[6], this new method decreases the process steps by combining the oxidation sharpening and insulator deposition steps. Moreover, this processes need also much fewer steps than the similar work reported by Spallas[7], due to using thicker oxide caps instead of complex forming spacers and etching steps. In addition, the thermally grown oxide shows a better uniformity and breakdown resistibility than the conventional e-gun deposited oxide film.

3.3 Characterization of filed emission from Si and Cr-clad FEAs

The high vacuum measurement environment was set up to characterize the field emission properties. The vacuum chamber is pumped down by a turbo pump. Cathode contact is made through the holder to the backside of the wafer. The collector (anode) was a copper plate. All cables were shielded except for the ground return path to the power source. The DC measurement system is based on the Keithley 237 high-voltage source units with IEEE 488 interface. The measurement instruments are auto-controlled by computer. The schematic diagram of the test configuration is shown in Fig. 4. During the measurement, the spacing between the emitter (cathode) and collector (anode) was controlled to be a constant of 30μm and the base pressure in testing chamber was about $1.0\sim2.5\times10^{-7}$ torr. Prior to the electrical measurement, the emitters were applied with a high constant voltage of about 1100V to exhaust the adsorbed molecules and evaporate the native oxide. Field emission characterization was obtained from the microtip arrays over a voltage swept from 0 to 1100V and the tip number in an array is 50×50. Each experimental data point was extracted by averaging a few tens of measured results.The characteristics of diode current (Id) versus applied voltage (Va) for the FEAs including pure Si, and Si with Cr surface coating are shown in Fig. 5 (a). The stright slopes in F-N plots shown in Fig. 5 (b) indicated the field-emission characteristic. At Va=1100 V, the diode current of the pure Si FEA without coating is about 1.41 μA. It also shows that the Id=19.8 μA for the 200 Å-thick Cr-clad Si tips is about 15 times higher than those of un-coated tips. It is due to the higher electron-supplement capability and the surface electrical conductivity for the Cr ones as compared with Si. Moreover, the threshold voltage V_T, defined as the emission current Id reaches 1 μA, for pure silicon and Cr-clad are about 1060 V and 855 V, respectively. Thus, the Cr metal surface coating can great improve the field emission capability in comparison with the un-coated Si FEAs.

4. CONCLUSIONS

A new method for fabricating gated field emitter arrays based on the high-aspect-ratio sharp silicon tips have been successfully developed. The extremely uniform results of the volcano-shaped-gate with 0.33 μm and 0.26 μm gate aperture have been achieved without the needs of advanced lithography process. Such devices can be applied to serve as low-voltage vacuum microtriodes. Furthermore, according to the field-emission characterization, the Si FEAs with the thin Cr metal surface coating can greatly improve the field emission capability in comparison with the un-coated ones.

5. REFERENCES

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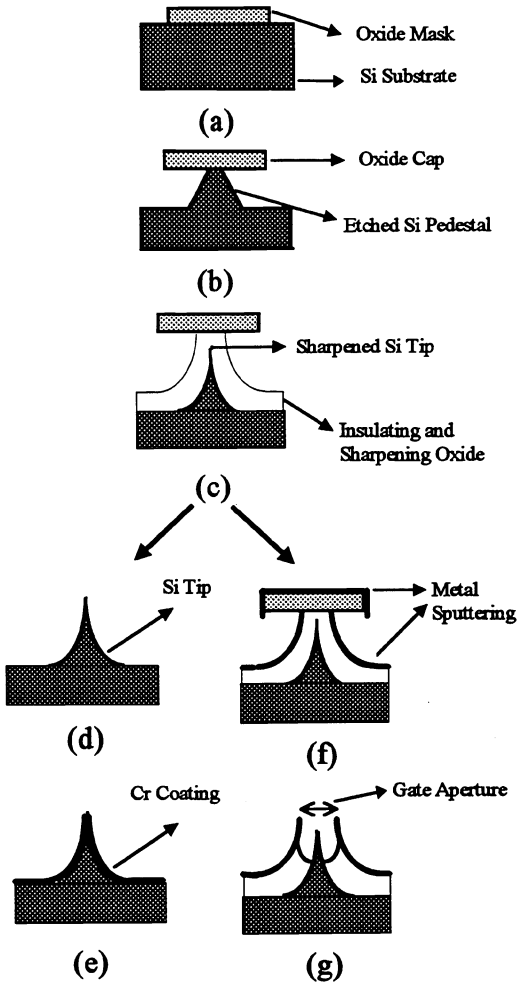


Fig. 1 Scheme of new self-aligned fabrication process

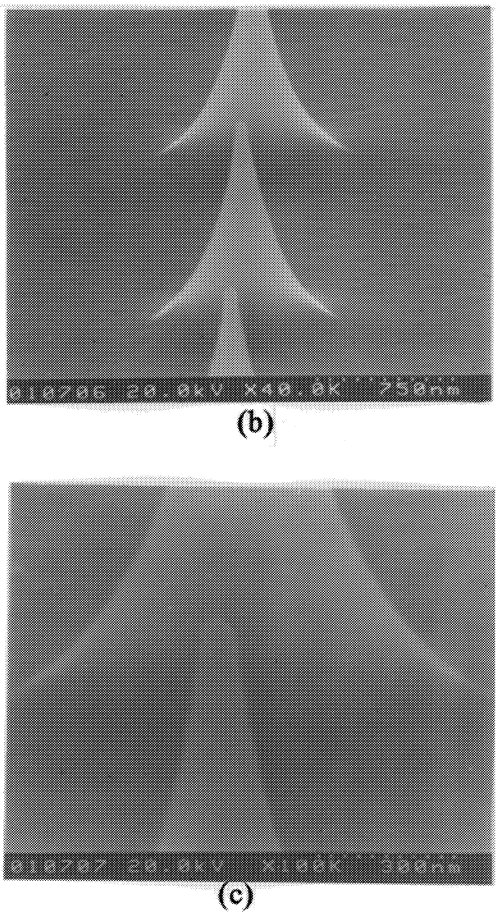
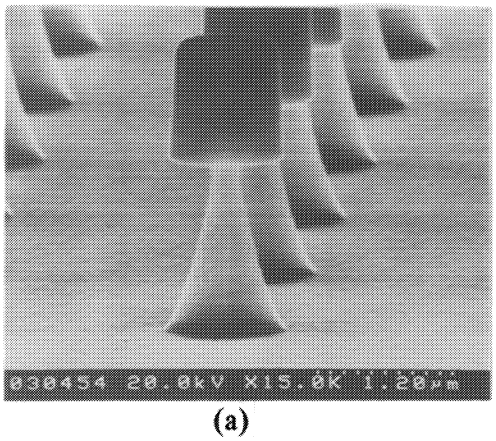
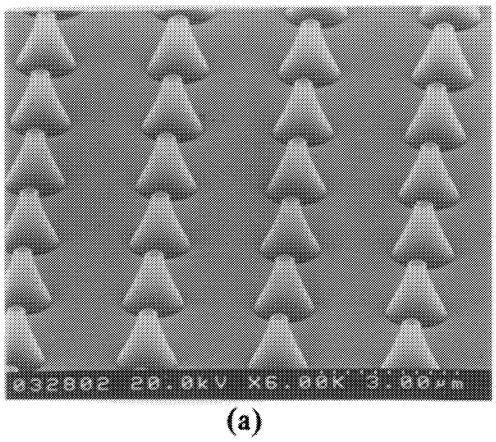
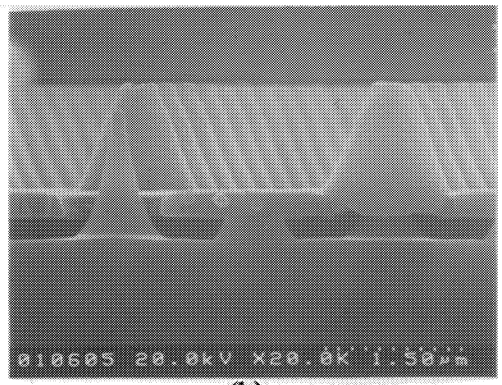


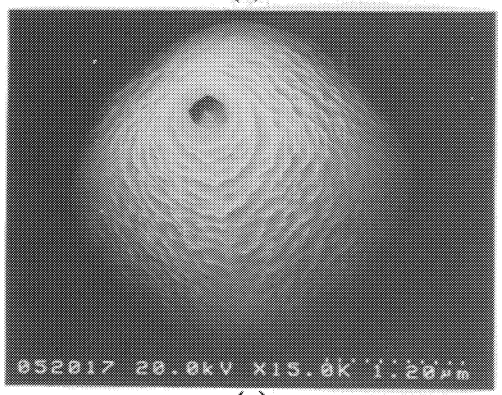
Fig. 2 A Si tip array formed by SF_6/Cl_2 RIE (a) the etched Si pedestal with remained 1μm-width oxide caps (b) a sharp Si tip formed after RIE etching and oxidation-sharpening (c) high resolution SEM micrography shows the tip radius is about 200 Å.







(b)



(c)

Fig. 3 Fabrication results of Si FEAs with the volcano-shaped-gate (a) a uniform 50×50 GFEA with a 0.33 μm gate aperture (b) the cross-section view of the above device indicates that the tips are about 0.3 μm recessed to the top plane of gate aperture (c) another GEFA show a result of only 0.26 μm gate aperture nearly without tip recess.

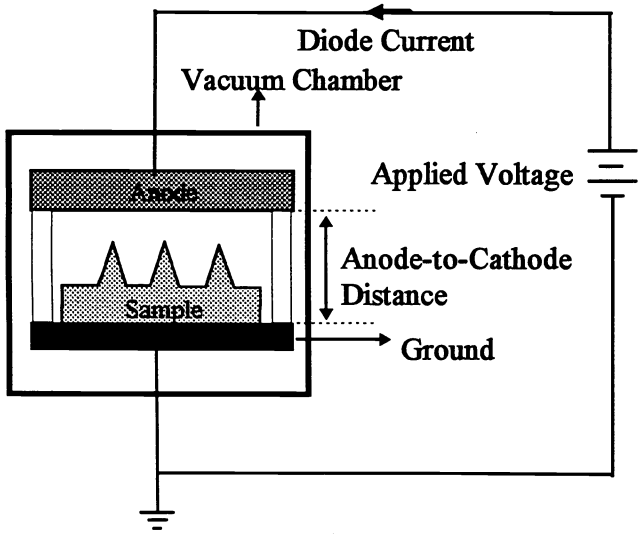
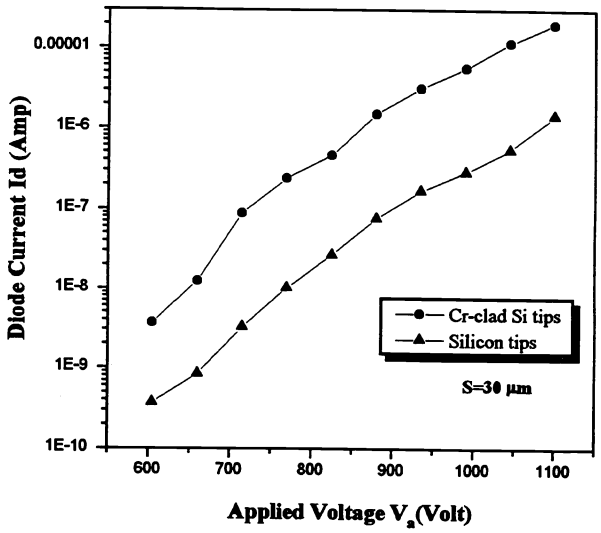
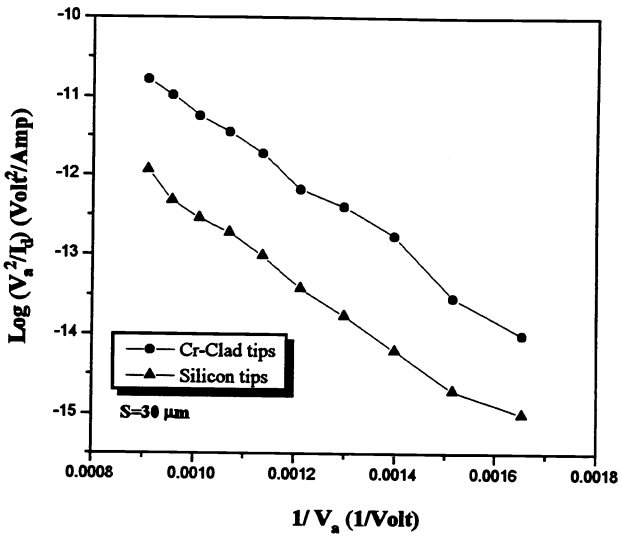


Fig. 4 Configuration of field-emissio characterization



(a)



(b)

Fig. 5 The I-V characteristics of the pure Si and the Cr-clad Si FEAs (a) the Id-Va curve in a log-scale (b) the F-N plots indicate the typical field-emission property.