Fabrication and Characterization of the Pd-Silicided Emitters for Field-Emission Devices

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ABSTRACT

The structure of Pd-silicided field emitters based on the silicon micromachining technology has been demonstrated. The uniform and extremely sharp silicided emitters are formed using wet chemical etching, low-temperature oxidation sharpening (LTOS), coating metal and furnace annealing in N_2 ambient. The sheet resistance and Auger electron spectroscope (AES) results depict the transformation of silicidation. Transmission electron microscope (TEM) of bright-field, dark-field, and diffraction pattern show the formation of silicided emitters. These emitters have potential applications in vacuum microelectronics to obtain superior lifetime, reliability, and stability.

Keywords: Pd, silicided, field emitter, micromachining, sharpening, annealing, TEM, AES

1. INTRODUCTION

Vacuum microelectronic devices have been extensively studied in recent years because of its potential applications in high frequency devices, flat panel displays, microscopy, lithography, and microsensors. Field-emission flat panel displays are the most interesting one for its ultra-high resolution, thin thickness, low power consumption, and good color image. Such properties are particularly desirable for portable computer and electronic avionics displays [1)].

For most applications, vacuum microelectronic devices had to be maintained in ultrahigh-vacuum conditions which was less than 10^{-9} torr. To diminish this problem, it was thus important to choose the appropriate emitter materials that were suitable for a given state and possibly to stabilize the emission. There were some methods to fabricate the field emitters, which consisted of metal, silicon, metal-coated and silicided ones. The first field emitter satisfied the requirements of field-emission devices was the metal emitters, commonly called as "Spindt type" [2)]. The advantage of this type was the high current density that could be achieved for their lower surface work function; the disadvantages included the relatively complicated and non-standard fabrication process to the very-large-scale-integration (VLSI). The emitters were formed by using special electron beam deposition system to deposit metal through near-micron-size gate apertures that were defined lithographically. Hence, precise control of the tip radii and heights of the cones were hard to achieve. The strong temperature dependency of molybdenum emitters was another reliability problem on emission [3)]. On the other hand, the fabrication process of the pyramid-shaped silicon was relatively easily controlled for the tip radii and pyramid heights. The native oxide layer, however, was feasibly produced in the surface of silicon emitters and made the devices deviated from the classical Fowler-Nordheim behavior slightly. Furthermore, the metal-coated microtips with the advantages of silicon one and without the disadvantages of metal one were reported. But if the native oxide layer was not removed completely in the dual-electron-gun evaporation system, the emitter surface would be broken and removed like a result of emitter explosions in the operation [4-6)]. Therefore, the consideration of the reliability and the fabrication technology of the field emitters, made the silicided emitters more suitable for the field emission devices.

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Some interesting aspect was to explore the silicides as field emitting materials. High-temperature stability of silicides throughout IC fabrication and actual usage of the devices have been well established. High-temperature solid-state reactions between deposited metals and Si emitter can be activated by sintering. The silicide formation causes the silicide-silicon interface to be free of surface imperfections and contamination. In addition, the work function of the Mo silicides formed by heating the Si/Mo tips are about 10 % smaller than that of a clean Mo surface. The strong metal-Si bonds are moreover indicative of the excellence of the field emitting materials [7]. The topics of this study are therefore focused on the Pd silicided-emitter. The sheet resistance (Rs), Auger electron spectroscope (AES) and transmission electron microscope (TEM) were used to examine the emitter microstructures and constituents before and after silicidation.

2. FABRICATION

The silicon field emission cathode reported here were fabricated on 3-inch, (100)-oriented, 5 ~ 7 ohm-cm phosphorus-doped silicon wafers. After a standard RCA initial cleaning process, 3000 Å-thick SiO_2 layers were thermally grown on the wafers in an $O_2 + H_2$ ambient at 1100 C to provide a masking material for the following wet chemical etching process, as shown in Figure 1(a). The samples were then photolithographically patterned. The oxide layer was etched using buffer HF acid (or BOE) to form a 40x25 array with 2~5 mm square pads as shown in Figure 1(b). After the photo-resist was removed, the residual oxide pad became the self-aligned etching mask. The silicon pyramids were formed by the isotropic etchant. The etchant consisted of 95% HNO_3, 3% CH_3COOH, and 2% HF (vol. %). The etching process was monitored and terminated when the oxide caps were undercutted almost completely or a few oxide caps in the arrays had been already released. Then, the initial pyramids, as shown in Figure 1(c), would be formed after these processes. In order to obtain the Fowler-Nordheim emission at moderate voltages, a sharp emitter tip is needed. Low-temperature oxidation sharpening technique (LTOS) is used to sharpen the emitter radius [8], as shown in Figure 1(d). The LTOS included reoxidizing the emitter in dry O_2 at 950 C for 2.5 hr and subsequent oxide stripping. This procedure can be repeated as often as necessary to achieve the desired sharpness. Immediately after the sharpened tips were dipped in a concentrated HF, as shown in Figure 1(e), 300 Å-thick Pd film was deposited onto by dual-electron-gun evaporation system, as shown in Figure 1(f). In addition to the substrate with tips, flat Si substrates were also installed into the chamber for comparative studies. The deposition rate of Pd layer was 1.0 Å/s. The vacuum during deposition was maintained to be better than 4×10^{-6} torr. Then, the annealing processes at the temperatures ranging from 200 C to 800 C in N_2 ambient for 60 min were used to form the silicided emitters.

Specimens for cross-sectional TEM observations were prepared and a JEOL-2000FX scanning transmission electron microscope operating at 200 KV was used to examine the microstructures of the formed emitters. In order to protect the silicide emitters, a photoresist was used to cover the whole sample before specimen cleaving. Since the silicided emitters would be milled by the powder which was lapped from the samples. This specimen was cleaved and then lapped from the sides to assure the emitters remained. Then, the specimen was mounted on its side onto a copper ring using epoxy. The acetone was used to remove the photoresist on the silicide emitters and clean the specimen surface. The silicide emitters were studied with the electron beam normal to the emitter axis. The thinning procedure was not necessary because the region near the apex was already electron transparent. The specimen with flat surface for comparison was prepared by the usual process of bonding the identical pieces of the sample face to face, mechanical thinning, dimpling, and finally argon ion milling to electron transparency [9].

3. RESULTS AND DISCUSSION

Figure 2(a) shows a silicon emitter after low-temperature oxidation sharpening and removing the oxide layer with buffer HF solution. The silicon emitter is not sharpened enough in the oxidation procedure. Therefore, it has a small neck on the apex and the tip radius is in the order of 500 Å. The

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apex of this silicon tip will be further sharpened when the oxidation time is added. The sharpening mechanism agrees with the result of Marcus [10]. The final radius of the tip is ranging from 200 Å to 300 Å. The fringes in Figure 2(a) is the thickness effect. Figure 2(b) shows the TEM diffraction pattern corresponding to Figure 2(a). It is the [110]-orientation of silicon, which is normal to the orientation of the emitter. Figure 3(a) shows a TEM bright-field micrograph of a tip deposited with a 300 Å-thick palladium layer. The roughness of the palladium surface is attributed to the Pd grain morphology. Selected area diffraction and dark field images show that the Pd has a grain size less than 100 Å. It can also be seen that the Pd film completely covers all the tip surface. In addition, the emitter has a tip redius less than 300 Å. Figure 3(b) shows a TEM diffraction pattern corresponding to Figure 3(a). The {111}, {200}, {220}, {311}-oriented diffraction rings of polycrystalline palladium are observed. Figure 4(a) shows the TEM micrograph of silicon emitter coated with Pd layer and annealed at 500 C for 60 min. From the dark-field image and the concerning diffraction pattern in Fig. 4(b), it can be seen that the silicide phase Pd_2Si has completely be formed on the whole emitter surface. In addition, the apex of the emitter is also converted into palladium silicide and the radius of the emitter is keep even after the silicidation. In order to further identify the phase of silicided emitter, a flat silicon substrate deposited with a 300 Å-thick Pd layer and subsequent annealed in N_2 ambient at 200 C for 60 min were also analyzed with TEM. Consequently, the bright-field and diffraction pattern, as shown in Figs. 5(a) and (b), indicate the same Pd_2Si phase, as those in Figs. 4(a) and (b). R. A. King and his co-authors also reported that the palladium-silicide-coated silicon emitters were identified by the pulse laser atom probe [11]. However, the shape of the emitter was round and the tip radius of the emitter was larger than 1500 Å due to the different fabrication technique of emitter for the King's report.

In order to understand the constituent of the emitters, the performance of Auger electron spectroscope (AES) was undertaken. Figure 6 shows the AES depth profile for the silicided emitters formed by annealing at 200 C for 60 min. It was observed that the emitters had the palladium atoms twice time more than silicon ones. The phase of these field emitters was thus Pd_2Si, which has been confirmed by the images of transmission electron microscope. Four-point-probe (4PP) was used to measure the sheet resistance of the silicide films. The sheet resistance results could depict the silicide transformation. The sheet resistance (Rs) slightly increased with annealing temperature initially due to the initial phase transition from Pd to Pd-silicide. Then, the sheet resistance decreased slightly with increasing annealing temperature up to 600 C. It can be attributed to the grain growth of Pd silicide. The sheet resistance increased rapidly when the temperature rises above 600 C. It is due to the island formation of the Pd silicide at 700 C and 800 C annealings. The results was also consistent with the TEM micrographs.

4. CONCLUSIONS

In summary, the palladium-silicided emitters was completely fabricated by etching, low-temperature oxidation sharpening, coating metal and furnace annealing in N_2 ambient. The silicide emitters were demonstrated by bright-field, dark-field images and diffraction pattern of transmission electron microscope, Auger electron spectroscope and sheet resistance. The silicided phase of the field emitter was first identified by the transmission electron microscopy. In addition, the TEM results are consistent with Auger electron spectroscopy. The silicided emitter can be concluded to be Pd_2Si. In the consideration of reliability and stability, the silicided emitter is more suitable for the field emission devices.

5. ACKNOWLEDGMENTS

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FIGURE CAPTIONS

Fig. 1 Schematic fabrication processes. (a) Thermal oxidation. (b) Mask formation. (c) Silicon etching. (d) Low-temperature oxidation sharpening. (e) Thermal and Mask oxide removed. (f) Metal deposition and silicidation.

Fig. 2 (a) TEM micrograph of silicon emitter after low temperature oxidation sharpening.
2 (b) TEM diffraction pattern corresponding to Fig. 2(a).

Fig. 3 (a) TEM micrograph of a tip clad with a 300 Å-thick as-deposited palladium layer (Pd/Si tip).
3 (b) TEM diffraction pattern corresponding to Fig. 3(a), showing the diffraction rings of polycrystalline palladium.

Fig. 4 (a) TEM micrograph of the Pd/Si tip annealed in N_2 ambient at 500 C for 60 min.
4 (b) TEM diffraction pattern corresponding to Fig. 6(a), showing the diffraction rings of polycrystalline Pd_2Si.

Fig. 5 (a) TEM micrograph of the flat silicon substrate deposited with a 300 Å-thick palladium layer and subsequent annealed in N_2 ambient at 200 C for 60 min.
5 (b) TEM diffraction pattern corresponding to Fig. 4(a), showing the diffraction rings of polycrystalline Pd_2Si.

Fig. 6 The AES depth profile for the emitters annealed at 200 C for 60 min.

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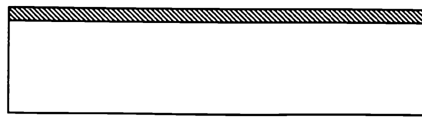

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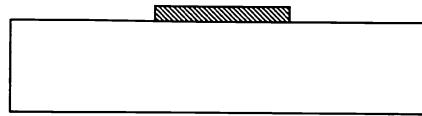

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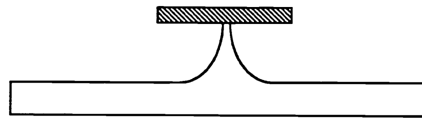

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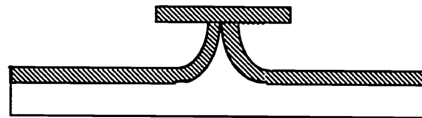

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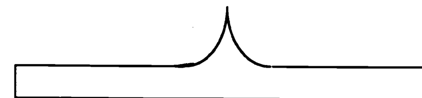

(e)

(f)

Fig. 1

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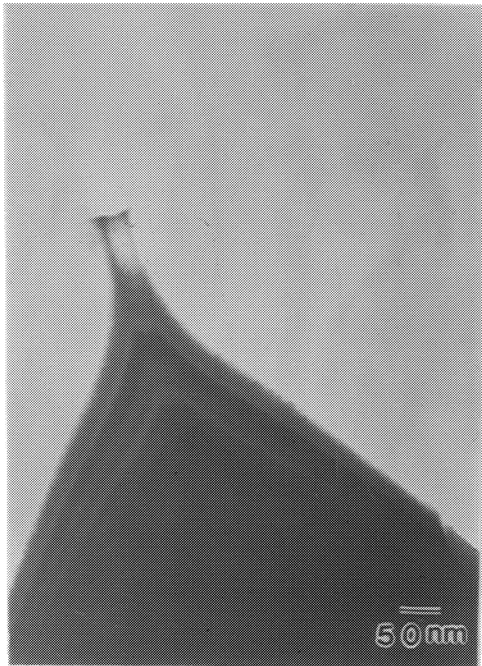

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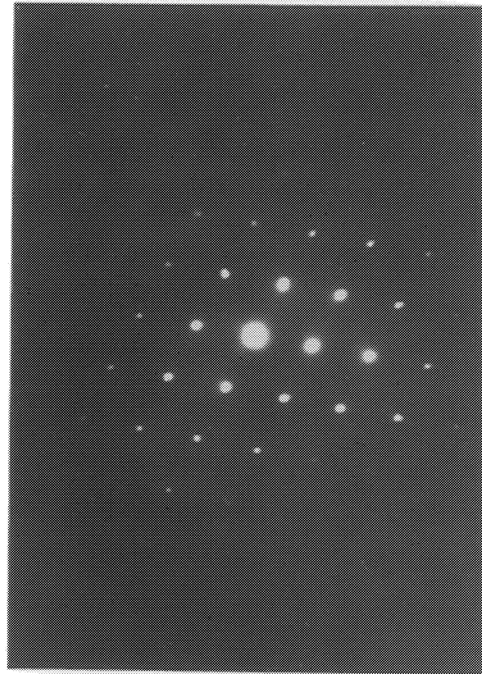

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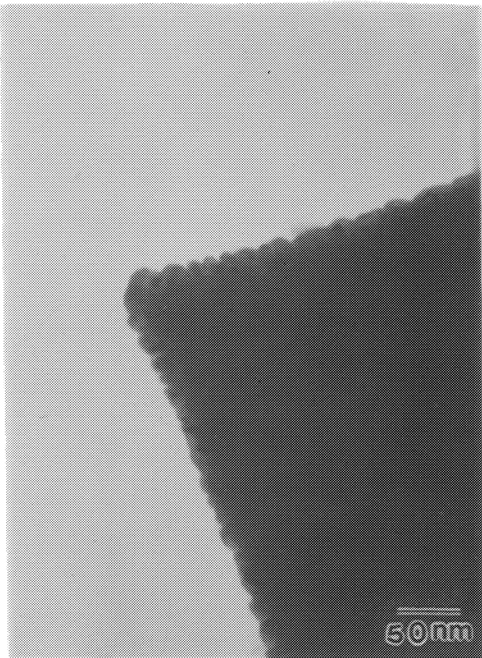
Fig. 2



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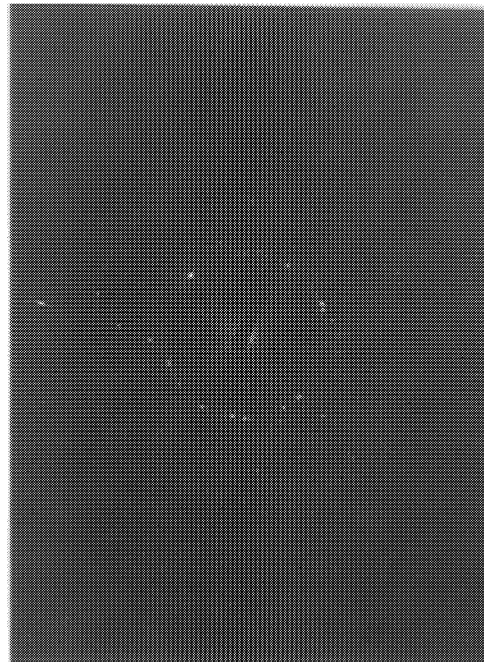

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Fig. 3

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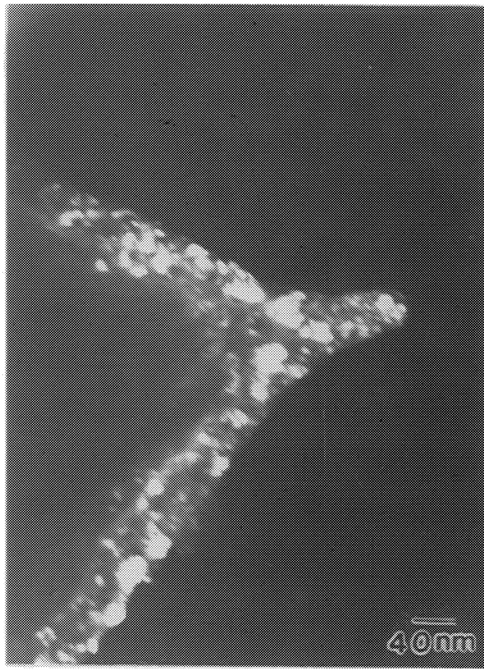

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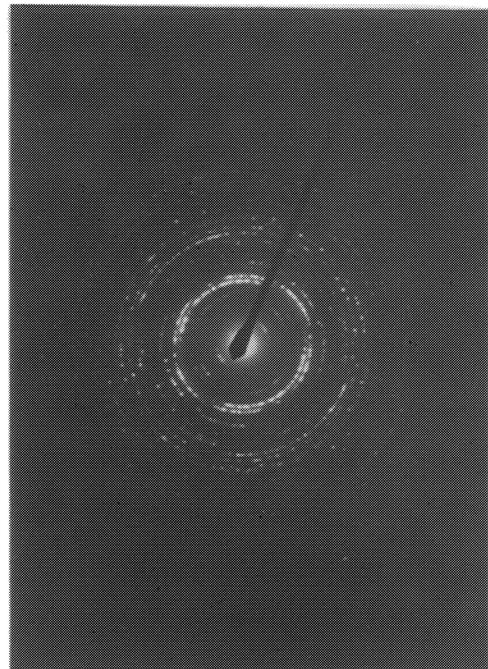

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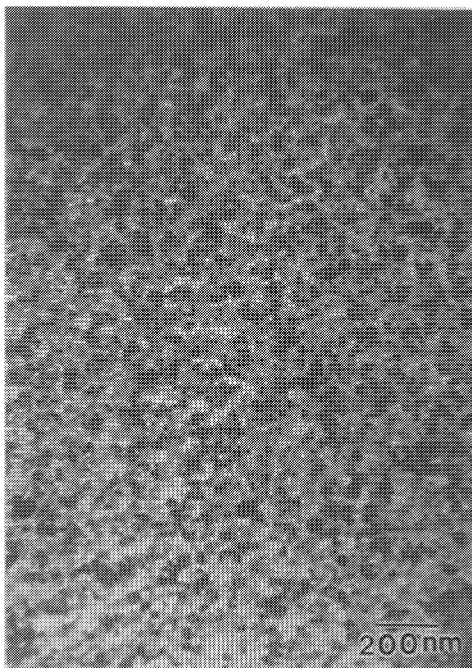
Fig. 4



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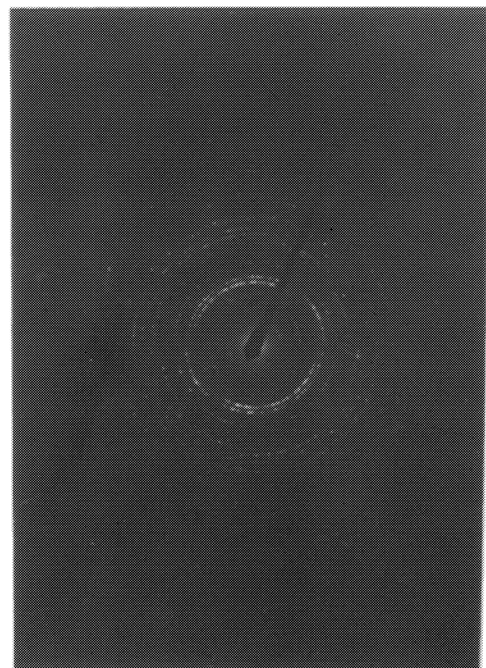

(b)

Fig. 5

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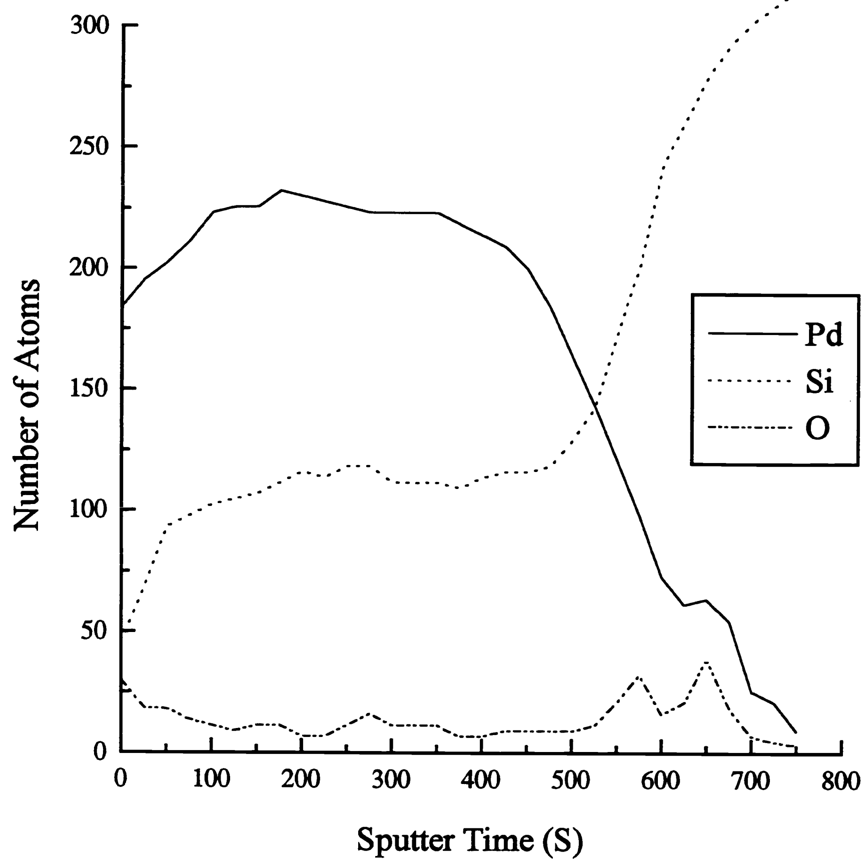

Fig. 6

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