Accurate MOS Device Hot Carrier Models for VLSI Reliability Simulation

Steve S. Chung, J.-J. Yang and J.-S. Su

Department of Electronic Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

Abstract - This paper describes a Spice-compatible circuit reliability simulation model of submicron LDD MOS devices. It incorporates an accurate hot carrier model of the degraded MOSFET characteristics under long term operations, which includes a drain current model and a substrate current model. The drain current reduction is modeled as mobility degradation due to interface states enhanced scattering. The substrate current model is developed based on a new effective electric field concept which shows a significant improvement to the conventional local field model. By characterizing the time-dependent of the device parameters, hot carrier I-V model can be obtained. Comparison of the modeled results with those of experimental shows excellent match for a wide range of device channel length, bias conditions and stress time. Moreover, the reliability simulator that we developed allows prediction of lifetime or aging of a device or circuit in VLSI design.

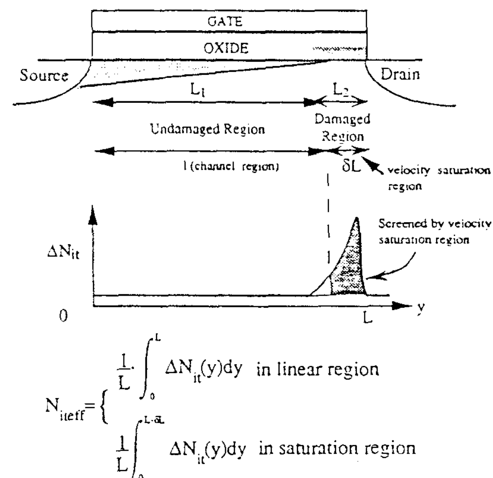
1. Introduction

Analysis of the device or circuit failure under long-term stress environment has become an increasingly important issue in design-for-reliability of VLSI circuits. It is well known that the device or circuit will encounter hot carrier induced reliability problem under long time operating conditions. Hot carrier reliability simulators that can predict circuit reliability are an integral part in the early stages of technology development and circuit design. Simulation tools such as HOTRON [1], RELY [2] and BERT [3] have been developed for such a need. However, accurate simulation of circuit degradation requires an accurate device degradation models such as the drain and substrate current characteristics. Reported models in this aspect are not matured yet.

It is well known that hot carrier induced interface state and oxide trapped charge are the main cause of device degradation [4]. The reported drain current degradation models [5-6] were developed primarily based on conventional MOSFET's, none was done on LDD MOS devices. In addition, owing to the difficulty in knowing the exact information about the amount and distribution of interafce states or oxide trapped charges, none has been made to model the substrate current characteristics (I_B) of stressed MOSFET's in analytical form for circuit simulation use so far. To deal with these problems, in this paper, we present a new form of I_D and I_B models for both fresh and degraded LDD MOS devices. In addition, a reliabaility simulator feasible for predicting the lifetime or aging of a device or circuit under long term stress environment will be demonstrated with a typical example.

2. A Hot Carrier Drain-Current Model for Stressed MOS Devices

It has been experimentally established that for stressed devices, interface states and oxide charges are generated in a form as shown in



$$N_{iteff}=\begin{cases}\frac{1}{L}\int_0^L \Delta N_{it}(y)dy & \text{in linear region}\\ \frac{1}{L}\int_0^{L-a} \Delta N_{it}(y)dy & \text{in saturation region}\end{cases}$$

Fig.1 A model of MOS device with generated interface state profile and screening effect in velocity-saturation region.

Fig.1 at the near device drain region which will induce the so-called oxide damages. The hot carrier induced I_D degradation for MOSFET's is mainly due to these oxide damages, which increases the series resistance at drain region under the oxide spacer (the so-called *spacer-induced degradation*) and enhances surface scattering near the channel region. For the present VLSI technology based on LDD structures, the generated interface state, ΔN_{it}, is more significant than the oxide charges. Therefore, knowing the amount of ΔN_{it} and its distribution are the first step in modeling stressed device I_D current. The DC hot carrier stress was done at biases V_{DS}=7V and V_{GS}=3.5V with source and substrate electrodes grounded. We use a newly proposed technique [7] to explore the interface state distribution by utilizing a fixed based level charge pumping measurement. Fig.2 presents the measured charge pumping current versus stress time. The characterized ΔN_{it} distribution is shown in Fig. 3. Here, by including the spacer-induced degradation effect into mobility degradation, the local mobility term can be expressed as

$$\mu_{nit}(y)=\frac{\mu_y}{1+\alpha\Delta N_{it}(y)} \tag{2.1}$$

where μ_y is the mobility without hot carrier effect and α is mobility degradation factor. Using our previous model in [8], the drain current degradation model for an oxide damaged device is listed in Part A of Table 1. The two decisive parameters that determine degraded I_D characteristics are average effective generated interface states ($N_{it,eff}$), which is the average of $\Delta N_{it}(y)$ along the effective damaged region that affects device performance, and the factor α. As the device is

IEEE 1995 CUSTOM INTEGRATED CIRCUITS CONFERENCE

0-7803-2584-2/95 $3.00 ©1995 IEEE

the local electric field for calculating channel impact ionization rate. The widely used form for device analysis and circuit simulation utilizes the maximum electric field (E_m) in the local electric field for the specific device structure as the dominant factor in hot carrier generation. However, for the short channel MOS devices, the local field model fails to model the I_B especially at high gate biases, since the impact ionization rate has to be modeled nonlocally by considering the two-dimensional heating effects. To improve modeling accuracy, we propose a new modeling approach based on the so-called *effective electric field* (E_{eff}) instead of the E_m concept to calculate the impact ionization rate as well as the substrate current. The new I_B expressions are listed in Part B of Table 1. Here, the impact ionization rate α_i=A·exp(-B/E_{eff}) is used in the conventional LE model, in which we define $E_{eff}=(V_{DS}-V_{Dhot})/l_d$ as the effective electric field inside a device that is decisive for hot carrier behaviors. E_{eff} can be extracted experimentally using eq. (5). This E_{eff} can really reflects the two-dimenional non-local field effect within devices

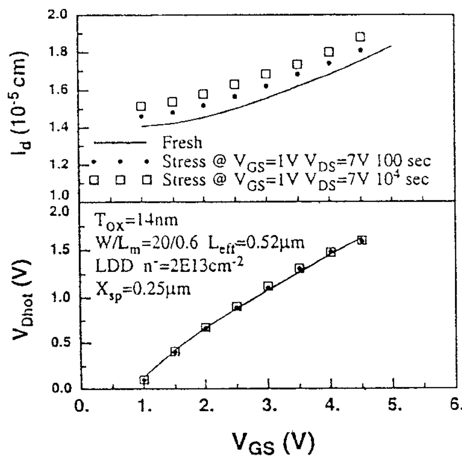


Fig. 6 Variations of V_{Dhot} and l_d with time during hot carrier stress.

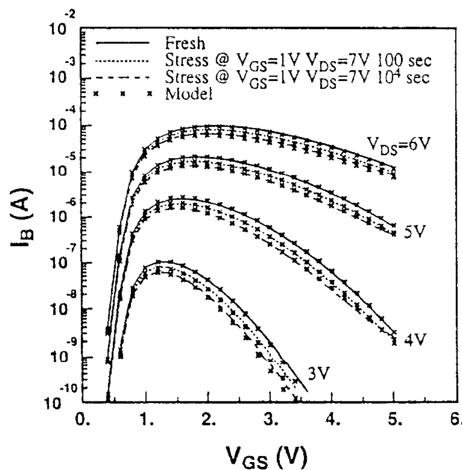


Fig. 7 Comparison between modeled and experimental fresh and stressed device I_B characteristics.

Owing to the presence of oxide trapped charges and interface states, the electric field in the surface depletion area changes. As a result, the E_{eff} varies and then modulates the magnitude of the substrate current. In other words, V_{Dhot} and l_d changes with stress time. Through the characterization of the time evolution of V_{Dhot} and l_d, the substrate current of a stressed MOSFET can be adequately modeled. Fig. 6 shows the time evolution of V_{Dhot} and l_d during hot carrier stress done at V_{GS}=1V and V_{DS}=7V, in which V_{Dhot} is varied slightly, while the values of l_d increases with stress time, therefore, the resultant E_{eff} decrease. I_B then decreases. Fig. 7 shows the comparison between modeled and experimental fresh and stressed I_B characteristics, excellent match can be achieved.

4. Circuit Reliability Simulation Example

In addition to the above model equations, device degradation models due to the hot carrier effect under long term stress environment are the key element for reliability analysis. Using quasi-static approach, the following form for N_{it} variations in a period of time can be predicted.

$$N_{it}=C[\frac{t}{T}\sum_{p=1}^{h}\frac{I_D(t_p)}{W}(\frac{I_B(t_p)}{I_D(t_p)})^m(t_p-t_{p-1})]^n \qquad (4.1)$$

where t is the stress time and T is the signal cycling time. Once I_B and I_D are established, the quantity of N_{it} after long time stress can be predicted. The two model equations and the associated time-varying parameters can then be incoporated into the simulator, from which devices' drain current can be simulated at any instant of time and the lifetime for each in-circuit device can be found. The developed simulator has the framework as shown in Fig.8.

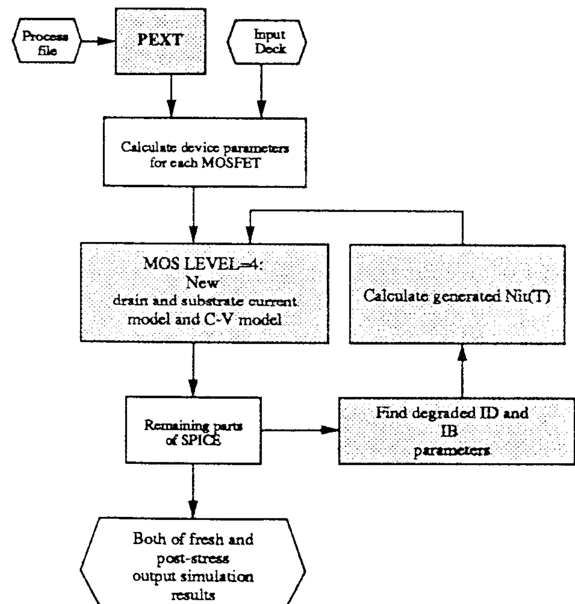


Fig. 8 HotSpice: The modified Spice for hot carrier reliability analysis.

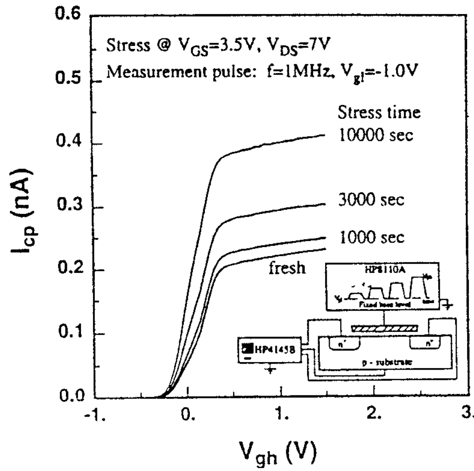


Fig. 2 Charge pumping measured current as a function of device stress time.

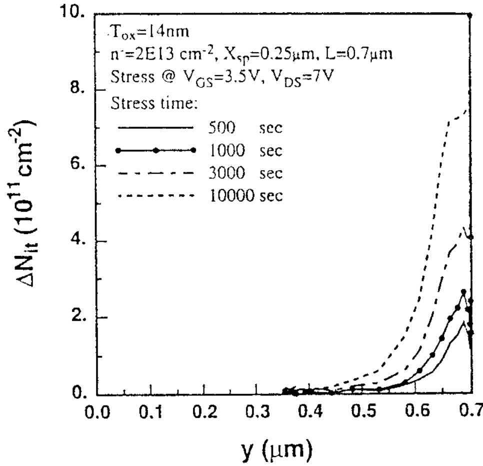


Fig. 3 Time evolution of hot carrier generated interface states distribution for a 0.7μm LDD device.

biased in saturation operation, the lateral electric field modulates the length of channel inversion layer as illustrated in Fig. 1. The interface states located above the velocity-saturation region is therefore screened and will not degrade the channel mobility. The phenomenon is called *screening effect* which explains why the drain current is hardly degraded at deep saturation region (biased at high V_{DS}-V_{GS} value). The $N_{it,eff}$ expression in Fig.1 includes this screening effect. In general, the mobility degradation factor α, eq. (2), can be extracted experimentally as functions of drain and gate voltages, in which ΔI_{CP} is the charge pumping current increment after the stress that directly related to the total amount of ΔN_{it}. Fig.4 give the extracted values of α which varies with stress time. The δL of stressed device can be obtained using an iteration algorithm. Fig.5 compares the modeled and experimental fresh and stressed drain current characteristics, in which excellent match can be achieved.

3. Substrate Current Model for Fresh and Stressed Devices

The conventional approach [9] for the I_B models were based on

A. Drain Current Model

1. *Linear region* ($V_{GS} \geq V_T$ and $0 \leq V_{DS} < V_{DSAT}$)

$$I_D = \mu_0 C_{ox}(W/L)[(V_{GS}-V_T)-0.5aV_{DS}]V_{DS}/ [(1+\theta(V_{GS}-V_T))(1+\eta V_{DS})(1+\alpha N_{iteff})+ R_t(V_{DS}/V_{DSAT})\,\beta_0(V_{GS}-V_T-0.5aV_{DS})] \quad (1)$$

where $R_t = 0.5RV_{dsat}/(V_{GS}-V_T-0.5aV_{DSAT})$

$$R = R_0+R_1(V_{GS}-V_T)+R_2(V_{GS}-V_T)^2$$

$$\alpha = qfwL_{eff}(\Delta I_D/I_D)/\Delta I_{cp} = At^n \quad (2)$$

2. *Saturation region* ($V_{GS} \geq V_T$ and $V_{DS} > V_{DSAT}$)

$$I_{d,sat} = \beta(V_{GS}-V_T-0.5aV_{dsat})V_{dsat}/(1+\beta RV_{dsat})$$

$$I_D = I_{d,sat}/(1-\delta L/L) \quad (3)$$

where

$$\beta = \beta_0/[(1+\theta(V_{GS}-V_T))(1+\eta V_{DS})(1+\alpha N_{iteff})$$

$$\beta_0 = \mu_0 C_{ox}(W/L)$$

B. Substrate Current Model

$$I_B = (A/B)(V_{DS}-V_{Dhot})I_D \exp(-B/E_{eff}) \quad (4)$$

$$E_{eff} = \frac{(V_{DS}-V_{Dhot})}{l_d} = \frac{B}{\ln\left(\frac{I_D A(V_{DS}-V_{Dhot})}{I_D B}\right)} \quad (5)$$

where l_d, V_{Dhot}: functions of stress time

Table. 1 Model formulations of I_D and I_B for an oxide damaged LDD MOSFET.

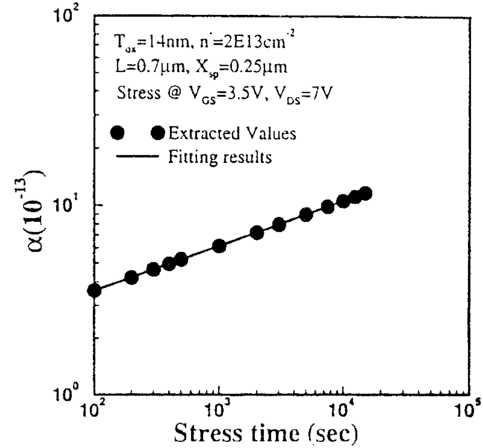


Fig. 4 Time evolution of mobility degradation factor α during hot carrier stress.

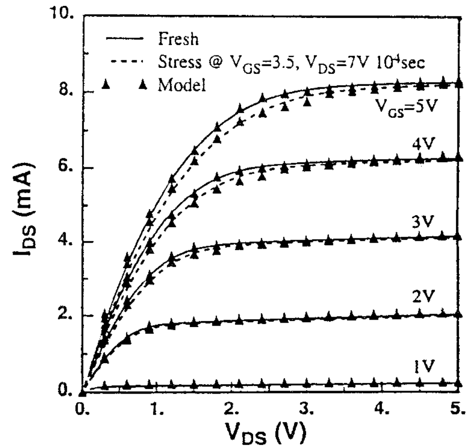


Fig. 5 Comparison between modeled and experimental fresh and stressed device I_D characteristics.

One typical example for demonstrating the reliability simulation of a 9-stage CMOS ring oscillator circuit is illustrated in Fig.9(a). The simulated circuit outputs have been shown in Fig.9(b), for comparison with and without stress. One practical application of the simulation results is shown in Fig. 9(c), in which from the simulated $\Delta I_D/I_D$ values for devices we may determine the lifetime of each transistor.

5. Conclusion

In this paper, a circuit level reliability simulation tool has been developed for predicting the hot carrier induced degradation effect and the evaluation of lifetime in VLSI circuits. This simulator incorporates a new hot carrier MOSFET I-V model for both drain and substrate currents. The resulting reliability simulator can be used for simulating and observing the circuit behavior, such as the evolution of device or circuit degradation, and lifetime evaluation under long term stressed conditions. In particular, it can be used as a design aid, for improving the long term reliability of VLSI circuits through design modifications.

Acknowledgements The authors would like to acknowledge support mainly from the National Science Council, Taiwan, R.O.C, under contract *NSC81-0404-E009-620*. Samples provided by the Tsmc, Hsinchu Industrial Park, Taiwan, ROC., are also gratefully acknowledged.

References

[1] S. Aur et al.,in *IEDM Tech. Dig.*, p.498, 1987.
[2] B.J. Sheu et al., *IEEE J. Solid-State Circuits.*, p. 473, 1989.
[3] P.M. Lee et al., in *IEDM Tech. Dig.*, p. 134, 1988.
[4] P. Heremans et al., *IEEE Trans. ED*, p. 2194, 1988.
[5] Y. Leblebici et al., *IEEE Trans.CAD*, p. 235, 1992.
[6] Khandker N. Quader et al., *IEEE Trans. ED*, vol. 40, no. 12, pp. 2245-2254, 1993.
[7] S.S. Chung et al., *Proc. SSDM.*, Aug.29-Sept.1, Chiba, Japan, p. 841, 1993.
[8] S.S. Chung et al., *IEEE Trans. ED.*, p.1691, 1989.
[9] T. Y. Chan et al., *IEEE EDL*, vol. EDL-5, pp. 505-507, 1984.

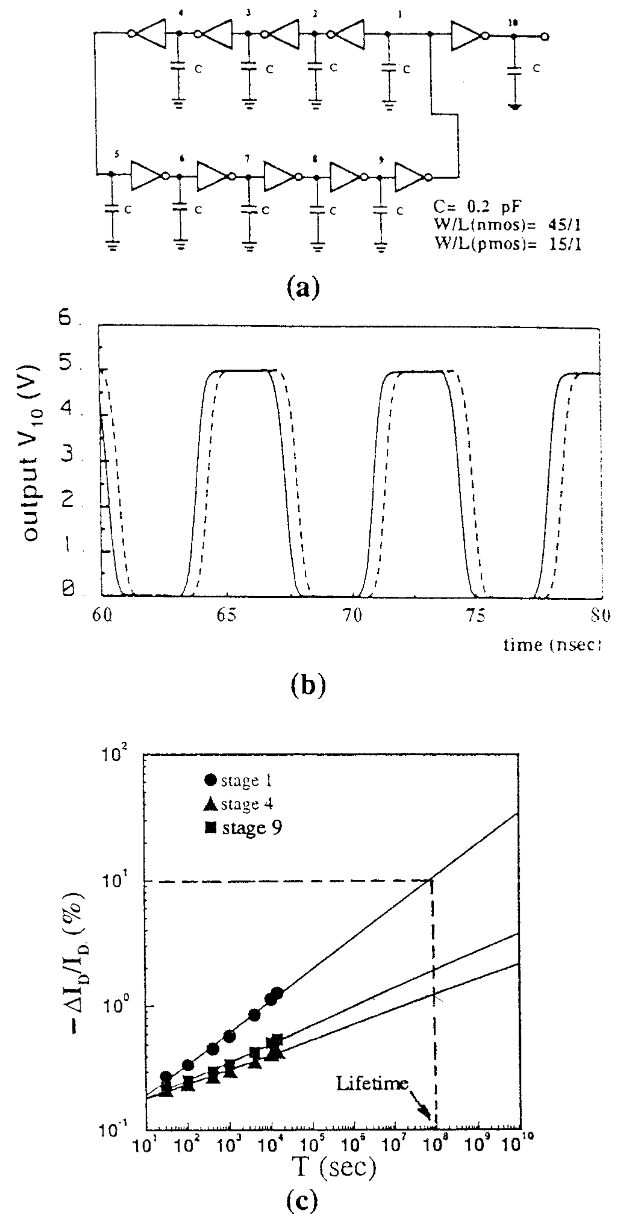


Fig.9 (a) A 9-stage ring oscillator for simulation.
(b) The output waveform before and after stress.
(c) Simulated $\Delta I_D/I_D$ for determining lifetime.