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A NEW GATE CURRENT SIMULATION TECHNIQUE CONSIDERING Si/SiO_2 INTERFACE TRAP GENERATION

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Abstract—An efficient and accurate 2D numerical simulation technique is developed to study the hot-electron effects on short-channel *n*-MOSFETs. The 1D substrate injection probability used by Ning *et al.* has been further modified by considering the channel hot-electron-enhanced injection probability. Moreover, the hot-electron-injection-induced Si/SiO_2 interface-trap generation and its effects on MOSFET drain, substrate and gate currents have also been taken into consideration. It is shown that the generated electron traps at the Si/SiO_2 interface enhance both the impact ionization rate and the degradation of MOSFET characteristics but retard the injection probability of hot electrons into the gate oxide. The spatial distribution of the generated Si/SiO_2 interface traps calculated by our model has been well verified by the charge pumping measurement. In addition, the simulated substrate current, gate current, and degradation of drain current are in good agreement with the experimental results of a short-channel *n*-MOSFET with the oxide thickness of 100 Å and the effective channel length of 0.45 μm for wide ranges of drain and gate biases.

1. INTRODUCTION

Device degradation caused by the hot-carrier effect has been recognized as a major concern as the feature size of submicrometer MOSFET is further scaled down. This kind of instability is mainly due to the substantial increase of the interface/oxide trapped charges generated by hot-carrier injection[1–3]. On the other hand, the Channel Hot-Electron Injection (CHEI) has been widely used as the programming mechanism for denser and faster nonvolatile memory devices nowadays[4–6]. Consequently, the optimized design technique for reliable MOSFET and memory devices, particularly using advanced high-density submicrometer technologies, should need the accurate modelings of gate injection current and interface/oxide trap generation.

A simple and phenomenological model for the substrate hot-electron injection probability of MOS capacitor was first developed by Ning *et al.*[7]. Subsequently, Tam *et al.*[8], based on the mean-free-path concept, had modified Ning's model for channel hot-electron injection in MOSFET. However, this empirical model only considers the maximum channel electric field and cannot be directly applied to a 2D device simulator. Roblin *et al.*[3], based upon Tam's injection model, had developed a physical model for hot-electron trapping and aging of *n*-MOSFET. This model had been used to characterize the degradation of threshold voltage and transconductance but was not applied to the substrate and gate current simulation. Recently, several 2D numerical simulation techniques have been developed to characterize the substrate and gate currents using the solution of Boltzmann transport equation via the Monte Carlo (MC) method[9–13]. However, some key issues concerning the physics of hot-carrier transport at the Si/SiO_2 interface remain unknown[14]. Furthermore, these approaches do not consider the effects of interface traps generated by hot carrier on scaling-down MOSFETs.

In this work, a simple and accurate gate current model is presented, in which the conventional 1D substrate injection model[7] is modified by considering the equivalent hot-electron-enhanced Si/SiO_2 interface barrier lowering. It will be shown that only one fitting parameter is introduced into our new developed model and is found to be a constant for wide ranges of applied biases. Moreover, the kinetics of Si/SiO_2 interface-trap generation due to hot-electron injection at high drain and gate biases can be included in our calculation. The simulated spatial distribution of the Si/SiO_2 interface traps has been well verified by the charge pumping measurement[15,16]. Based upon these considerations, the developed model can accurately simulate the drain, substrate and gate currents of short-channel *n*-MOSFETs simultaneously. Furthermore, the degradation of I–V curves caused by the generated Si/SiO_2 interface traps can also be accurately characterized by our model.

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2. MODEL

By scaling the geometrical dimensions of a MOSFET while keeping the supply voltage constant, the high channel electric field may generate electron–hole pair through impact ionization, and some of the impact ionization-generated carriers will gain enough energy from high field to overcome the potential barrier at the Si–SiO_2 interface, resulting in the gate current. Moreover, the hot electrons can generate the oxide and interface traps, resulting in serious device degradation. The tool for the study of hot carrier effect should be able to quantitatively determine these two effects and are emphasized below.

2.1. Modified injection probability

From the substrate injection model used by Ning *et al.*[7], electrons injected from various positions in silicon can be phenomenologically described by an equivalent injection point with the distance d away from the Si/SiO_2 interface, as shown in Fig. 1. The injection probability can be characterized by:

$$P = A\exp\left(-\frac{d}{\lambda}\right), \quad (1)$$

where A is a normalization constant; d is equivalent injection distance away from the Si/SiO_2 interface with the potential energy of the Si/SiO_2 interface equal to the 1D effective barrier Φ_B; λ is the mean-free-path of optical phonon–electron collision and has been determined experimentally to be about 91 Å.

The 1D effective barrier height Φ_B is expressed as:

$$\Phi_B = \Phi_{B0} - \alpha E_{ox}^{1/2} - \beta E_{ox}^{2/3}, \quad (2)$$

where $\Phi_{B0} = 3.1$ eV is the intrinsic Si/SiO_2 interface barrier height for electrons; E_{ox} is the oxide electric field; $\alpha = 2.59 \times 10^{-4}$ $e\,(\mathrm{Vcm})^{1/2}$ is the coefficient of the barrier lowering due to the image force [the dashed line in Fig. 1(a)]; and $\beta = 1.0 \times 10^{-5}$ $e\,(\mathrm{Vcm}^2)^{1/3}$ is the equivalent barrier lowering due to Fowler–Nordheim tunneling. Note that in Ning's experiment, electrons were optically generated and the source/drain electrodes of n-MOSFET were grounded, while a large negative bias was applied to the substrate and a positive bias was applied to the gate electrode. In such a measurement setup, electrons in the conduction band of the substrate are only swept by the vertical electric field. To properly extend this 1D model to hot-electron problems in short-channel n-MOSFETs, where the lateral electric field plays an important role on hot-electron behaviors, we should further take the effects of lateral electric field into consideration. It is known that the lateral electric field raises the energy of these impact-ionization-generated electrons, as shown in Fig. 2(a), and makes them much easier to overcome the Si/SiO_2 interface potential barrier. In order to keep the injection model as simple as possible, we introduce an additional "hot-carrier-induced barrier lowering" term [shown by Φ_{BL} in Fig. 2(a)] for the effective Si/SiO_2 interface barrier height in eqn (2) to represent the equivalent lateral-field enhanced injection effect. Therefore, the 2D effective barrier height is given as:

$$\Phi_{B,2D} = \Phi_{B0} - \alpha E_{ox}^{1/2} - \beta E_{ox}^{2/3} - \Phi_{BL}, \quad (3)$$

and

$$\Phi_{BL} = \gamma\frac{J \cdot E}{|J|}, \quad (4)$$

where $J \cdot E/|J|$ is the lateral electric field along the current path; γ is an empirical coefficient and can be directly obtained by fitting the measured gate current.

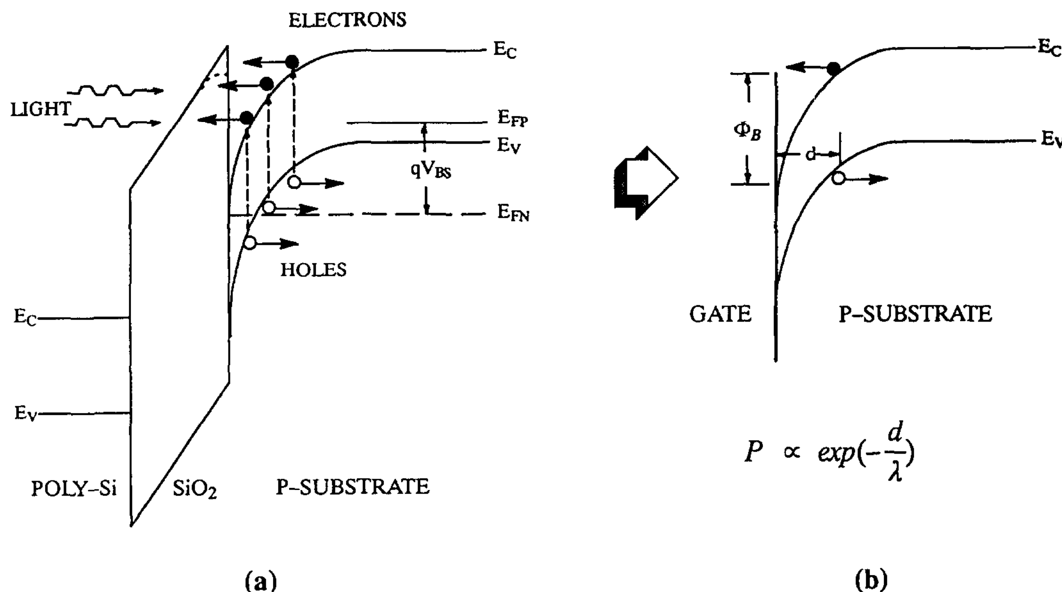

Fig. 1. (a) Illustration of the conventional 1D injection process due to optically generated electrons; (b) the equivalent injection distance for modeling the injection probability.

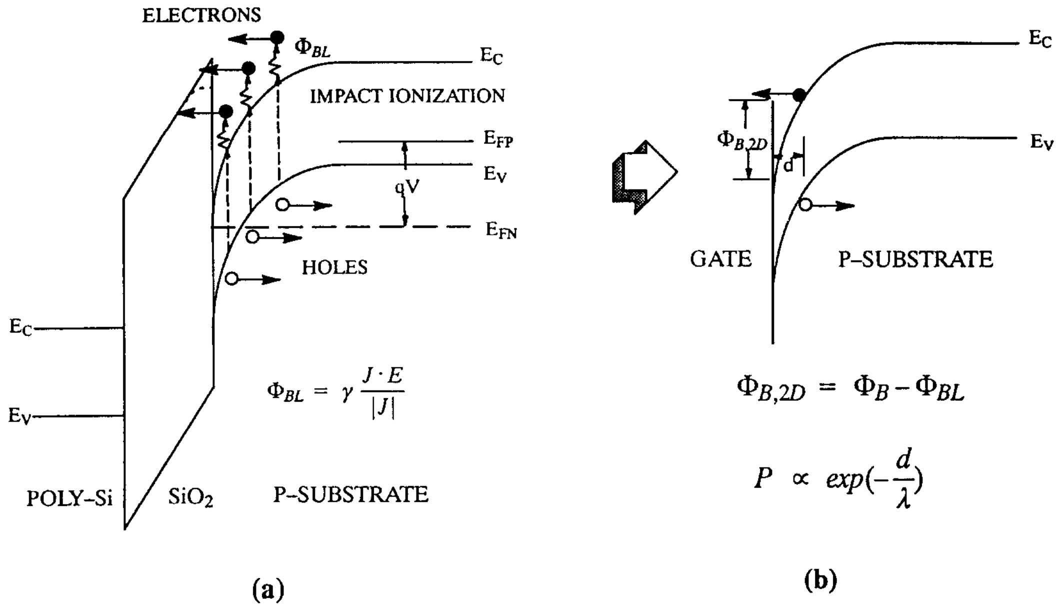

Fig. 2. (a) Illustration of the 2D injection process with hot-carrier enhanced barrier lowering effect; (b) the equivalent injection distance for our 2D injection probability modeling.

Following Ning's idea, the various injection sources along the mesh line normal to the Si/SiO_2 interface can shrink to one injection point, as shown in Fig. 2(b), and d is the equivalent distance away from the Si/SiO_2 interface with the potential energy equal to the 2D effective barrier height as given in eqn (3).

When the vertical field near the drain junction is high for hot-electron injection (generally in the case of $V_{gs} > V_{ds}$), the impact-ionization-generated hot carriers are mainly located very close to the Si/SiO_2 interface. Therefore, the calculation of the equivalent injection distance d can be simplified as:

$$d = \frac{\Phi_{B,2D}}{qE_{\perp}}, \quad \text{for } V_{gs} > V_{ds}, \tag{5}$$

in which $E_{\perp}$ is the vertical surface electric field. As the field E_{ox} near the drain island becomes repulsive for electrons (as normally happens at the drain junction of n-MOSFET with $V_{gs} < V_{ds}$), we expect no contribution of gate current from this portion of channel hot electrons, i.e.

$$P = 0, \quad \text{for } E_{ox} < 0. \tag{6}$$

In summary, the implemented 2D injection probability of each mesh line normal to the Si/SiO_2 interface is simply given as

$$P = \begin{cases} A \exp\left(-\dfrac{\Phi_{B,2D}}{qE_{\perp} \cdot \lambda}\right), & \text{for } E_{ox} > 0 \\ 0, \quad \text{for } E_{ox} \leq 0 \end{cases}. \tag{7}$$

2.2. *Generation and occupation of Si/SiO_2 interface traps*

The Si/SiO_2 interface traps will be generated by hot electrons through breaking the weak bonds at the Si/SiO_2 interface and can be calculated by the following time- and spatial-dependent rate equation:

$$\frac{dN_{it}(x,t)}{dt} = \frac{J_{inj}(x,t)\sigma}{q}[N_{total} - N_{it}(x,t)], \tag{8}$$

where J_{inj} is the injection current density; σ is the capture cross-section; N_{total} is the total weak bond density that can be broken during the injection process and assumed to be uniformly distributed along the channel and source/drain islands. When the external drain and gate biases are large enough, hot-electron injection occurs. Since the impact-ionization-generated carriers are nonuniformly distributed in the high field region near the drain junction, the injection current $J_{inj}(x,t)$ as well as the generated Si/SiO_2 interface-trap density $N_{it}(x,t)$ are also localized near the drain junction. Some of the generated interface traps can be occupied by the injected electrons. The occupation function depends on the external bias and is simply given as:

$$f_0 = \frac{1}{1 + \exp\left[\dfrac{E_t - E_F}{k_B T}\right]}, \tag{9}$$

where E_F is the quasi Fermi-level and E_t is the "effective" trap level.

The density of occupied electrons $N_{oc}(x,t)$ at certain bias condition is:

$$N_{oc}(x,t) = N_{it}(x,t) \cdot f_0. \tag{10}$$

Because the surface potential is strongly influenced by the presence of Si/SiO_2 interface trapped electrons[17,18], Poisson's equation should include the contribution of these trapped electrons in order to accurately calculate the potential and electric field distributions.

3. COMPARISONS BETWEEN SIMULATION AND EXPERIMENTAL RESULTS

The test device under study is a conventional n-channel MOSFET with the gate-oxide thickness (T_{ox}) of 100 Å and the effective channel length of 0.45 μm. The non-uniform channel profile can be described by the equivalent Gaussian profile, i.e.

$$N_{peak} \exp\left[-\left(\frac{y - R_p}{\sqrt{2}\Delta R_p}\right)^2\right] + N_{sub}, \qquad (11)$$

where N_{peak} is the peak concentration of channel profile; R_p is the projected range; ΔR_p is the straggle of the Gaussian profile; y is the distance away from the Si/SiO_2 interface; and N_{sub} is the substrate doping concentration. Note that the parameters in the substrate profile can be extracted by the threshold voltage vs substrate bias curve of a long-channel device and further checked by the subthreshold current vs substrate bias curves. The source/drain n^+ diffusion islands are assumed to have a junction depth R_j and a lateral diffusion ratio f. The equivalent source/drain doping profile is assumed to be a Gaussian-tail profile and can be expressed as:

$$\begin{cases} N_{SD}(y) = N_{max} \ \text{for}\ 0 \leqslant y \leqslant R_{pd} \\ N_{SD}(y) = N_{max} \exp\left[-\left(\frac{y - R_{pd}}{\sqrt{2}\Delta R_p}\right)^2\right] \ \text{for}\ R_{pd} \leqslant y \leqslant R_j. \end{cases} \qquad (12)$$

The detailed descriptions of device parameters are shown in Table 1. The parameters of the source/drain profile can be extracted by the drain-induced barrier lowering from the subthreshold current as a function of drain biases. The detailed extraction method can be found elsewhere[19].

In order to study the injection and trapping characteristics in detail, we measured the charge pumping current in conjunction with each gate current measurement by HP4145 and HP8115A. The detailed experimental flowchart is shown in Fig. 3. Just before the I–V measurement, the spatial distribution of intrinsic interface traps is determined by using the charge pumping technique, and then the basic I_{ds}-V_{gs} and I_{ds}-V_{ds} curves are measured in order to extract all the device parameters. The bias ranges of these basic I–V characteristics are carefully chosen for parameters extraction without introducing high-field stress. Then, the substrate current, gate current, and corresponding drain current with the applied gate bias from 0 to 7 V are measured simultaneously at high drain bias (beginning with $V_{ds} = 4$ V). After that, the charge pumping current is measured again to monitor the generation of interface traps. Furthermore, the I–V curves under low V_{gs} and V_{ds} biases are also measured to study the degradation of I–V characteristics due to these generated interface traps. These processes are repeated in sequence with $V_{ds} = 4$, 5 and 6 V. The spatial distribution of Si/SiO_2 interface traps extracted from the charge pumping measurement is shown in Fig. 4. We can see that the Si/SiO_2 interface traps are generated gradually due to each gate current measurement step. Also from the analysis of charge pumping current[20], we find that there are no apparent oxide traps generated in addition to the Si/SiO_2 interface traps as marked by Δ in Fig. 4. Therefore, all features discussed below are obtained without the influence of oxide traps.

Table 1. The extracted device parameters for gate current simulation

Device parameters	Conventional n-MOSFET
T_{ox} (Å)	100
L_{eff} (μm)	0.45
Width (μm)	100
V_{TB} (V)	−0.79
N_{sub} (cm^{-3})	3.0×10^{15}
N_{peak} (cm^{-3})	1.18×10^{17}
R_p (cm)	5.23×10^{-5}
ΔR_p (cm)	6.74×10^{-5}
N_{max} (cm^{-3})	1.0×10^{20}
R_{pd} (cm)	1.7×10^{-5}
R_j (cm)	2.3×10^{-5}
f	0.7

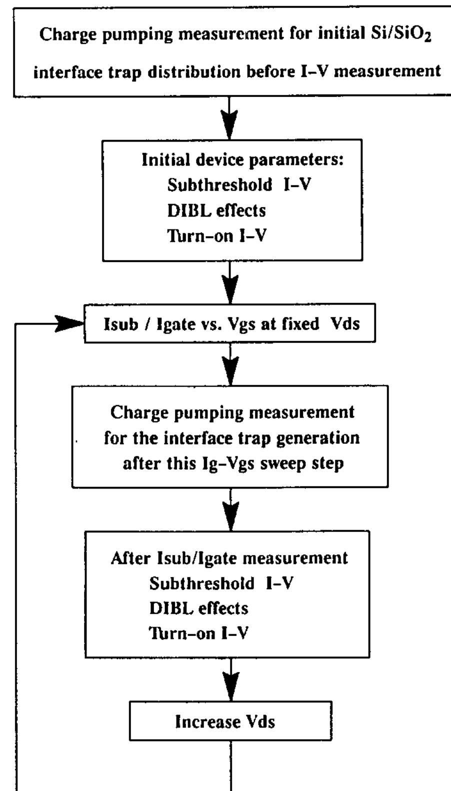

Fig. 3. The experimental procedure for characterizing the I–V curves, charge pumping current, and device degradation.

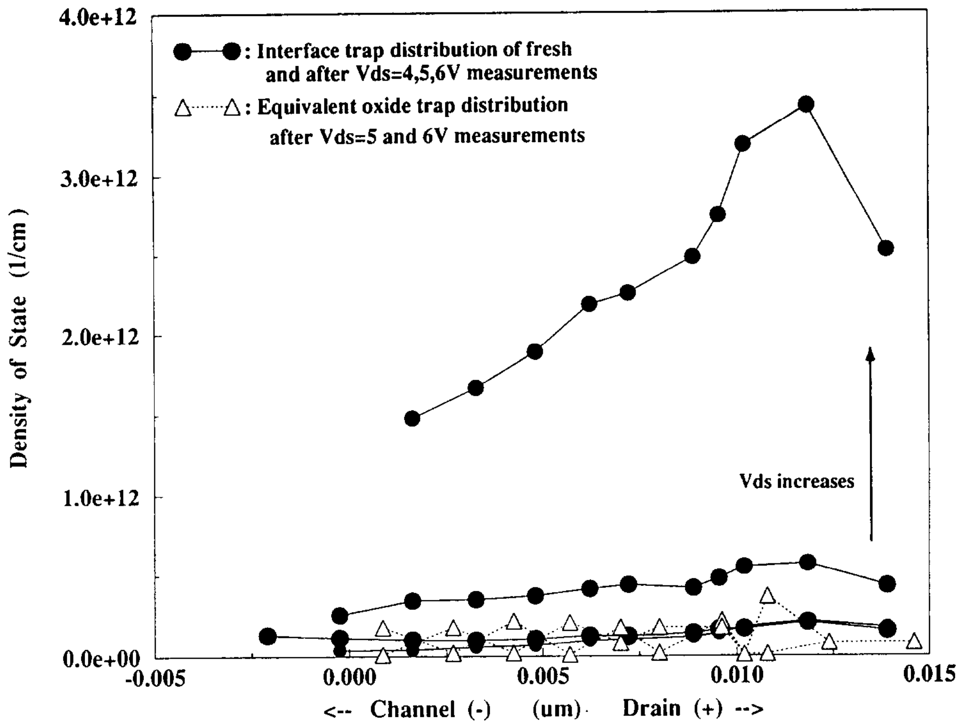

Fig. 4. The spatial distribution of Si/SiO_2 interface traps and oxide traps extracted from the charge pumping current.

Comparisons of the simulated drain, substrate and gate currents for the test device are shown in Fig. 5. It is clearly shown that the simulated drain and substrate currents match experimental data very well. This reveals that the device parameters and the impact-ionization-generated electron–hole pairs have been accurately extracted. It is known that the presence of interface trapped electrons will enhance the

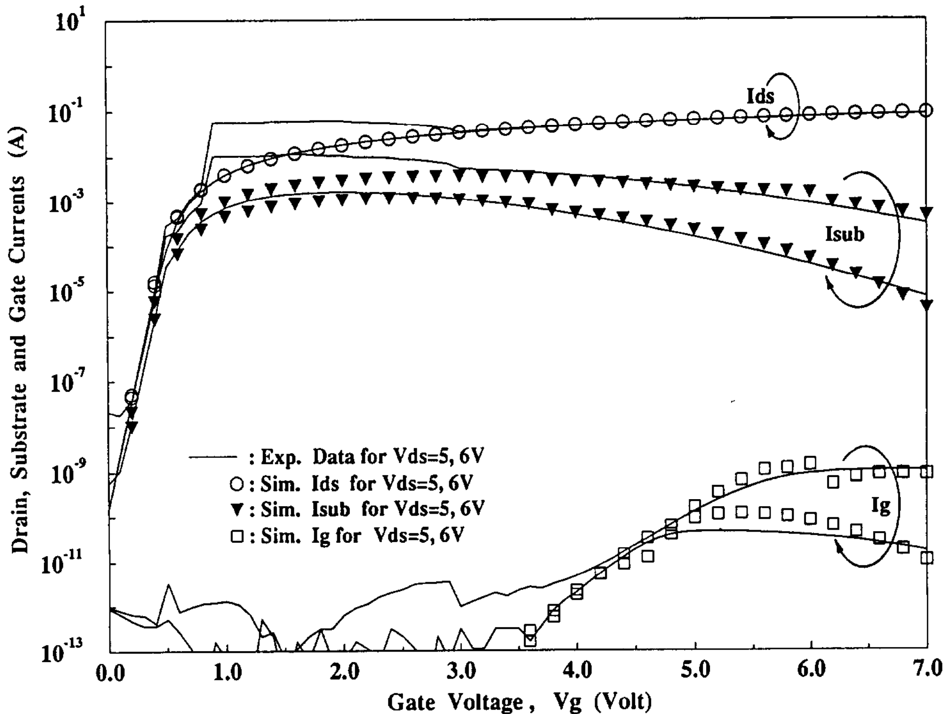

Fig. 5. Comparisons of calculated drain, substrate, and gate currents with experimental data for a conventional n-MOSFET with $L_{eff} = 0.45\ \mu m$, $W = 100\ \mu m$, $T_{ox} = 100$ Å, and $V_{bs} = 0V$.

impact ionization event and degrade the vertical field[18], the injection source of gate current is increased but the injection probability is decreased and both these two effects influence the gate current exponentially. Therefore, any deviation will make an order of magnitude change in the simulated gate current. Figure 5 demonstrates that our modeling can accurately characterize the hot-carrier injection and interface-trap generation effects. The fitting parameter γ in eqn (4) is $3.8 \times 10^{-6} e$ (cm), the capture

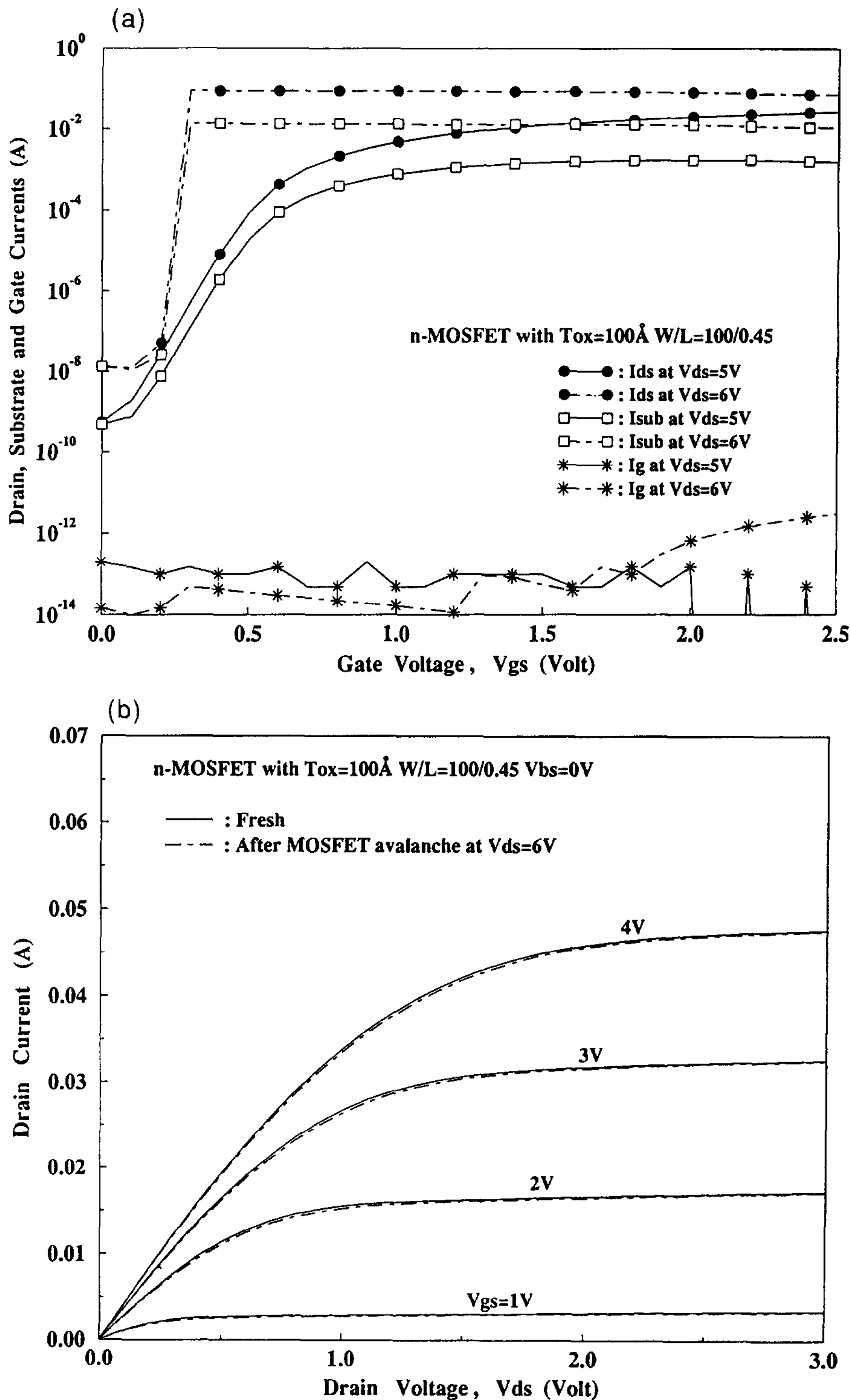

Fig. 6. Experimental results of (a) drain, substrate and gate current when the avalanche occurs; (b) output characteristics before and after the avalanche event.

cross-section σ in eqn (8) is $1 \times 10^{-17}\,cm^2$, and the effective trap level is determined to be 0.04 eV below the conduction band. Our developed model considering the impact ionization, injection probability, and trapping effects, has been verified to accurately simulate the drain, substrate and gate currents simultaneously. Note that the abrupt increase of experimental data shown in Fig. 5 at low V_{gs} and high V_{ds} is due to the avalanche phenomenon, which is beyond the focus point of this paper. However, one will doubt that the Si/SiO_2 interface traps may be generated by the avalanche-induced hot carriers. We repeat the measurement procedures described in Fig. 3 except that the gate bias is only swept to $V_{gs} = 2.5$ V. At this bias condition, avalanche occurs at $V_{ds} = 6$ V and $V_{gs} \simeq 0.5$ V where the drain and substrate currents increase dramatically to the current limit of HP4145 but the corresponding gate current is negligible, as shown in Fig. 6(a). The on I–V characteristics before and after avalanche event are illustrated in Fig. 6(b) and no apparent degradation has been observed. Therefore, the Si/SiO_2 interface-trap generation considered to fit the experimental data shown in Fig. 5 is only due to the gate injection process.

To verify the quantity of Si/SiO_2 interface-trap generation calculated by our model, comparisons with those measured by the charge pumping technique have been made. Figure 7 shows the simulated Si/SiO_2 interface-trap distribution at the end of I_g–V_{gs} measurement biased at $V_{ds} = 5$ V and $V_{ds} = 6$ V. It is clearly seen that the simulated amount and spatial distribution of Si/SiO_2 interface traps match experimental results very well. The simulated Si/SiO_2 interface-trap distribution can be further checked by comparing the I–V characteristics after the degradation of high-field measurement procedure. Figures 8 and 9 show the I_{ds}–V_{gs} and I_{ds}–V_{ds} curves of the fresh device and those of device after gate current measurement at $V_{ds} = 6$ V, respectively. Quite good agreement between the simulation and experimental results once more reveals the accuracy of our developed model. Figures 8 and 9 also show the effects of the oxide traps equivalent to the trapped charge density at the Si/SiO_2 interface. It is clearly shown that the oxide traps cause a large I–V shift for MOSFET biased at the subthreshold region, while the interface traps localized near the drain side slightly change the subthreshold swing. The simulated results are consistent with that reported by Schwerin *et al.*[18], in which they had reported how to discriminate the generated Si/SiO_2 interface traps from oxide traps using the I–V measurement. Therefore, the degradation during the gate current measurement process is mainly due to the generated Si/SiO_2 interface traps.

4. CONCLUSIONS

A simple and accurate simulation technique for the gate current of short channel n-MOSFETs has been developed, in which the 1D substrate injection probability has been modified by considering the channel hot-carrier-enhanced injection probability. The enhanced factor is modeled in terms of an effective barrier lowering term which is proportional to the lateral electric field along the current path. Moreover,

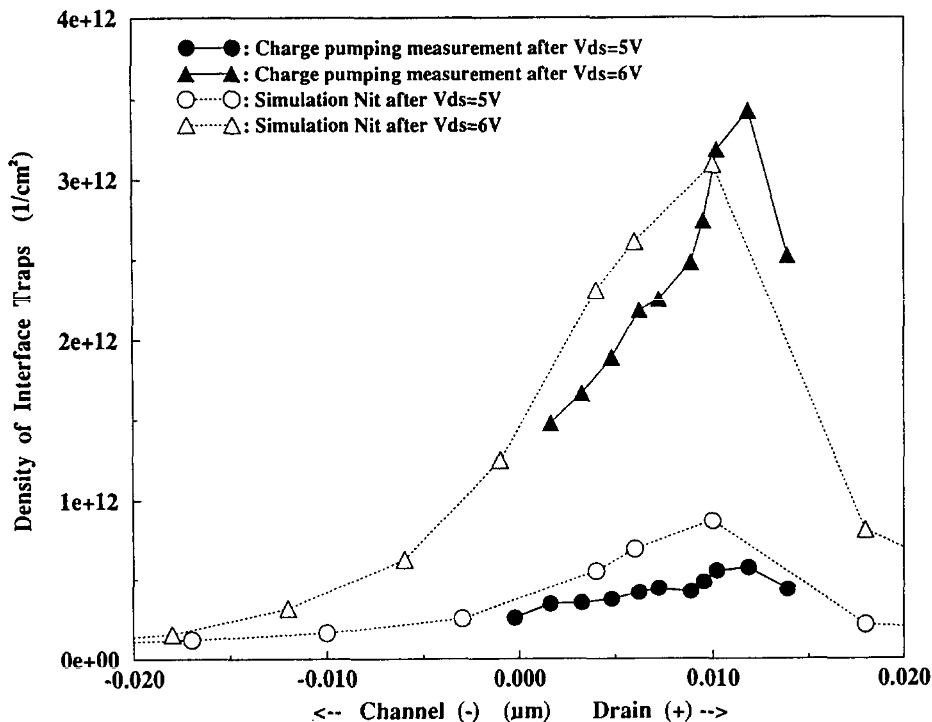

Fig. 7. Comparisons between the simulated and experimental results of Si/SiO_2 interface-trap generation.

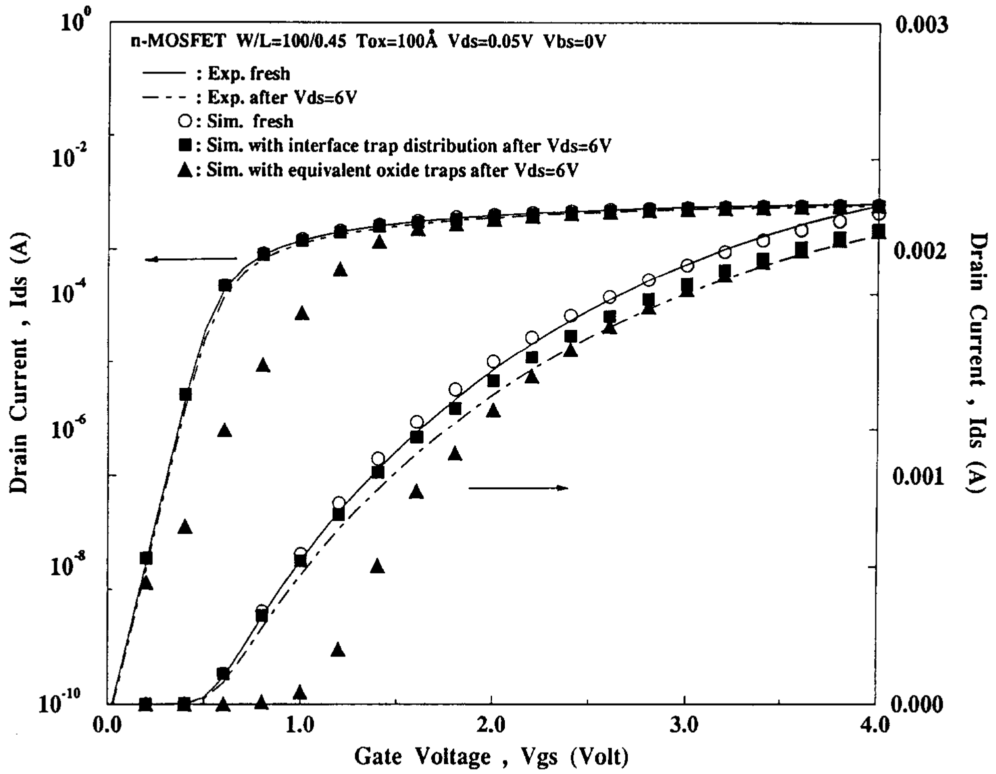

Fig. 8. The simulated and experimental results of linear and subthreshold drain current versus gate voltage before and after gate current measurement at $V_{ds} = 6$ V.

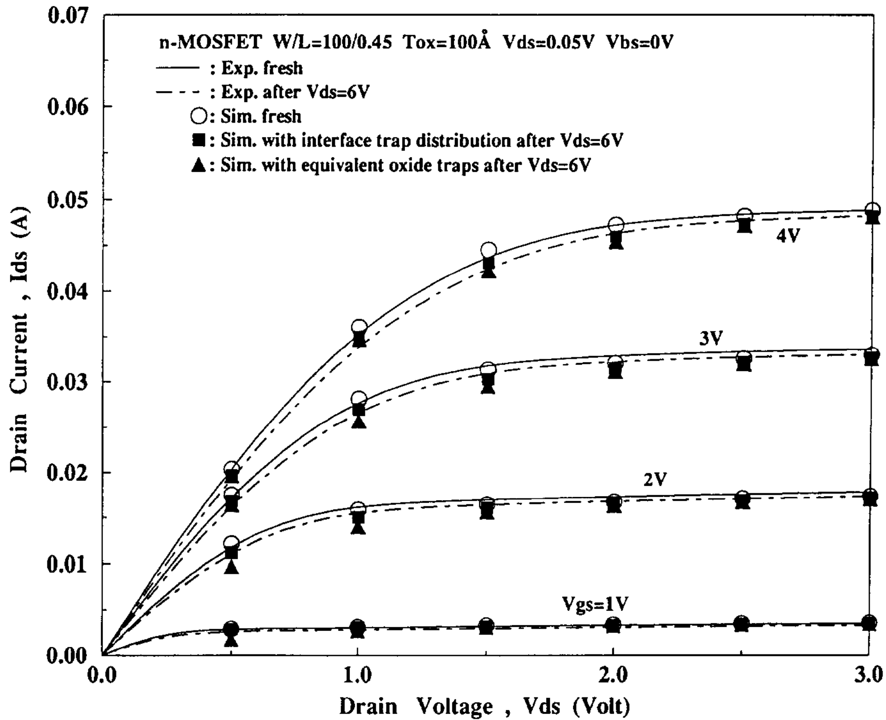

Fig. 9. The simulation and experimental results of drain current vs drain voltage before and after gate current measurement at $V_{ds} = 6$ V.

the Si/SiO_2 interface-trap distribution has been simulated by considering both the hot-electron generation and occupation effects. The deduced Si/SiO_2 interface-trap distribution has been well verified by the charge pumping measurement. Moreover, the degraded $I-V$ characteristics have also been simulated by the extracted distribution of Si/SiO_2 interface traps. Therefore, the proposed simulation technique offers an overall description for the injection and trapping characteristics of hot carriers during the measurement procedure and has been verified to be efficient for gate current calculation.

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