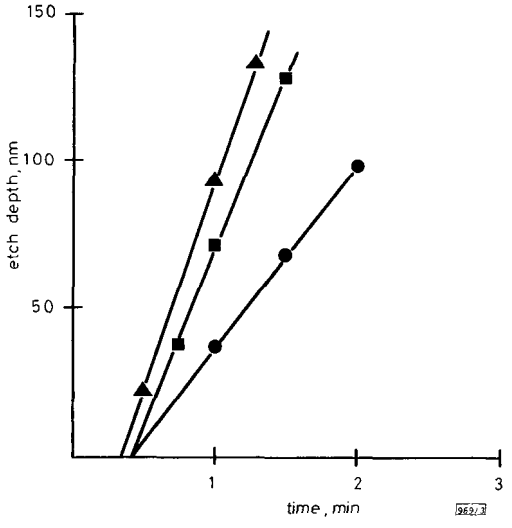

Fig. 3 *$Ta_{36}Si_{14}N_{50}$ etch depth against time with 150mtorr pressure, 40sccm total flow rate, 62.5% O_2 concentration in CHF_3+O_2, for several cathode power densities*

● 0.43W/cm²
■ 0.55W/cm²
▲ 0.66W/cm²

results in the delay increasing back up to 0.8min. The maximum etch rate shown in Fig. 2 at 62.5% O_2 concentration corresponds to minimum delay. Thus, fast removal of $Ta_{36}Si_{14}N_{50}$ also implies fast removal of the surface native oxide. Fig. 3 shows etch rate as a function of time for several power densities at the optimum 62.5% O_2 concentration. Increased power densities result in higher etch rates presumably due to higher production of reactive F species. Increased power densities also tend to give lower time delays due to faster removal of the native oxide as a result of increased chemical etching and/or sputter etching.

Maximum etch rate of $Ta_{36}Si_{14}N_{50}$ in CF_4+O_2 was found to occur for 15% O_2 concentration [4]. The higher O_2 concentrations required to produce maximum $Ta_{36}Si_{14}N_{50}$ etch rate for CHF_3+O_2 mixtures may be due to the greater tendency for plasma polymer formation for CHF_3 than for CF_4 [9]. In general, higher power levels and O_2 concentrations were required for CHF_3 than for CF_4 to achieve comparable etch rates.

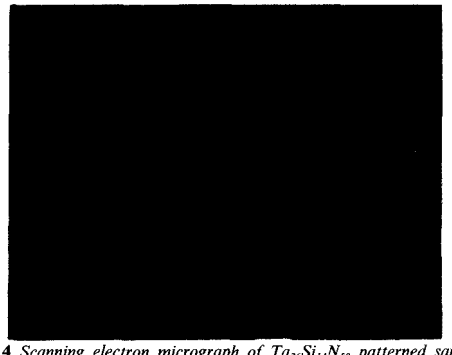

Fig. 4 *Scanning electron micrograph of $Ta_{36}Si_{14}N_{50}$ patterned sample etched with 0.43W/cm² cathode power density, 150mtorr pressure, 40sccm total flow rate, 62.5% O_2 concentration in CHF_3+O_2*

Fig. 4 shows a scanning electron micrograph of a patterned $Ta_{36}Si_{14}N_{50}$ sample etched in CHF_3+O_2. The etched region at the lower left area of the photograph is observed to be about as smooth as the masked region.

In summary, reactive ion etching of $Ta_{36}Si_{14}N_{50}$ diffusion barrier layers was successfully performed in CHF_3+O_2 plasmas. The presence of a native surface oxide results in an initial delay for the commencement of etching. Maximum etch rate is achieved at 62.5% O_2 concentration, which also corresponds to minimum etch delay time.

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Recessed-gate AlGaAs/InGaAs/GaAs pseudormorphic HEMT with Si-planar-doped etch stop layer

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Indexing terms: High electron mobility transistors, Etching

An improved slot etch technique based on an Si planar doped layer has been applied to gate recessing in the fabrication of AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistors (HEMTs). The devices exhibited comparable g_m with much better breakdown and leakage behaviour than conventional pseudomorphic HEMT devices.

As a class of field effect transistor (FET), high electron mobility transistors (HEMT) are of great interest due to their high speed and high frequency applications [1]. To date, many HEMT products have been developed which use the GaAs/AlGaAS material system. To improve HEMT performance and obtain higher frequencies of operation, an InGaAs channel with higher electron velocity can be used [2]. Many pseudomorphic and lattice-matched structures with superior transport properties have been investigated [3, 4].

To enable the device to withstand higher overshoot voltage, and experience less gate leakage, gate recess etching is a critical step in the fabrication of FETs. Many improvements, such as the selective wet/dry etch and directional etch techniques, have been developed [5, 6]. In this Letter we introduce one Si planar doped layer as the

recess-controlled layer and demonstrate that a high performance InGaAs FET can be fabricated using this method.

Our pseudomorphic structure consists of a 400Å (Si)GaAs cap layer ($N_d = 3 \times 10^{18}cm^{-3}$), 50Å $Al_{0.3}Ga_{0.7}As$, (upper) planar doped Si layer ($8 \times 10^{12}cm^{-2}$), 300Å $Al_{0.3}Ga_{0.7}As$, (lower) planar doped Si layer ($1.7 \times 10^{13}cm^{-2}$), 60Å $Al_{0.3}Ga_{0.7}As$, 150Å $In_{0.15}Ga_{0.85}As$, and a 0.5μm GaAs buffer layer. The device layers are grown on a semi-insulating (100) GaAs substrate in an MBE system (RLBER 32P). The mobility determined from Hall measurement is $1900cm^2/Vs$ and $2900cm^2/Vs$ at 300 and 77K, respectively.

We begin device fabrication with a mesa etch, followed by AuGe/Ni/Au ohmic contact deposition, patterning, and furnace annealing at 460°C for 3min in a hydrogen environment. Specific contact resistance and the overall sheet resistance were determined to be $7\pm2 \times 10^{-7}\Omega cm^2$ and $3.4\pm0.2\ \Omega/\mu m$ using the transmission line method (TLM) [7]. After gate photolithography, the cap layer and AlGaAs layer are removed with 2:1:300 $NH_4OH:H_2O_2:H_2O$ etchant with an estimated etching rate of 2.8Å/s. This etch is stopped when it meets the Si planar doped plane. After the 3min slot etch, the Si planar doped plane was removed with 1:10 $NH_4F:H_2O$ etchant in 8s, followed by 2:1:300 $NH_4OH:H_2O_2:H_2O$ etchant to ensure an enhancement mode device. The gate structure was completed with the gate metal (Al) deposition followed by the lift-off technique. Chromium-gold (Cr-Au) deposition was used to complete the interconnection layer.

The device TLM measurements were carried out using an HP 3457A multimeter. The device DC properties were measured with an HP41450. The microwave S-parameter measurements were performed from 0.45 to 26.5GHz with CASCADE microwave wafer probes and an HP 8510 automatic network analyser.

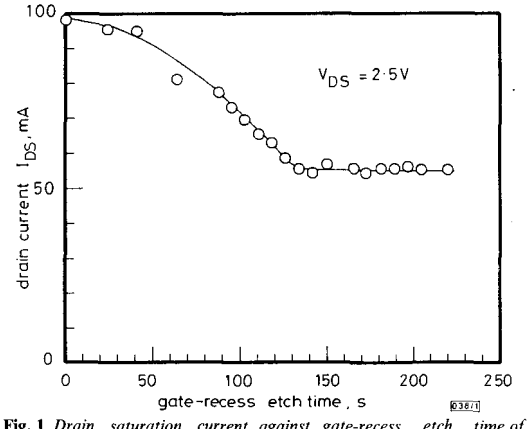

Fig. 1 *Drain saturation current against gate-recess etch time of 'fat' device*

L_g = 50mm, W_g = 200mm

Fig. 1 shows the saturation current as a function of gate recess etch time during recessing of the 'fat' device with 50μm gate length (L_g), 200μm gate width (W_g) and 2.5μm gate to drain/source spacing. After the saturation current reaches a stable value (around 55mA in this Figure), we believe that it reaches the Si planar-doped plane. Thus, the Si planar-doped layer acts as an etch stop layer with respect to this etchant. The remaining etching causes slot (sidewall) etching to the drain and source sides. This etching process, like anisotropic etching, will increase the sidewall etch distance.

Fig. 2 shows the typical device drain current (I_{DS}) against drain-source voltage (V_{DS}) of our pseudomorphic HEMT device with L_g = 0.9μm and W_g = 50μm. The distance between the gate and drain/source is 1.5/1.2μm. The drain-source breakdown voltage (BV_{DS}, defined at 10% of maximum I_{DS}) above 8.5V can be observed. This result is comparable to around 6V of the device without the upper Si planar doped layer processed as a control experiment using the same etchant. The measured extrinsic transconductance (g_m) as a function of gate bias is shown in Fig. 3, with a maximum transconductance of over 400mS/mm and maximum I_{DS} of 380mA/mm. It is also comparable to 350mS/mm (g_m) and 280mA/mm (maximum I_{DS}) of the device without the upper

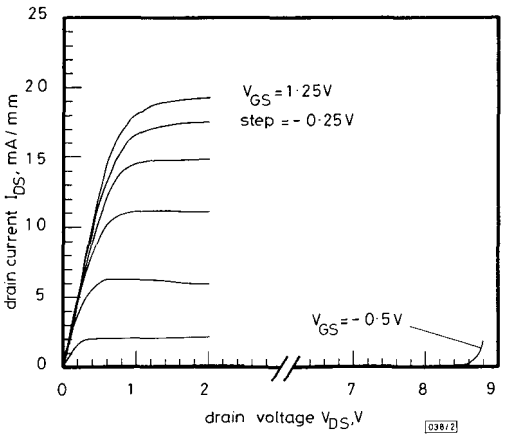

Fig. 2 *Current-voltage characteristics (I_{DS} against V_{DS}) of Si-doped planar doped InGaAs HEMT with V_{GS} = −0.25V/step of the 0.9μm gate length device*

Si-planar doped layer. The gate-drain/source reverse bias current was also reduced (<10μA at −7V), which is an expected result due to the minor DX centres of the undoped high energy gap material ($Al_{0.3}Ga_{0.7}As$) [8].

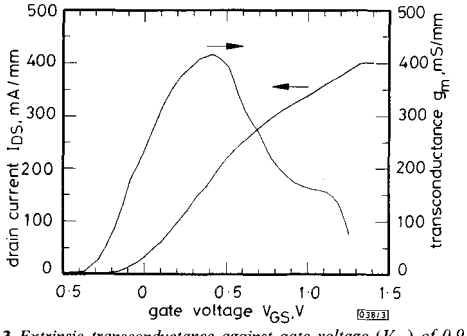

Fig. 3 *Extrinsic transconductance against gate voltage (V_{GS}) of 0.9μm gate length device at 300K*

In summary, we have presented a method for fabricating pseudomorphic InGaAs HEMTs with Si planar doped layer to control the slot etch. High performances with high transconductance and low leakage current and high breakdown voltage can be achieved. This introduced Si planar-doped layer with high effective carrier concentration also reduces the specific contact resistance. The cut-off frequency as high as 34GHz for the 0.9μm gate length device shows that a high performance HEMT can be made using this proposed slot etching technique.

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Fuzzy control of power converters based on quasilinear modelling

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Indexing terms: Fuzzy control, Power convertors

Unlike feedback control by the fuzzy PID method, a new fuzzy control algorithm based on quasilinear modelling of the DC-DC converter is proposed. Investigation is carried out using a buck-boost converter. Simulation results demonstrated that the converter can be regulated with improved performance even whaen subjected to input disturbance and load variation.

Introduction: Switching DC-DC converters are highly nonlinear and time-varying in nature. Most controller designs are based on a linearised model with perturbation around a fixed steady-state operating point [1, 2]. A quasilinear model [3] which does not assume a fixed operating point considers the operating point as a function of the input signal. This model can describe a nonlinear system with better accuracy, and even be subjected to great disturbance. The proposed fuzzy quasilinear controller (FQLC) is based on this accurate model together with the state feedback method.

Quasilinear modelling and control: A DC-DC converter can be represented in the discrete-time domain using the following difference equation:

$$x_{n+1} = \Phi x_n + \Psi e_n \tag{1}$$

where $x = [v_c\ i_L]^T$ is the state vector, e is the input voltage, and $\Phi \in R^{2\times2}$ and $\Psi \in R^2$ are the state transition matrices. With the assumption that the DC-DC converter can reach its steady-state operating point, (X, E, D), the converter's state variables will vary about its operating point and the dynamics of this system can be approximated by the following Taylor expansion:

$$\Delta x_{n+1} \simeq \left.\frac{\partial x_{n+1}}{\partial x_n}\right|_{x_n=X} \Delta x_n + \left.\frac{\partial x_{n+1}}{\partial e_n}\right|_{e_n=E} \Delta e_n + \left.\frac{\partial x_{n+1}}{\partial d}\right|_{d=D} \Delta D \tag{2}$$

The state vector x_{n+1} is a function of x_n, e_n and d. The following state equation can accurately describe the system only if Δx_n, Δe_n and Δd are small:

$$\Delta x_{n+1} = \Phi(D)\Delta x_n + [\Phi'(D)X + \Psi'(D)E]\Delta d + \Psi(D)\Delta e_n \tag{3}$$

Quasilinear modelling does not assume Δe_n to be a small quantity. Any variation of input signal e will affect the operating point (x_{op}, d_{op}) if the output is to be regulated to follow a reference voltage V_{ref}. The above equation is simplified into

$$\Delta x_{n+1} = \Phi(d_{op})\Delta x_n + \Gamma(d_{op}, x_{op}, e)\Delta d \tag{4}$$

where $\Gamma(d_{op}, x_{op}, e) = \Phi'(d_{op})x_{op} + \Psi'(x_{op})e$. The state feedback control law, $\Delta d = K\Delta x_n$, is used to reduce eqn. 4 into the following state equation:

$$\Delta x_{n+1} = [\Phi(d_{op}) + \Gamma(d_{op}, x_{op}, e)K(e)]\Delta x_n \tag{5}$$

With the controller based on pole assignment and the desired poles of λ_1 and λ_2 being considered, the appropriate feedback coefficients can be evaluated to be:

$$k_1 = \frac{(\lambda_1+\lambda_2-\phi_{11}-\phi_{22})(\gamma_2\phi_{11}-\gamma_1\phi_{21})-\gamma_2(\lambda_1\lambda_2+\phi_{12}\phi_{21}-\phi_{11}\phi_{22})}{\lambda_1\lambda_2(\phi_{11}-\phi_{22})-\lambda_1^2\phi_{21}+\lambda_2^2\phi_{12}} \tag{6}$$

$$k_2 = \frac{-(\lambda_1+\lambda_2-\phi_{11}-\phi_{22})(\gamma_1\phi_{22}-\gamma_1\phi_{12})-\gamma_1(\lambda_1\lambda_2+\phi_{12}\phi_{21}-\phi_{11}\phi_{22})}{\lambda_1\lambda_2(\phi_{11}-\phi_{22})-\lambda_1^2\phi_{21}+\lambda_2^2\phi_{12}} \tag{7}$$

Fuzzy quasilinear control algorithm: In the design of the fuzzy control algorithm, the input linguistic variable Δe is considered. The universe of discourse is ΔE and the corresponding fuzzy term sets are ΔE_1 to ΔE_n. The membership function μ is a mapping $\mu_{\Delta E_i}: \Delta e \rightarrow [0,1] | \Delta e \in \Delta E$, where 1 represents full membership and 0 represents no membership to any fuzzy term set ΔE_i. The proposed FQLC contains a feedforward path to continuously monitor any disturbance of input voltage, relocates the operating point and modifies the feedback gains k_1 and k_2 accordingly. The usual inference process is adopted. The following fuzzy relation and the composition rule of inference are used:

$$\mu_R(\Delta e, \Delta k) = \max_{i\,j}(\min(\mu_{\Delta E_i}(\Delta e), \mu_{\Delta K_j}(\Delta k))) \tag{8}$$

$$\mu_{\Delta K}(\Delta k) = \max_{\Delta e}(\min(\mu_{\Delta E}(\Delta e), \mu_R(\Delta e, \Delta k)) \tag{9}$$

All the output fuzzy term sets are summed to form a resultant output set and defuzzified into a crisp value best representing the output set to produce a real control action. In the design here, a centre of gravity method is used for defuzzification and the control output is determined by the following formula:

$$\Delta k^* = \frac{\sum_{i=1}^{n_k} \Delta k_i \mu_{\Delta K}(\Delta k_i)}{\sum_{i=1}^{n_k} \mu_{\Delta K}(\Delta k_i)} \tag{10}$$

By tuning feedback gains heuristically, steady-state error can be eliminated and a good dynamic response can be obtained.

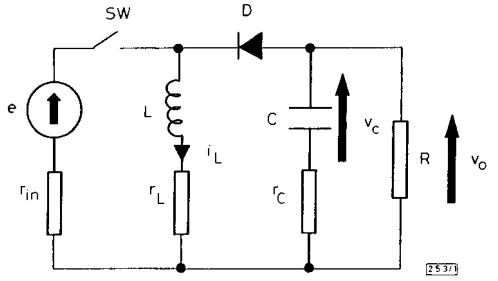

Fig. 1 *Schematic diagram of buck-boost converter*

Simulation results: The Runge-Kutta fourth-order method is used to solve the three sets of differential equations according to the state conditions of the buck-boost circuit. These conditions are: (a) switch ON, diode OFF; (b) switch OFF, diode ON; (c) switch OFF, diode OFF. The converter under consideration is shown in Fig. 1 and has a nominal output voltage V_{ref} = 30V, input resistance r_{in} = 0.2Ω, nominal input voltage E = 20V, switching frequency f = 5kHz, load resistance R = 20Ω, capacitance C = 1.45mF with parasitic resistance r_C = 1.18Ω and inductance L = 0.42mH with parasitic resistance r_L = 0.07Ω. The transient response of the converter is studied under the following conditions: (i) nominal input voltage superimposed by a 10 V peak-to-peak sinusiodal signal; (ii) a step load change from 20Ω to 10Ω at time = 50.5ms.

For the quasilinear design, the desired eigenvalues chosen are 0.7 and 0.95. For the FQLC design, the nominal feedback coefficients of $k_{1,n}$ = –0.0400 and $k_{2,n}$ = 0.0032 are used with $\Delta e = e–E$, $\Delta k_1 = k_1–k_{1,n}$ and $\Delta k_2 = k_2–k_{2,n}$. After optimisation, the linguistic rules are tabulated in Table 1.