A New Switch-Current Integration Readout Structure for Infrared Focal Plane Array

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ABSTRACT

A new current readout structure for the infrared (IR) focal-plane-array (FPA), called the switch-current integration (SCI) structure is proposed and analyzed. It is found that the proposed SCI readout structure can achieve a good readout performance in a small pixel size. It is clearly shown through the analysis that the proposed SCI readout structure and the associated design technique can be applied to the high density and high performance readout circuit design. The high injection efficiency, good detector bias, high detectivity, and large storage capacity readout performances are achieved in a 50x50 μm^2 pixel size.

Keywords: IR focal plane arrays, infrared imaging, readouts, integrated circuit, switch-current integration

1. INTRODUCTION

In the design of the infrared (IR) focal-plane-array (FPA), high resolution has become a common requirement in many applications. This leads to large array sizes and small pixels. The small pixel size usually limits the readout input circuit complexity and, what is affected directly, the readout performance as well. Thus it is difficult to implement complex readout input circuits like buffered direct injection (BDI)[1][2], capacitive transimpedance amplifier (CTIA)[3][4], and chopper-stabilized input circuit (CSI)[5] where a large integrating capacitor has to be implemented in a small pixel size. Moreover, the strict constraints on the unit-cell power dissipation and pixel size also increase the difficulty to achieve the good readout performance in the large format IR FPA.

In this paper, a new current readout structure for the IR FPA, called the switch-current integration (SCI) structure is proposed. It can achieve a good readout performance in a small pixel size by using switch-current-integration technique, off-focal plane integration capacitors, and the previously proposed share-buffered direct injection (SBDI) input circuit.[6] The design and performance evaluation of the SCI readout circuit are also described in this paper. The SPICE simulation results are present and a conclusion is given finally.

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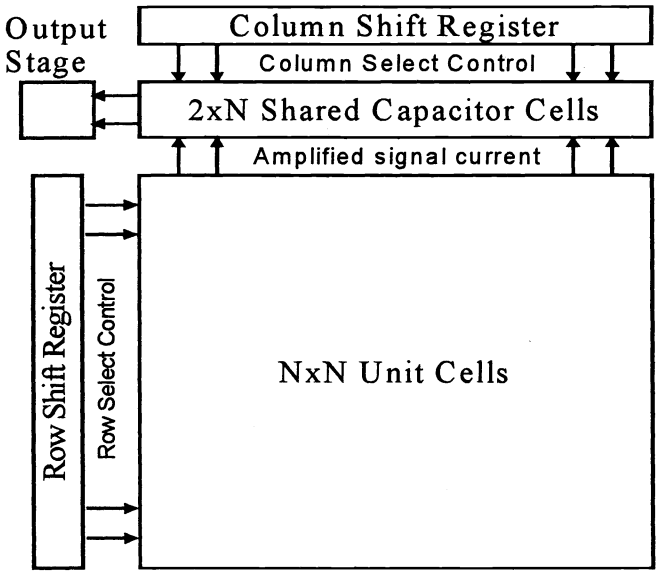

Fig. 1. The block diagram of the SCI readout chip

2. SWITCH-CURRENT INTEGRATION READOUT STRUCTURE

The SCI readout structure is composed of three parts: the unit cell input stage, the off-focal plane integration capacitor array and the common output stage as shown in Fig. 1. The unit cell input stage is achieved by a previously proposed SBDI circuit and a cascode current mirror. The SBDI input circuit support a high injection efficiency, good detector bias stability, low noise, good threshold uniformity, low power dissipation, and small-size input stage. The signal photocurrent is mirrored to the select switch and a current gain is introduced by the current mirror to improve the detection sensitivity and noise coupling effect to input stage. In the design of the SCI input stage, a high-swing cascode current mirror is used to increase the output impedance and current accuracy.[7] As shown in Fig. 2. the cascode current mirror is composed of Q1 to Q4. The current ratio of i_O to i_I is [8]

$$\frac{i_O}{i_I}=\left(\frac{L_1W_2}{W_1L_2}\right)\left(\frac{V_{GS}-V_{T2}}{V_{GS}-V_{T1}}\right)^2\left(\frac{1+\lambda\upsilon_{DS2}}{1+\lambda\upsilon_{DS1}}\right)\left(\frac{\mu_{o2}C_{ox2}}{\mu_{o1}C_{ox1}}\right) \tag{1}$$

Where i_I is the current of the branch Q1~Q2 and i_O is that of the slave branch Q3~Q4. The physical parameters such as V_T, μ_o, C_{ox}, etc. are identical for both devices. As a result, Eq. (1) simplifies to

$$\frac{i_O}{i_I}=\left(\frac{L_1W_2}{W_1L_2}\right)\left(\frac{1+\lambda\upsilon_{DS2}}{1+\lambda\upsilon_{DS1}}\right) \tag{2}$$

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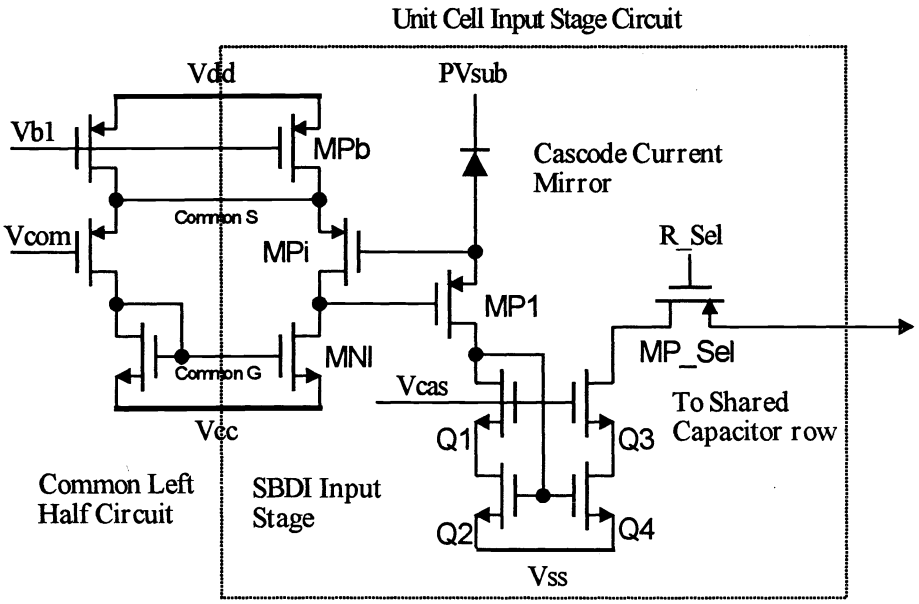

Fig. 2. The unit cell circuit of the SCI readout structure with SBDI input stage.

The channel modulation effect factor λ can be small by using a long channel device. Then, the ratio of i_O/i_I becomes

$$\frac{i_O}{i_I}=\left(\frac{L_1W_2}{W_1L_2}\right) \tag{3}$$

by ignoring the small factor λ. It is shown that the gain factor can be implemented by the dimension ratio of the MOS devices Q4/Q2 in the current mirror. Through the slave current mirror, the amplified current signal is switched through MP_Sel and *R_Sel* to the shared off-focal plane capacitor row and integrated. The shared off-focal plane capacitor cell is composed of the integration capacitor C_{int}, reset device Mres, and anti-blooming control device Mant as shown in Fig. 3. There are two shared capacitor row in the SCI readout structure for even-odd selecting. When the integrated odd-cell's voltage signal of the first capacitor row is sampled to the common output stage, the even-cell's current signal is integrated in the second capacitor row The maximum integration time is limited to one row processing time because one off-focal plane integration capacitor is shared by one column. Under this time limit, a high detection sensitivity can still be achieved by designing a proper current gain at the cascode current mirror. The charge storage capacity is enlarged by designing a large off-focal plane integration capacitors without increasing the pixel size limit. Since only a simple cascode current mirror and the SBDI input stage are included in the SCI circuit, the unit call size can b small and the good readout performance in the high resolution large format IR FPA can be achieved.

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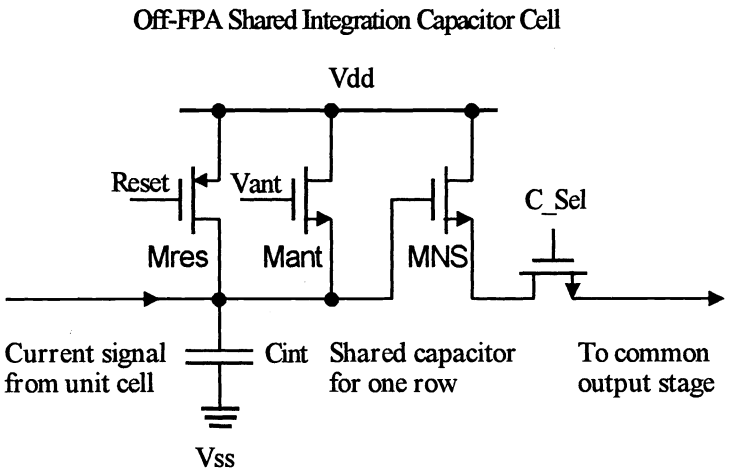

Fig. 3. The off-focal plane shared integration capacitor cell of the SCI readout.

The integrated voltage signals of the two capacitor rows are sampled to the common output stage alternately through the N-type source-follower after a integration internal, that is, one row processing time. In the commonoutput stage as shown in Fig. 4., clamping function is achieved by the clamp device Mclp, AC coupling capacitor C_{AC}, and the current load MNC for the multiplexing source-follower tree. When sample clock *C-Sel* is high, assuming the time is T_1, the clamp device Q is ON and the sampled signal is charged on the AC coupling capacitor C_{AC}. As shown in Fig. 4., the voltages of $V_1(T_1)$ and $V_2(T_1)$ are

$$V_1(T_1) = V_i - V_T \ , \ V_2(T_1) = 0 \tag{4a}$$

$$V_i = V_{dd} - V_{\text{int}} \tag{4b}$$

where V_{int} is the integrated signal on the capacitor and V_T is the threshold voltage drop of the N-type source-follower. The clamp device Mclp turns OFF just prior to the internal reset at time T_2. Then the voltage $V_1(T_2)$ is

$$V_1(T_2) = V_{dd} - V_T \tag{5}$$

since the integration capacitor is reset to V_{dd}. Because the charge on the AC coupling capacitor C_{AC} is the same at time T1 and T2. From Eqs. (4) and (5), they give

$$C_{AC}\left[V_1(T_1) - V_2(T_1)\right] = C_{AC}\left[V_1(T_2) - V_2(T_2)\right] \tag{6}$$

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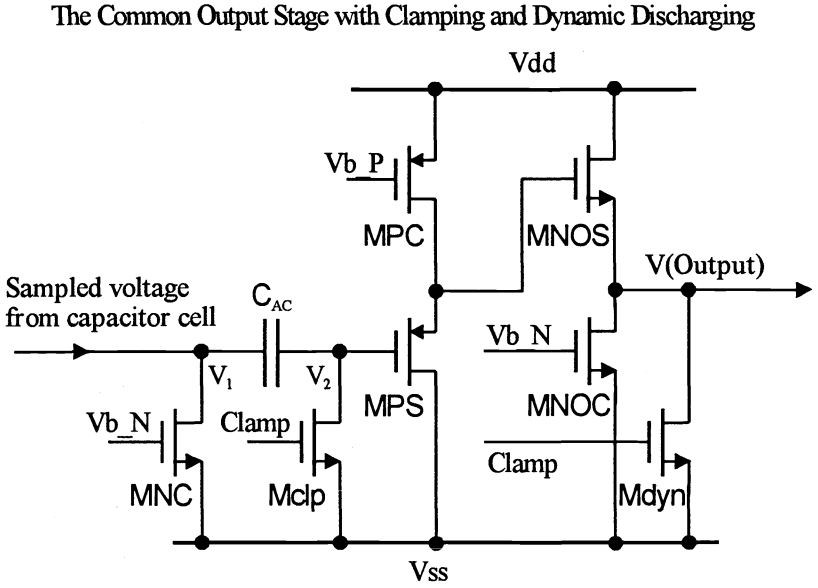

Fig. 4. The common output stage of the SCI readout with clamping and dynamic discharging functions.

Then the output signal V2(T2) after clamping function is

$$V_2(T_2) = V_{dd} - V_i = V_{\text{int}} \tag{7}$$

and the difference voltage is coupled through to the output buffer stage. This eliminates the fixed pattern noise and 1/f noise in the multiplexing tree. The output buffer stage is achieved by the P-type and N-type cascaded source-followers. A dynamic discharging device is also included to save the static power dissipation and maintain the proper readout speed.

3. SIMULATION RESULTS

The SPICE simulation results of the current readout in the SCI with the input signals 5nA, 15nA, 25nA, 35nA, and 45nA are shown in Fig. 5. and 6. The discharging waveform with different input signal is shown in Fig. 5. The minimum discharging voltage control by the gate Mant can reach 2V at the 8V power supply. The output waveform of the shared capacitor cell V(Clamp) and output stage V(Output) are shown in Fig. 6. The clamping and dynamic discharging function can be observed. The readout speed can reach 1MHz under 10mW power dissipation with 64x64 format.

The SCI readout structure has about 95M high transimpedance and good linearity as shown in Fig. 7. The slope difference between V(Output) and integrated signal V(Cint) is due to the non-unity gain of the source-followers. The simulation performance is summarized in Table. I.

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An experimental 30x30 SCI readout chip is designed and layout by using 0.8μm double-ploy-double-metal (DPDM) CMOS technology. The layout diagram of 30x30 SCI readout chip is shown in Fig. 8. The chip is now under fabrication.

4. CONCLUSIONS

A high performance SCI IR current readout structure has been demonstrated and analyzed. By using the proposed SCI readout structure and associated design technique, the good input stage and large storage capacity can be achieved in a small pixel. The inherent advantages of the low power and small pixel size make it suitable for the application to the high performance readout of the high density large format IR FPA.

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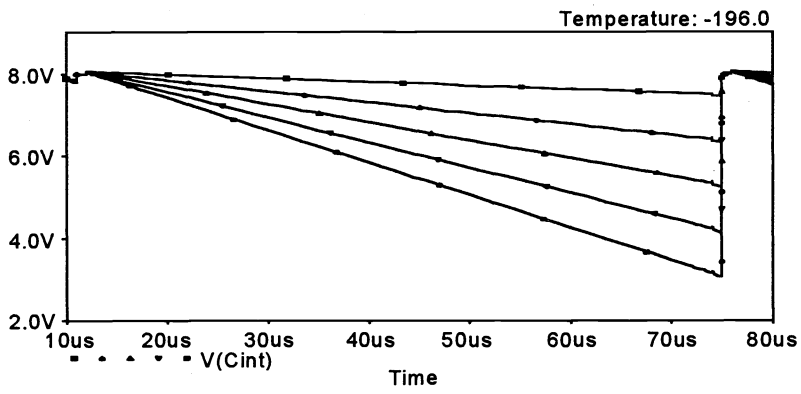

Fig. 5. The discharging waveform of the SCI integrated capacitor Cint with input from 5nA to 45nA and 10nA step.

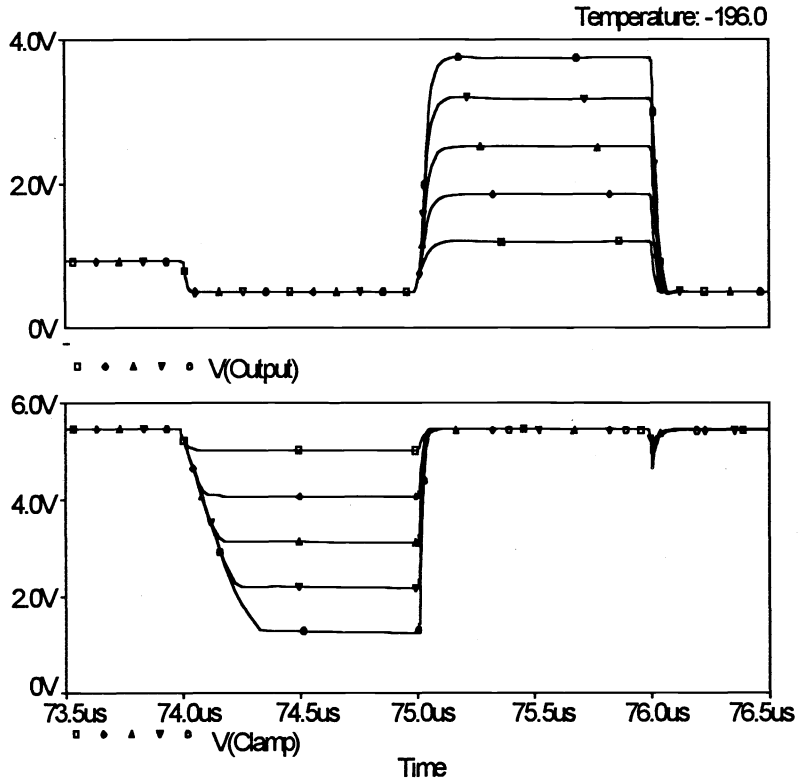

Fig. 6. The output waveform of the SCI capacitor cell V(Clamp) and the common output stage V(Output) with input from 5nA to 45nA and 10nA step.

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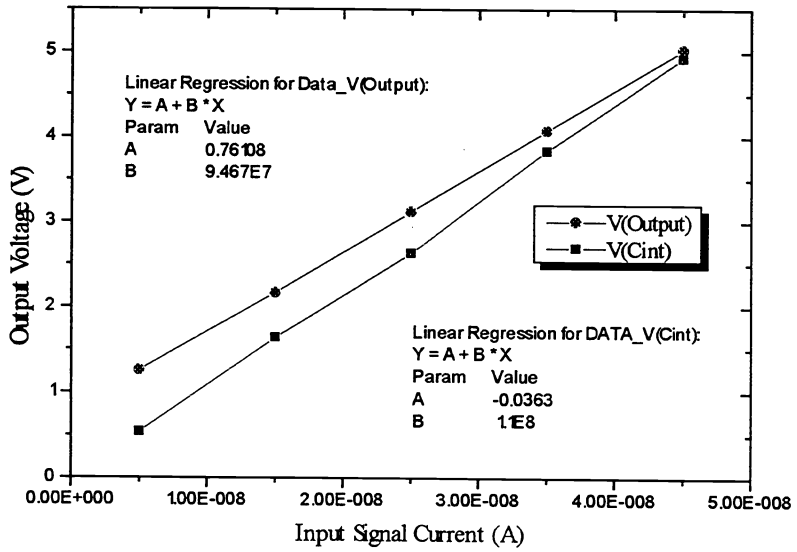

Fig. 7. The linearity and transimpedance of the integrated voltage V(Cint) and the output voltage V(Output)

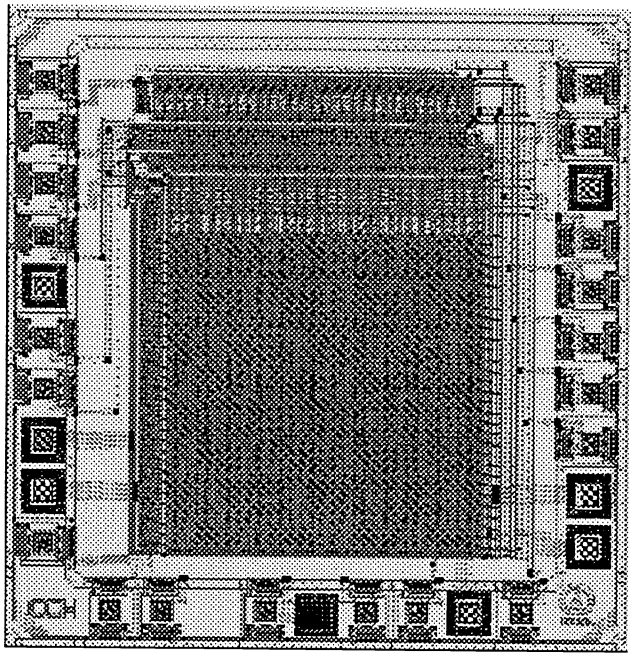

Fig. 8. The 30x30 SCI readout chip layout

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TABLE I.
Simulation Results and Operation conditions for the Switch-Current Integration Readout Structure

Parameter	Results
Power supply	0-4V-8V
Max. Photo-current	50 nA
Max. Readout speed	2 MHz
Integration capacitance	> 2 pF
Storage capacity	$> 6.25 \times 10^7 / e^-$
Transimpedance	> 90 MΩ
Power dissipation	< 10 mW
Linearity	> 99%
Anti-blooming control	yes
Operation temperature	77° k

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