A Unified Approach to Profiling the Lateral Distributions of Both Oxide Charge and Interface States in n-MOSFET's Under Various Bias Stress Conditions

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***Abstract*— A new and accurate technique that allows the simultaneous determination of the spatial distributions of both interface states (N_{it}) and oxide charge $(Q_{\rm ox})$ will be presented. The gated-diode current measurement in combination with the gate-induced drain leakage (GIDL) current were performed to monitor the generation of both N_{it} and $Q_{\rm ox}$ in n-MOSFET's. A special detrapping technique and simple calculations have been developed, from which the spatial distributions of both N_{it} and $Q_{\rm ox}$ under various bias stress conditions, such as the hot-electron stress $(I_{G,\max}), I_{B,\max}$, and hot-hole stresses, can be determined. The calculation of gated-diode current by incorporating the extracted profiles of N_{it} and $Q_{\rm ox}$ has been justified from numerical simulation. Results show very good agreement with the experimental results. The extracted interface damages for hot-electron and hot-hole stresses have very important applications for the study of hot-carrier reliability issues, in particular, on the design of flash EPROM, E^{2}PROM cells since the above stress conditions, such as the $I_{G,\max}$ and hot-hole stress, are the major operating conditions for device programming and erasing, respectively.**

I. Introduction

The HOT CARRIER effect will induce the so-called gate oxide damages, which include the oxide-trapped charge $Q_{\rm ox}$ and interface state N_{it} at the Si-SiO$_2$ interface. In the past, much effort has been spent to characterize the localized distribution of interface states N_{it} near the drain junction [1]–[3]; very few studies have been reported on the spatial distribution of the localized oxide charge $Q_{\rm ox}$.

Previous studies [4]–[6] showed that simultaneous determination of the interface states N_{it} and oxide charge $Q_{\rm ox}$ in MOS devices are rather difficult and not easy to implement. Thus far, only a few papers have reported achievement of this goal. The method by Chen *et al.* [4] used the conventional drain-substrate junction bias method, which will impose unintentional hot-carrier damage during measurement. The numerical method in [5] needs extensive numerical calculation. Both methods can be used to determine both N_{it} and $Q_{\rm ox}$ under a hot electron or a hot-hole stress condition but not for both. In a recent paper by Tsuchiaki *et al.* in [6], only a special case for determining $Q_{\rm ox}$ is dealt with. On the other hand, there are basically three different stressed conditions for hot electron or hot-hole stress, i.e, the maximum substrate current (we call this $I_{B,\max}$ condition), the maximum gate current (we call this $I_{G,\max}$ condition), and hot-hole stress conditions. The above three cases can only be restricted to the special stress conditions such as either hot electron or hot-hole stress. As a consequence, different approaches should be taken to deal with different stress conditions. It is the purpose of this study to find a generalized method that can be used to determine both $Q_{\rm ox}$ and N_{it} for devices stressed under various hot carrier stress biases.

In this work, we will develop a method for profiling both hot-electron-induced and hot-hole-induced interface damages. It is based on an improved gated-diode measurement technique with gate-induced drain leakage (GIDL) current as a monitor and a new characterization algorithm for determining N_{it} and $Q_{\rm ox}$.

In Section II, the experimental devices and stress condition throughout this study will be described. In Section III, the principle of a new method using gated-diode measurement in combination with an algorithm to simultaneously determine N_{it} and $Q_{\rm ox}$ will be demonstrated. The results of spatial distribution of $N_{it}(x)$ and $Q_{\rm ox}(x)$ at various hot carrier stress conditions will be presented and verified in Section IV. Finally, the conclusion of this study is given in Section V.

II. Experimental

The experimental devices used in this work were conventional n-MOS devices. The tested samples have 0.5-μm mask channel length and 20-μm channel width. The gate oxide thickness is 7 nm. The V_T implant is 25 keV, 3×10^{12} cm^{-2} BF$_2$, and the source/drain region was performed by using arsenic implant with an energy of 80 keV and a dose of 5×10^{15} cm^{-2}. The channel profile and source/drain profile have been calibrated against SIMS data. For the hot carrier stress experiment, three different bias stress conditions have been performed. The first one is the hot electron stress at $V_D = 5$ V and $V_G = 5.5$ V, where maximum gate current

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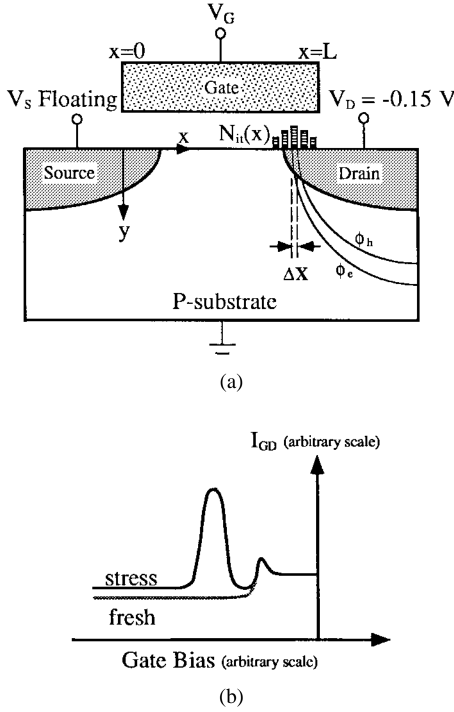

Fig. 1. (a) Schematic diagram of gated-diode current measurement setup, the contours of ϕ_e and ϕ_h at a drain voltage $V_D = -0.15$ V for a forward-biased drain-to-substrate junction are presented. Gate voltages V_G are varied from inversion to strong accumulation. (b) Qualitative expression of the measured gated-diode current $(I_{\rm GD})$ for device before and after the stress.

$(I_{G,\max})$ occurs. The second one is called hot-hole stress or off-state stress at $V_D = 5$ V and $V_G = -4$ V, where the device operates in the off state. The third one is called the $I_{B,\max}$ stress condition at $V_D = 5$ V and $V_G = 2$ V. Gated-diode current and GIDL current measurements have been carried out using the HP 4145B parameter analyzer.

III. Principle of the New Method

The new approach adopts the gated-diode measurement technique in [7] and [8] for N_{it} characterization and with addition of $Q_{\rm ox}$ characterization. The gated-diode current measurement only requires simple dc current measurement and yields better spatial resolution such that this method is more convenient than charge pumping current method. A voltage V_D is applied to the drain to forward-bias the drain-substrate junction, and the current is measured as a function of gate voltage V_G [Fig. 1(a)]. In this work, we use a drain forward-bias of $V_D = -0.15$ V, and the source terminal is left floating to avoid any potential drop along the channel. A typical I–V characteristic measured by gated-diode current measurement is illustrated in Fig. 1 (b), where both currents for a fresh device, and a stressed device can be seen. The difference between these two curves shows the additional recombination caused by the interface state.

According to Shockley–Read–Hall theory [9] and by assuming that $\sigma_n = \sigma_p = \sigma$, the surface component of $I_{\rm GD}$ current is mainly determined by the recombination in the region where the electron and hole concentrations are nearly equal, that is, the surface potential is close to the midgap. During the inversion, the electron concentration is higher than hole concentration at the interface so that interface states do not contribute to the $I_{\rm GD}$ current. The measured current is due to the recombination and diffusion in the p-n junction. When the channel is in the accumulation, the condition $n = p$ is only satisfied in the gate-drain overlap region. Only traps in the narrow band between ϕ_h and ϕ_e [ΔX as shown in Fig. 1(a)] contribute to the recombination current. Further, with decreasing V_G, ΔX moves toward the drain region. The difference $\Delta I_{\rm GD}$ (V_G) between the measured current of devices before and after stress can be used to determine the spatial distribution of N_{it}. The excess recombination current $\Delta I_{\rm GD}$ after the stress can be expressed as [7]

$$\Delta I_{\rm GD}(V_G) = \frac{qW}{2} v_{\rm th}\sigma\Delta N_{it}(x)\Delta x(V_G) n_i \, \exp\left(\frac{q|V_D|}{2\,{\rm kT}}\right) \tag{1}$$

where

W	device channel width;
q	unit charge;
$v_{\rm th}$	thermal velocity;
σ	defect capture cross section;
$\Delta x(V_G)$	current path where recombination current occurred;
n_i	intrinsic carrier concentration.

According to (1), we see that Δx is a function of gate bias V_G. If there are oxide trapped charges $(Q_{\rm ox})$ in the Δx region, they will cause the variation of V_G. Note that the interface states are simultaneously filled with electrons and holes between $q\phi_h$ and $q\phi_e$ such that the recombination current $I_{\rm GD}$ occurs only in this region. In the meantime, the interface states between $q\phi_h$ and $q\phi_e$ are neutral such that these traps do not cause the variation of V_G, whereas oxide trapped charges (either positive or negative) will induce a shift of $Q_{\rm ox}/C_{\rm ox}$. In other words, the value of V_G on the right-hand side of (1) will be replaced by $V_G + qQ_{\rm ox}/C_{\rm ox}$ if there is $Q_{\rm ox}$ present at location of x. In this case, for a stressed device including both N_{it} and $Q_{\rm ox}$, the increment of measured gated-diode current (1) should be modified as

$$\Delta I_{\rm GD}(V_G) = \frac{qW}{2} v_{\rm th}\sigma\Delta N_{it}(x)\Delta x\left(V_G + \frac{qQ_{\rm ox}}{C_{\rm ox}}\right) n_i \cdot \exp\left(\frac{q|V_D|}{2\,{\rm kT}}\right). \tag{2}$$

Here, the measured gated-diode current $\Delta I_{\rm GD}$ is contributed by both N_{it} and $Q_{\rm ox}$.

Based on (2), we will provide a new technique to determine spatial distributions of both N_{it} and $Q_{\rm ox}$ based on the basic gated-diode technique, which can only be used to determine N_{it} distribution. The neutralization (or detrapping) technique and simple numerical calculation are used to determine $Q_{\rm ox}$ distribution. To separate both N_{it} and $Q_{\rm ox}$, the experimental and numerical procedures are illustrated in Fig. 2 and described as follows.

1) Measure the gated-diode $(I_{\rm GD})$ and gate-induced drain leakage $(I_{\rm GIDL})$ currents on a fresh n-MOS device with

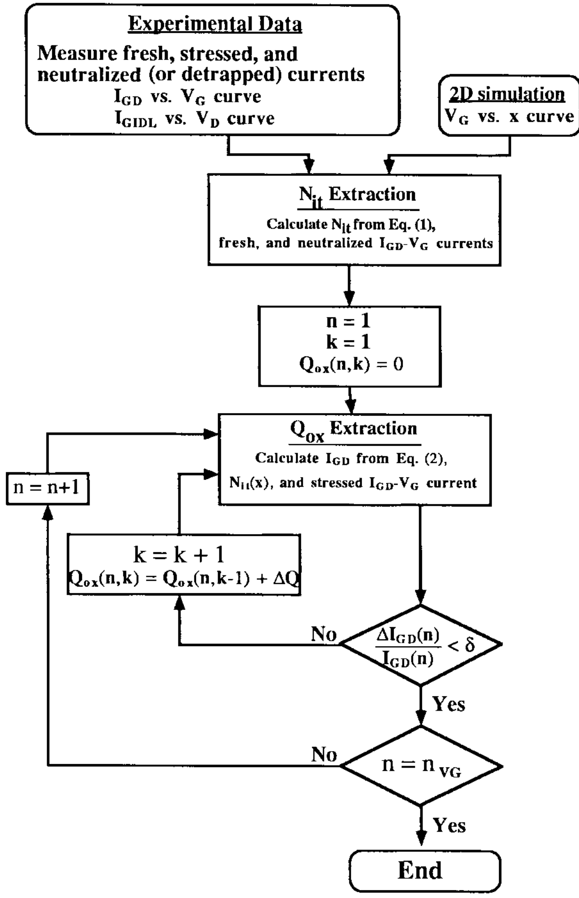

Fig. 2. Flowchart of a new method to characterize the spatial distributions of $N_{it}(x)$ and $Q_{ox}(x)$.

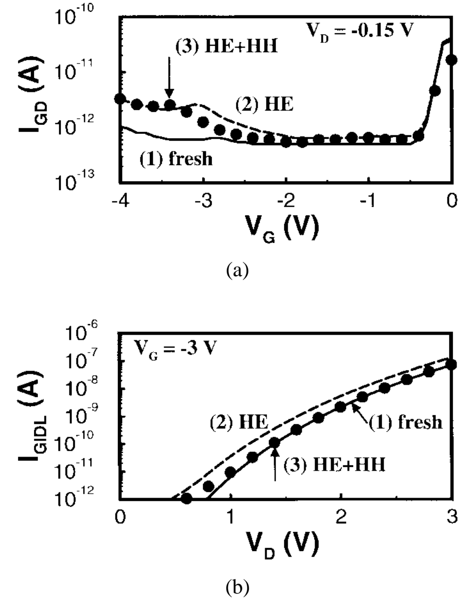

Fig. 3. (a) Measured I_{GD} characteristics of the test device after $I_{G,\max}$ stress at $V_D = 5$ V and $V_G = 5.5$ V. (b) Measured GIDL currents. Curves (1) fresh (solid line); (2) hot electron stress (dashed line); (3) after hot hole detrapping (solid circles).

source floating as shown in Fig. 1. The V_G versus x relationship near the drain junction is established by 2-D numerical simulation.

2) Measure the I_{GD}-V_G and I_{GIDL}-V_D characteristics for devices after the hot-carrier stress.
3) Use a neutralization (or detrapping) step to neutralize (or detrap) the hot-carrier induced Q_{ox}, and ensure that this step does not cause any stress or change N_{it} (which can be verified by inspecting the magnitude of I_{GD}-V_G current).
4) Using the recover current obtained by step 3), we can directly calculate the hot-carrier-induced $N_{it}(x)$ by using (1) and V_G versus the x relationship. (The complete recovery of the oxide charge is verified by the I_{GIDL}-V_D current).
5) The hot-carrier-induced $Q_{ox}(x)$ is obtained from the I_{GD}-V_G curve before and after the neutralization step.

In the flowchart of Fig. 2, the fresh, stressed, and neutralized (or detrapping) I_{GD}-V_G currents can be obtained by the above experimental procedures (1)–(3). Values of δ and ΔQ represent the chosen convergence criterion for iteration and the increment of oxide charge, respectively. In this new method, the $N_{it}(x)$ distribution can be first extracted from the difference between fresh and neutralized (or detrapping) $\Delta I_{GD}(V_G)$ currents by using (1). Then, the $Q_{ox}(x)$ distribution will be determined by comparing the stressed $\Delta I_{GD}(V_G)$ current with the simulated one, which includes the N_{it} and the superimposed Q_{ox} profiles. In this $Q_{ox}(x)$ profiling procedure, there are two iteration loops. The inner loop in the flowchart is to determine the value of oxide charge at a fixed gate voltage. The external loop varies the gate voltage such that we can determine the spatial distribution of oxide charges along the channel direction. n_{VG} is the total number of measured I_{GD}-V_G characteristics. According to this methodology, the profiles of N_{it} and Q_{ox} for devices stressed at various bias conditions, such as off-state, maximum substrate current ($I_{B,\max}$) and the maximum gate current ($I_{G,\max}$), can all be extracted. Details will be discussed in the next section.

IV. Results and Discussion

A. Damage Generation During Hot Electron Stress ($I_{G,\max}$)

Fig. 3 shows the measured I_{GD}-V_G and I_{GIDL}-V_D characteristics. Solid lines are the measured current for fresh devices. Dashed lines are the measured currents after hot electron stress at $V_G = 5$ V and $V_D = 5.5$ V. I_{GD} currents will be used for determining N_{it} and Q_{ox}, whereas I_{GIDL} is used for monitoring the generation of interface state or oxide trapped charge. Under the above stress bias, it will generate not only N_{it} but negative Q_{ox} as well. The peak value of I_{GD}-V_G curve is shifted to a more positive gate voltage region when the negative Q_{ox} exists as shown by dash curve in Fig. 3. To extract the distribution of $N_{it}(x)$, we must neutralize this Q_{ox}, and it was accomplished by hot-hole injection by the band-to-band tunneling (@ $V_D = 3$ V, $V_G = -4.5$ V, for 10 s), as shown by solid circles in Fig. 3. The step for hot-hole injection does not cause any change in fresh I_{GD}-V_G

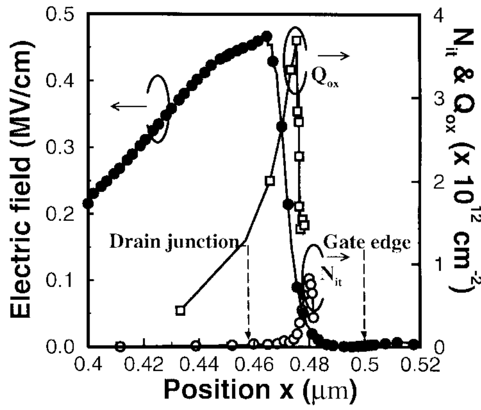

Fig. 4. Extracted spatial distributions of $N_{it}(x), Q_{\rm ox}(x)$ and simulated maximum lateral field for devices with hot electron stress at $I_{G,\max}$.

and $I_{\rm GIDL}$-V_D curves (which are not shown here), and the peak value of $I_{\rm GD}$-V_G curve (solid circles) is shifted to more negative gate voltages, that is, the previous negative charges can be compensated by hot-hole injection. In addition, we may observe from the bottom figure in Fig. 3 that after the hot-hole neutralization step, the GIDL current (solid circles) has been reached to the original current level at large V_D bias (e.g., $V_D > 1.2$ V). This means that the oxide trapped charge has been filled with holes. The gated-diode current ($I_{\rm GD}$) after this neutralization step is given in the top figure of Fig. 3, in which the solid circles give the current with N_{it} only.

From the HE+HH curve (curve 3) and the fresh $I_{\rm GD}$-V_G current (curve 1), $N_{it}(x)$ can be extracted using the above method described in Section III. Once the $N_{it}(x)$ has been extracted, we can easily use curve 3 (solid circles) and curve 2 (dashed lines) in the top figure of Fig. 3 to calculate the negative $Q_{\rm ox}(x)$. The extracted spatial distribution of N_{it} and $Q_{\rm ox}$ are given in Fig. 4, in which the lateral electric field is also shown for comparison. The location of maximum N_{it} and $Q_{\rm ox}$ is several hundred Angstroms away from the location of maximum lateral field (@ $V_D = 5$ V, $V_G = 5.5$ V). Note that the simulated maximum electric field is plotted along the surface direction. We also observed that N_{it} and $Q_{\rm ox}$ is localized in the gate-drain overlap region. Therefore, this result does not change the subthreshold current and is consistent with the experimental results (which are not shown here). To verify the accuracy of this method, the extracted $N_{it}(x)$ and $Q_{\rm ox}(x)$ are put into the simulator to calculate the gated-diode current from (2); we found that the calculated result is in agreement with the experimental result, as shown in Fig. 5(a). The V_G versus x relationship due to the $N_{it}(x)$ and $Q_{\rm ox}(x)$ is also shown in Fig. 5(b), in which the solid curve represents the simulated V_G versus x curve for the fresh device, and the long dash curve represents the V_G versus x curve with N_{it} and $Q_{\rm ox}$. The difference of these two curves at each position x is due to the existence of negative $Q_{\rm ox}$.

B. Damage Generation After Hot-Hole Stress (Off-State Stress)

To verify the efficacy of the new method, we also implement this method for the off-state stress condition at $V_D = 5$ V and

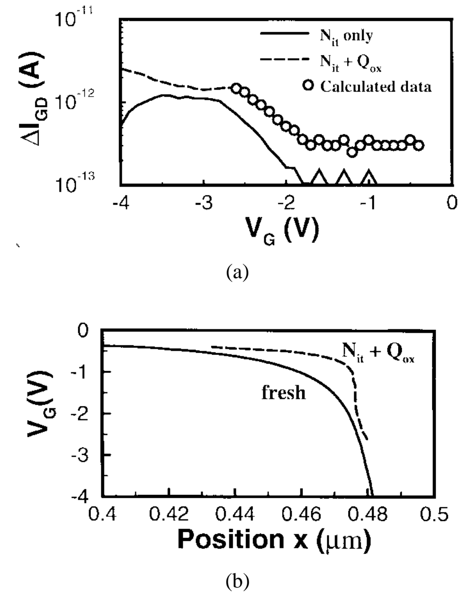

Fig. 5. (a) Fresh and stressed V_G versus x curves in which the difference for two curves results from the negative $Q_{\rm ox}(x)$ due to the hot electron stress. (b) Comparison between the experimental and calculated gate-diode currents.

$V_G = -4$ V for 5000 s. The $I_{\rm GD}$-V_G and $I_{\rm GIDL}$-V_D curves for fresh, after hot-hole injection, and detrapping are shown in Fig. 6 with forward drain-substrate bias of $V_D = -0.15$ V. Here, we use the detrapping step (@ $V_D = 3$ V, $V_G = 3$ V for 500 s) to detrap the positive $Q_{\rm ox}$. The peak value of $I_{\rm GD}$-V_G curve is shifted to more negative gate voltages after the hot-hole injection and is shifted to more positive gate voltages after the detrapping. This detrapping step will not cause any stress in fresh $I_{\rm GD}$-V_G and $I_{\rm GIDL}$-V_D curves by repeating the measurement. The extracted spatial distributions of $N_{it}(x)$ and $Q_{\rm ox}(x)$ are given in Fig. 7. The peak value of extracted positive charges is beyond 1×10^{12} cm^{-2} and larger than the peak value of extracted interface states. The verification of the calculated gated-diode current with experimental data is shown in Fig. 8. The calculated gated-diode current is matches well with the experimental results. The bottom figure also shows the calculated V_G-x relationship in which the difference of two curves at any position x is due to the existence of positive $Q_{\rm ox}(x)$.

C. Damage Generation at Maximum Substrate Current ($I_{B,\max}$)

The distribution of N_{it} under the maximum substrate current ($I_{B,\max}$) stress condition is well understood [5], but the comparison of peak position and quantities for N_{it} between the $I_{B,\max}$ and $I_{G,\max}$ are as yet unclear. To tell the difference, $I_{\rm GD}$-V_G and $I_{\rm GIDL}$-V_D curves for fresh and stressed conditions under $I_{B,\max}$ are measured in Fig. 9(a) with a forward drain-substrate bias of $V_D = -0.15$ V and, in Fig. 9(b), with gate bias of $V_G = -3$ V, respectively. From the $I_{\rm GIDL}$ current of Fig. 9(b) and the subthreshold current (which is not shown here), we know that the N_{it} generation is dominant, and the $Q_{\rm ox}$ generation is neglected at $I_{B,\max}$ stress since it can be observed from Fig. 9(b) that the $I_{\rm GIDL}$ currents for

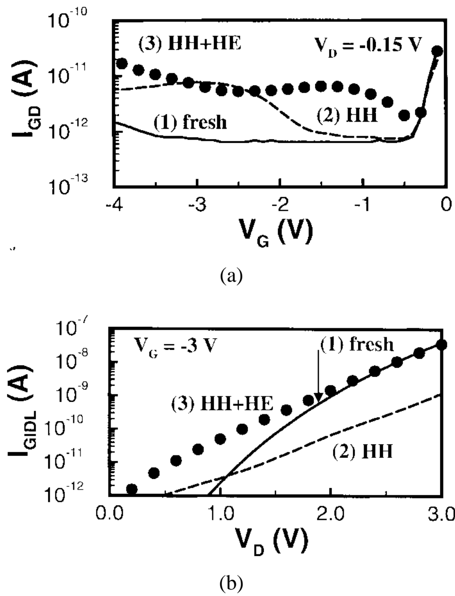

Fig. 6. (a) Measured $I_{\rm GD}$ characteristics of the test device after hot-hole stress at $V_D = 5$ V and $V_G = -4$ V. (b) Measured GIDL currents. Curves (1) fresh (solid line); (2) hot electron stress (dashed line), (3) after hot-hole detrapping (solid circles).

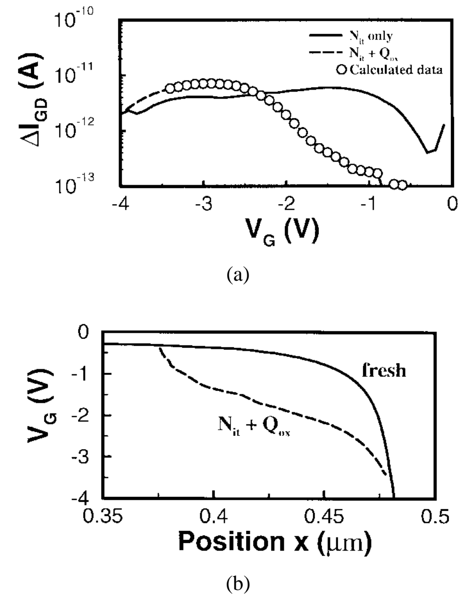

Fig. 8. (a) Fresh and stressed V_G versus x curves in which the difference for two curves results from the positive $Q_{\rm ox}(x)$ due to the hot-hole stress. (b) Comparison between the experimental and calculated gate-diode currents.

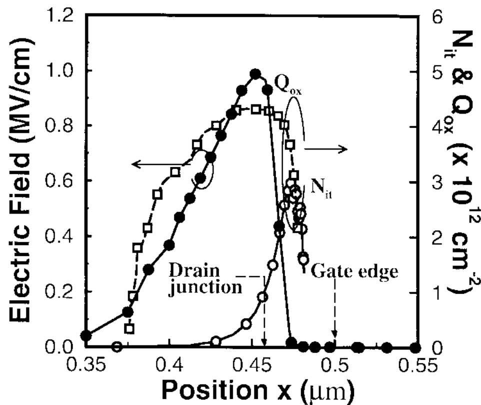

Fig. 7. Extracted spatial distributions of $N_{it}(x), Q_{\rm ox}(x)$ and simulated maximum lateral field for devices with hot-hole stress in Fig. 6.

fresh (curve 1) and stressed (curve 2) are the same at larger V_D bias. The extracted distribution of $N_{it}(x)$ and simulated lateral electric field at $I_{B,\max}$ stress are given in Fig. 10. The peak value of $N_{it}(x)$ is about 20 nm away from the peak of the electric field. We also found that values of N_{it} at $I_{B,\max}$ stress are larger than values of $I_{G,\max}$ stress due to a larger lateral field of $I_{B,\max}$ than values of $I_{G,\max}$. Furthermore, the lateral fields for $I_{B,\max}$ and $I_{G,\max}$ are all located in the gate-drain overlap region, but the position of $I_{G,\max}$ is far from the drain junction than those of $I_{B,\max}$, i.e., the lateral field of the $I_{G,\max}$ stress case is moving toward the gate edge. This result causes the peak N_{it} position of the $I_{B,\max}$ stress condition located in front of the $I_{G,\max}$ case.

Based on the above results, the advantages of the present method are as follows.

1) N_{it} and $Q_{\rm ox}$ can be simultaneously determined by using the neutralization (detrapping) technique and simple numerical calculation. It is very easy to implement based on simple dc measurement, and no complicate numerical iteration is needed to extract N_{it} and $Q_{\rm ox}$.
2) Lateral distributions of both N_{it} and $Q_{\rm ox}$ can be obtained under any stress conditions, such as $I_{G,\max}, I_{B,\max}$ and hot-hole stresses.
3) The gated-diode technique is much better than the charge pumping method in terms of the feasibility for probing oxide damages deeply into the gate-drain overlap region. In other words, the gated-diode technique can detect a wider range of damage distribution (see [7], Fig. 7).

V. Conclusion

In summary, we have successfully demonstrated a new method to separate the N_{it} from the $Q_{\rm ox}$ and to determine their spatial distributions for devices under various stress conditions such as $I_{G,\max}$, off-state stress, and maximum substrate current biases. Several salient features are the following.

1) We present *for the first time* a generalized method for device oxide damage characterization no matter whether there are hot-electron or hot-hole stress conditions.
2) The results have very important applications for studying flash EPROM reliabilities since $I_{G,\max}$ is the operating bias for hot carrier programming, and the generated $Q_{\rm ox}$ during the erase operation corresponds to the off-state stress bias that we used.
3) The gated-diode measurement technique is well suited for probing device oxide damage in the gate-drain overlap region with good accuracy.

Finally, the developed technique is very simple to implement in profiling the hot-electron-induced and hot-hole-induced damage for submicron or deep-submicron MOSFET's, and in particular, it is useful for flash EPROM, E^{2}PROM device reliability studies [10].

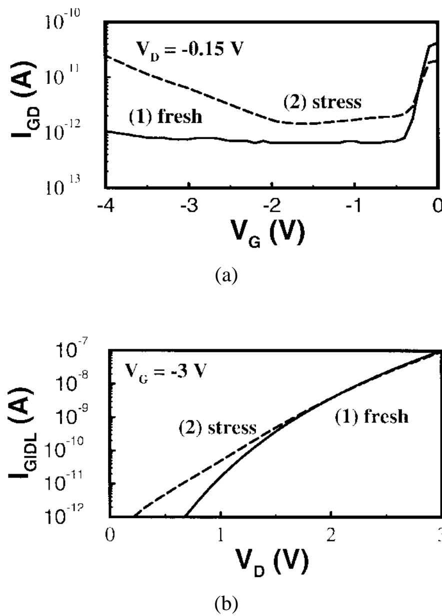

Fig. 9. (a) Measured $I_{\rm GD}$ characteristics of the test device after $I_{B,\max}$ stress at $V_D = 5$ V and $V_G = 2$ V. (b) Measured GIDL currents. Curves (1) fresh (solid line); (2) hot electron stress (dashed line).

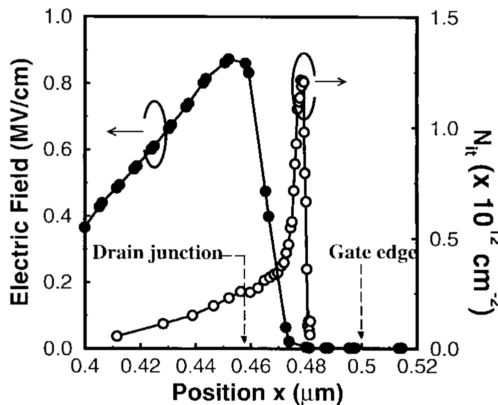

Fig. 10. Extracted spatial distributions of $N_{it}(x)$ and simulated maximum lateral field for devices with $I_{B,\max}$ stress in Fig. 9.

REFERENCES

[1] M. G. Ancona, N. S. Saks, and D. McCarthy, "Lateral distribution of hot-carrier-induced interface traps in MOSFET's," in *IEEE Trans. Electron Devices*, vol. 35, p. 2221, 1988.

[2] P. Speckbacher, A. Asenov, M. Bollu, F. Koch, and W. Weber, "Hot-carrier induced deep-level defects from gated-diode measurements in MOSFET's," *IEEE Electron Device Lett.*, vol. 11, p. 95, 1990.

[3] S. S. Chung, J.-J. Yang, C.-H. Tang, and P.-C. Chou, "Characterization of hot electron induced interface states in LATID MOS devices using an improved charge pumping method," in *Extended Abs. SSDM*, Chiba, Japan, 1993, pp. 841–843.

[4] W. Chen, A. Balasinski, and T. P. Ma, "Lateral profiling of oxide charge and interface traps near MOSFET junction," *IEEE Trans. Electron Devices*, vol. 40, no. 1, 1993.

[5] G. H. Lee, J. S. Su, and S. S. Chung, "A new profiling technique for characterizing hot carrier induced oxide damages in LDD n-MOSFET's," *Microelectron. Eng.*, vol. 28, p. 365, 1995.

[6] M. Tsuchiaki, H. Hara, T. Morimoto, and H. Iwai, "A new charge pumping method for determining the spatial distribution of hot-carrier-induced fixed charge in p-MOSFET's," *IEEE Trans. Electron Devices*, vol. 40, p. 1768, 1993.

[7] S. Okhonin, T. Hessler, and M. Dutoit, "Comparison of gate-induced drain leakage and charge pumping measurements for determining lateral interface trap profiles in electrically stressed MOSFET's," *IEEE Trans. Electron Devices*, vol. 43, p. 605, 1996.

[8] P. Speckbacher, A. Asenov, M. Bollu, F. Koch, and W. Weber, "The 'gated-diode' configuration in MOSFET's, a sensitive tool for characterizing hot-carrier degradation," *IEEE Trans. Electron Devices*, vol. 42, p. 1287, 1995.

[9] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.

[10] S. S. Chung, C. M. Yih, S. M. Cheng, and M. S. Liang, "A new oxide damage characterization technique for evaluating hot carrier reliability of flash memory cell after P/E cycles," in *Tech. Dig. Symp. VLSI Technol.*, June 10–12, Kyoto, Japan, 1997.

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