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Effects of Cobalt Silicidation on the Electrical Characteristics of Shallow p^+n Junctions Formed by BF_2^+ Implantation into Thin Polycrystalline Si Films

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ABSTRACT

Excellent shallow p^+n junctions have been formed by implanting BF_2^+ ions into thin polycrystalline Si films and subsequent annealing. The samples implanted at 50 keV to a dose 5×10^{15} cm^{-2} show a leakage of 1 nA/cm^2 and a junction depth of about 0.05 μm after a 800°C annealing. To reduce the series resistances of the junctions, silicidation with different cobalt thickness was used to drive the as-implanted dopants in the polysilicon films into the resultant junctions of the silicon substrates. For the low energy implantation at 50 keV at all dosages, silicidation can result in poor electrical characteristics due to the confinement of the dopants by the silicidation process. On the other hand, the electrical characteristics can be retained when a higher implantation energy of 100 keV with a dosage higher than 5×10^{15} cm^{-2} was used. In addition, the samples implanted at 125 keV show poor electrical characteristics for the nonsilicided junctions but good characteristics after the silicidation. It is attributed to the enhanced defect annihilation by the formed silicide. Furthermore, silicided implanted through poly-Si junctions with excellent characteristics can be fabricated after a low temperature (600°C) annealing if the samples are implanted at 100 keV with a dosage higher than 5×10^{15} cm^{-2}.

Introduction

In metal oxide semiconductor (MOS) ultralarge scale integrated (ULSI) circuits, the channel length has been scaled down to submicron dimensions that require a concomitant reduction in source/drain junction depth to minimize short channel effects.[1] Besides, metal silicides have been used to lower the contact resistances and sheet resistances of source/drain and gate electrodes as well as interconnections.[2-4] Cobalt silicide ($CoSi_2$) is one of the most promising materials for this purpose because of its low bulk resistivity (about 18 μΩ-cm) and good high temperature thermal stability.

Polycrystalline silicon has been widely investigated due to its excellent compatability with monolithic silicon technology. A thin layer of polycrystalline silicon has been used as base and emitter contacts in bipolar devices to provide self-aligned structures and high current gain.[5] It has been also used as source/drain contacts in MOS devices to facilitate contact metallization and junction formation.[6,7] There has been recent interest in metal oxide semiconductor field effect transistors (MOSFETs) with self-aligned polycrystalline silicon source and drain electrodes.[8,9] In these devices, polycrystalline silicon serves as a dopant diffusion source for source/drain junction formation.

Conventionally, shallow p^+n junctions were difficult to be realized in part because of the rapid anomalous diffusion of B in Si. The anomalous boron diffusion has been attributed to the supersaturation of Si interstitials provided by the thermal dissolution of small defect clusters produced by ion implantation. The role of extended defect evolution during the annealing on the anomalous boron diffusion has been also reported.[10-15] In addition, in the previous self-aligned silicide (salicide) schemes, when silicide is formed on source/drain regions, a portion of the heavily doped junction is consumed during the annealing, *i.e.*, silicidation. Consequently, the junction depths are lowered, and the variation in the amount of Si consumed by the silicide makes it increasingly more difficult to achieve the proper final junction depth.[16] To further reduce the junction depth, new techniques must be employed. There are several approaches to form the silicided shallow junctions. Previously, excellent silicided shallow junctions have been prepared by implanting dopants into metal or silicide layers and then driving the dopants into Si substrates, namely, the implant through metal and implant through silicide (ITM

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and ITS) schemes.[17-22] However, some inherent problems came out when these schemes were used, such as poor dopant drive-in efficiency, difficult process control, and so on.[17-23] By implanting dopants into thin polycrystalline Si (poly-Si) films, instead of silicides, we can form good junctions without causing the above problems.[23-25] Devices made using the scheme have been shown previously.[24,26]

In a previous paper,[26] excellent shallow p^+n junctions were formed by implanting BF_2^+ ions into poly-Si films on Si substrate and subsequent drive-in in an N_2 diffusion furnace, and the implant and annealing conditions were systematically examined to comprehend their effects on the resultant junctions. In the present work, cobalt silicides with different thicknesses were used on top of the poly-Si layers to reduce the resistances and also to drive the as-implanted dopants into the silicon substrates to fabricate shallow p^+n junctions. The effects on the junction characteristics when silicidation was applied to fabricate shallow p^+n junctions formed by the implantation through poly-Si (ITP) scheme were reported and discussed.

Experimental

(100) oriented, 1 to 3 Ω-cm, phosphorus-doped Si wafers were first chemically cleaned by using the standard RCA process. A thermal oxide layer of 5500 Å thick was thermally grown for patterning the active regions of diodes as well as for the utilization of selective etching. The diodes were square-shaped regions surrounded by the insulating oxide. The size of all diodes was 1000 × 1000 μm. Thin poly-Si layers of 1500 Å thickness were deposited on the patterned samples at 625°C by the low pressure chemical vapor deposition (LPCVD) system. Just before polysilicon deposition, the native oxide on the Si substrate was removed by dipping into dilute HF solution. Subsequently, the specimens were BF_2^+ implanted from 50 to 125 keV to various doses. The samples were then annealed in an N_2 diffusion furnace at 700 to 900°C for 30 min. Then the poly-Si layers were patterned. These specimens are named as the ITP ones. For the electrical measurements of the ITP samples, the process of aluminum evaporation was conducted to form the metal contacts. In addition, some of the BF_2^+-implanted samples which did not receive the activation annealing were directly covered with thin Co films of various thickness to form the silicided ITP junctions. The thicknesses of the Co films were 150, 300, and 450 Å, respectively. Then Mo capping layers of 400 Å thick were evaporated to prevent the Co layer from oxidation during the subsequent annealing.[27-29] The samples were then annealed at 500°C for 30 min in N_2 ambient to form cobalt disilicide ($CoSi_2$). Following this annealing, Mo and the unreacted Co were selectively etched in a 5:1:1 mixture of H_2O:H_2O_2:NH_4OH and a 6:1:1 mixture of H_2O:H_2O_2:HCl, respectively, at 70 to 85°C. After the selective etching process, an annealing at temperatures ranging from 700 to 900°C for 30 min was carried out to activate and drive the dopants into the silicon substrate. In addition, some samples were also annealed at 600°C for various times. The current-voltage (I-V) characteristics were obtained with an HP 4145B semiconductor parameter analyzer. The junction depths were measured by conducting the spreading resistance probe (SRP) method.

Results and Discussion

In this study, the transport of ions in matter (TRIM) simulation program was used to predict the distribution of the as-implanted dopants in poly-Si and silicon substrates. From the TRIM simulation results, the dopants were entirely confined in the poly-Si layer to a depth less than 1000 Å for the 50 keV implantation and no damage to the Si substrate was expected. For the 100 keV implantation, the implanted dopants were also entirely located inside the poly-Si layer (to a depth of 1500 Å) and with also no damage to the Si substrate. In both cases, the poly-Si film serves as a diffusion source for the p^+n junction formation during the subsequent annealing treatment. When the implantation energy was raised to 125 keV which will increase the dopant concentration in the underlying silicon substrate, the damage would cause poor junction characteristics. Consequently, high temperature annealing was needed and the defect-enhanced diffusion of dopants made shallow junctions impossible.[30-32] Hence, several factors will influence the properties of p^+n junctions fabricated using the ITP scheme. The implantation energy and dose, which will affect the dopant concentration and damage in the silicon substrate, are the key factors related to the junction characteristics.

The leakage current density, J_r, was measured at −5 V and at room temperature. At least ten diodes per sample were taken to evaluate the average J_r value. Figure 1 shows the J_r values as a function of annealing temperature for the samples implanted with BF_2^+ ions from 50 to 125 keV to a dose of 5×10^{15} cm^{-2}. Because the dopants were confined in the poly-Si layer and no severe damage was introduced for the implantation energy below 100 keV, the diffusion current therefore exceeded the generation-recombination component and dominated the reverse behavior. For the samples implanted with a dosage of 5×10^{15} cm^{-2}, a 700°C annealing resulted in an somewhat insufficient doping in the substrate for the 50 keV implanted samples and thus led to a J_r value at about 10 nA/cm^2 because of the increased reverse current, which was now dominated by the diffusion component. On the other hand, for the 100 keV implant, leakage currents as low as 2 nA/cm^2 could be achieved even for 700°C annealing. In addition, the implantation energy below 100 keV shows little impact when the annealing temperatures are higher than 700°C. Hence, an annealing at 800°C resulted in excellent electrical characteristics as long as implantation energies were below 100 keV. However, high energy implantation at 125 keV shows poor characteristics at all annealing temperatures because the Si substrates are serverely damaged. Thus, leaving a dopant profile tail into the Si substrate, used in the ITS scheme, is probably not a good strategy for the ITP method.

Poly-Si which serves as the implantation buffer layer as well as the doping source here can greatly enhance the drive-in efficiency, relative to using silicide as the doping source.[25] Namely, the implanted dopants in the poly-Si layers can be easily driven into the underlayered silicon substrate during the annealing. The knock-on of the metal atoms in the ITM scheme also disappears when using the ITP scheme. In terms of the ITP scheme, however, the dopant drive-in efficiency still plays a very important role in determining whether a good junction can be formed or not. Appropriate implant energies, such as 75 and 100 keV here, can lead to the deeper as-implant dopant profile and thus more considerable dopant drive-in. Hence, lower annealing temperatures are enough to drive sufficient dopants into the Si substrates. In addition, annealing temperatures above 800°C resulted in low leakage diodes even for the samples implanted at 50 keV. Furthermore, increasing the

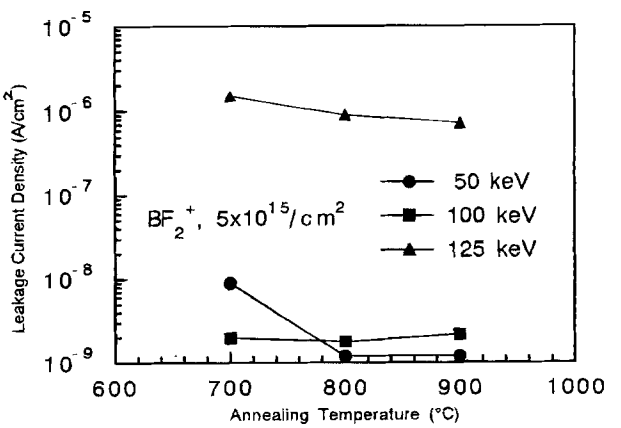

Fig. 1. Dependences of leakage current density on annealing temperature for the nonsilicided samples implanted at various energies to a dose of 5×10^{15} cm^{-2}. The annealing time is 30 min.

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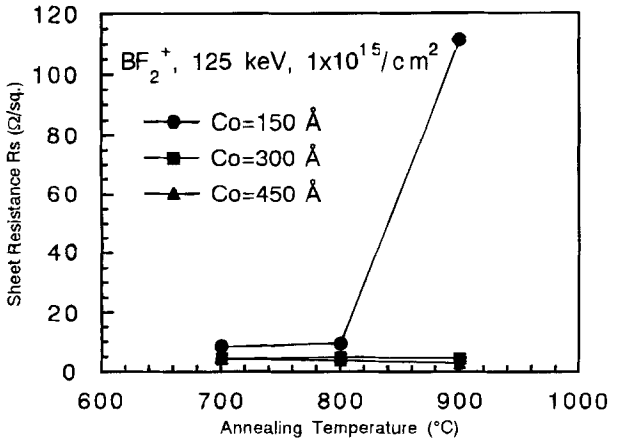

Fig. 2. Dependences of sheet resistance on annealing temperature for the Co films on poly-Si layers BF_2^+ implanted at 125 keV to a dose of 5×10^{15} cm^{-2}. The annealing time is 30 min.

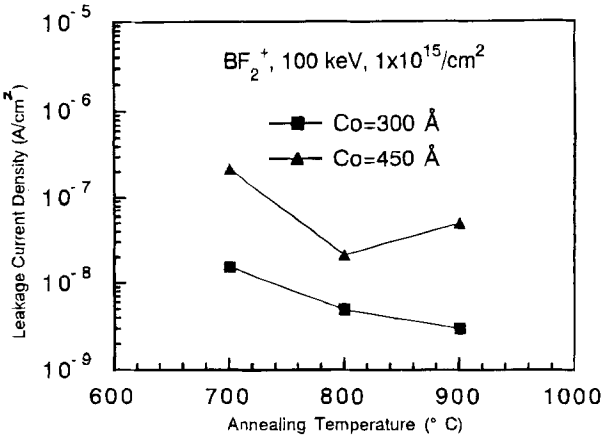

Fig. 4. Dependences of leakage current density on annealing temperatures with various Co thickness for the samples implanted at 100 keV to a dose of 1×10^{15} cm^{-2}. The annealing time is 30 min.

dosage can be able to enhance the drive in efficiency and improve the electrical characteristics for the specimens implanted at low energies and annealed at low temperatures. Even for the 50 keV implant, J_r value at about 3 nA/cm^{-2} was achieved by a 700°C/30 min annealing when the implant dose was raised to 1×10^{16} cm^{-2}. From the results mentioned above, the processing window for the ITP technique is wide.

Cobalt silicides are often used as the contacts to reduce the resistance and increase the device speed. As the cobalt films are deposited on the BF_2^+-implanted poly-Si specimens, the silicidation process can drive the as-implanted dopants in the poly-Si layer into the silicon substrate to form the silicided ITP junctions. At first, the thermal stability of the cobalt silicide films on the top of the poly-Si layers was investigated. Figure 2 shows the sheet resistance (R_s) value as a function of annealing temperature for the Co/implanted poly-Si bilayer structures with the cobalt thickness as a parameter. The thicknesses of the formed silicide were about 520, 1050, and 1570 Å for the Co films with 150, 300, and 450 Å in thickness. The thicknesses of the consumed silicon were about 540, 1090, and 1630 Å, respectively. The poly-Si layers were BF_2^+-implanted at 125 keV to a dose of 1×15 cm^{-2}. For the cobalt film with 150 Å in thickness, the resistance increases tremendously after an annealing at 900°C, indicating that the formed cobalt silicide films become island structures at such a temperature. However, the sheet resistances for the thicker films remained stable even after an annealing at 900°C. The dosage of the implanted dopants in the poly-Si layers also exhibit impact on the sheet resistances of the bilayer structures. Figure 3 shows the dependence of the sheet resistances on the annealing temperatures for different implantation dosage. Even for the cobalt films as thin as 150 Å, the R_s values display little increase for dosages higher than 5×10^{15} cm^{-2}. It can be attributed to the stabilization effect of the fluorine atoms in the silicide films, as observed previously in $CoSi_2$,[33-35] PtSi,[36,37] and Pd_2Si [38] thin films on silicon substrates. Moreover, the amorphization of the poly-Si layer by the medium and high dose implantation results in a smoother cobalt silicide/poly-Si interface, thus facilitating better thermal stability.[39]

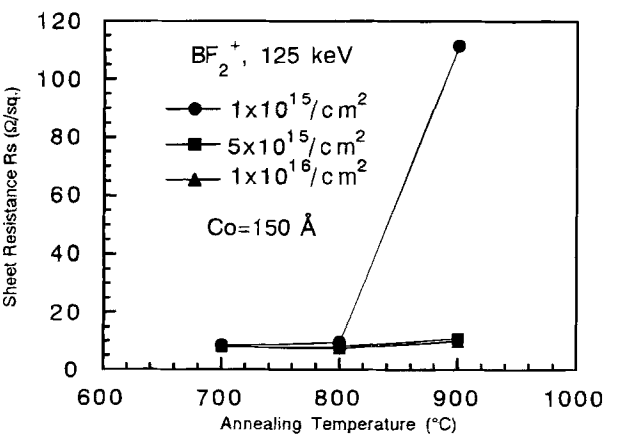

Fig. 3. Dependences of sheet resistance on annealing temperature for the 150 Å thick Co films on poly-Si layers BF_2^+ implanted at 125 keV with various dosages. The annealing time is 30 min.

Second, the effects of the silicidation process for the 300 and 450 Å thick Co on the electrical characteristics of the ITP samples are discussed. For the poly-Si samples implanted at 50 keV with various dosages, the resultant silicided ITP diodes are very leaky at all the annealing temperatures, which are very different from the nonsilicided specimens. For the nonsilicided samples, high enough activation temperatures result in good characteristics. According to the TRIM simulation results, the dopants were entirely confined in the poly-Si layer to a depth less than 1000 Å for the implantation energy 50 keV. Since the 300 Å thick cobalt films will consume a 1000 Å silicon layer, it means that the dopants cannot be driven effectively during the silicidation for such a low energy implantation. Hence, for the samples implanted at 50 keV, a preannealing cycle for driving the dopants into the silicon substrate before the cobalt deposition was needed to attain the low leakage characteristics.

As for the high implantation energy at 100 keV with the dosage of 5×10^{15} cm^{-2}, all the silicided samples exhibited the comparable J_r values with the nonsilicided ones. The junction depth measured from the poly-Si/Si substrate interface for the 100 keV/5×10^{15} cm^{-2} implanted specimens after a 700°C silicidation process of 0.07 μm, which was suited for ULSIs utility. Similar results are also found for the dose of 1×10^{16} cm^{-2}. However, the low-dose implantation of 5×10^{15} cm^{-2} gave very different results, as shown in Fig. 4. The leakage of the samples with the 300 Å thick Co films was low when an annealing temperature above 800°C was applied. From this figure, it was found that the samples with the 450 Å thick Co possess much higher leakage than others in this low dose case due to more dopant confinement for the thicker formed silicides, as in the case of 50 keV implantation. The increase in the leakages when the silicidation temperature was raised from 800 to 900°C may be due to the increased rough interface coming from the native oxide on the original poly-Si/Si interface and the grain growth of the silicide films. This impact was seen to be lessened when doses higher than 5×10^{15} cm^{-2} were used, and the resultant diodes exhibited low leakage characteristics even if 450 Å thick Co films were used.

Increasing the implantation energy to 125 keV, the curves of J_r values *vs.* annealing temperatures for the implanta-

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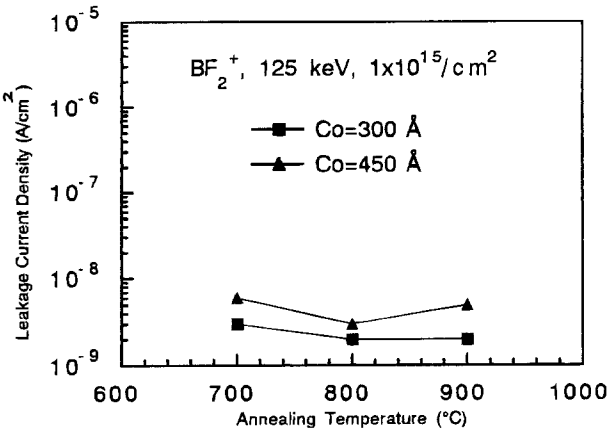

Fig. 5. Dependences of leakage current density on annealing temperatures with various Co thickness for the samples implanted at 125 keV. The dosage of 1×10^{15} cm^{-2}. The annealing time is 30 min.

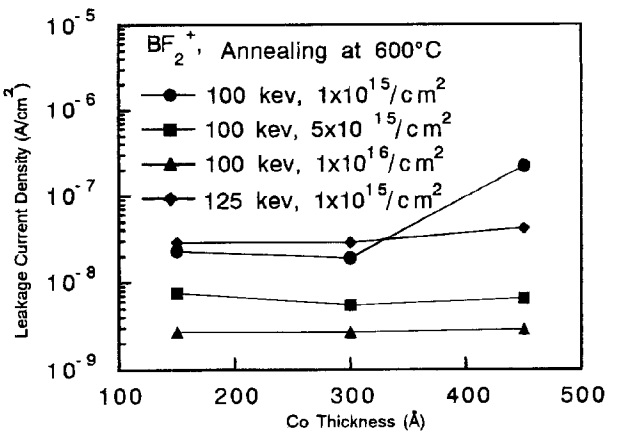

Fig. 7. Dependences of leakage current density on Co thickness for the samples activated at 600°C for 1 h.

tion dosage of 1×10^{15} cm^{-2} with the cobalt film thickness as a parameter are shown in Fig. 5. All diodes showed leakages less than 10 nA/cm^2. For this low dose implant, even a 700°C/30 min annealing resulted in J_r values less than 8 nA/cm^2 for different Co thicknesses. The situation was quite different for the nonsilicided ITP specimens, which showed poor characteristics at all annealing temperatures because the silicon substrates were severely damaged, especially for the medium and high dose cases. The resultant low leakage characteristics for the silicided ITP junctions were attributed to the effects of the silicidation process, such as defect annihilation and substrate impurity redistribution enhancement due to point defect injections during the silicidation process. The leakage current for the samples silicided with 450 Å Co films were slightly larger than the others due to the interface roughness of the silicide/Si substrate and more dopant confinement for the thicker formed silicides, although the point defect injection level was higher for the thicker silicide. It was found that the samples silicided with 300 Å thick Co films exhibited lower J_r values than other thickness at all doses because of the compromise between the defect annihilation level and the dopant confinement of the silicides. The dependences of leakage current densities on annealing temperature when 300 Å thick Co was used is shown in Fig. 6. It was found that when the silicidation process was used, the 125 keV implanted samples showed J_r values less than 10 nA/cm^2 when a 700°C/30 min annealing was used, even in the high dose implantation case. The J_r values were higher for the high dose implantation samples because the damage was more severe in this case. Increasing the annealing temperature resulted in a further improvement in the leakage current densities to about 2 to 3 nA/cm^2. The junction depths measured from the poly-Si/Si substrate interface for the 125 keV/1 $\times$ 10^{15} cm^{-2} implanted specimens after a silicidation process at 700 and 800°C were 0.1 and 0.14 μm, respectively.

Low temperature feasibility of the diodes fabricated by the ITP method was also investigated. For the nonsilicided samples, a 600°C/7 h annealing was conducted to fabricate the junctions. The silicided ITP samples received a 600°C/6 h preannealing before the deposition of the cobalt films and the subsequent silicidation was performed at 600°C for 1 h. The result is shown in Fig. 7. For the nonsilicided samples, a 600°C/7 h annealing resulted in poor diode characteristics at all implantation conditions. For the silicided samples implanted at 100 keV with the medium and high dosages, the leakage current densities were about 8 to 6 and 3 nA/cm^2 for different Co thicknesses. The 100 keV/1 $\times$ 10^{15} cm^{-2} implanted samples failed to have low leakage characteristics due to insufficient doping in the substrate, especially when silicided with 450 Å thick Co films. In addition, although the formed silicide-enhanced defect annihilation, 125 keV/1 $\times$ 10^{15} cm^{-2} implanted samples still had J_r values above 30 nA/cm^2. Thus silicided ITP junctions with excellent characteristics can be fabricated by a low temperature annealing when the samples implanted at 100 keV with a dosage higher than 5×10^{15} cm^{-2} was used.

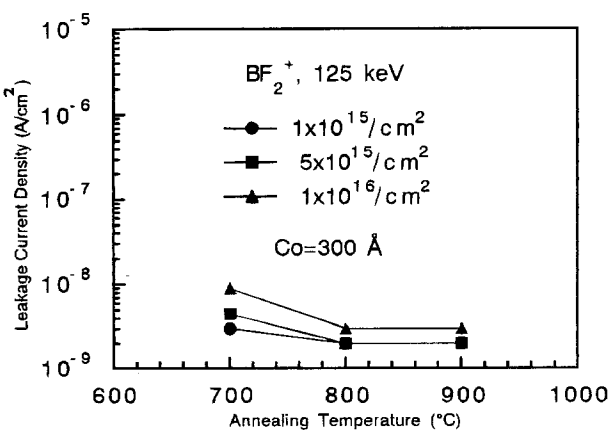

Fig. 6. Dependences of leakage current density on annealing temperatures for the 300 Å thick Co films on poly-Si layers BF_2^+ implanted at 125 keV to various dosages. The annealing time is 30 min.

Conclusion

By properly implanting BF_2^+ ions into thin poly-Si films (1500 Å) and subsequent annealing, shallow junctions with a leakage of 1 nA/cm^2 and a junction depth of about 0.05 μm have been successfully achieved. To reduce the series resistances of the junctions, silicidation with different cobalt thicknesses was used to drive the as-implanted dopants in the polysilicon films into the resultant junctions of the silicon substrates. For the low energy implantation at 50 keV at all dosages, silicidation can result in poor electrical characteristics because the formed silicides cannot effectively push down the dopants into the substrates. On the other hand, the electrical characteristics can be retained when a higher implantation energy of 100 keV with a dosage higher than 5×10^{15} cm^{-2} was used. In addition, the samples implanted at 125 keV show poor electrical characteristics for the nonsilicided junctions but good characteristics after the silicidation are attributed to the enhanced defect annihilation by the formed silicide. Furthermore, silicided ITP junctions with excellent characteristics can be fabricated after a low temperature (600°C) annealing if the samples are implanted at 100 keV with a dosage higher than 5×10^{15} cm^{-2}.

Acknowledgements

The research was supported in part by the Republic of China National Science Council under the Contract No. NSC 83-0404-E009-050. The technique supports from the

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National Nano Device Laborabory, National Science Council of the Republic of China, are also acknowledged.

Manuscript submitted June 1, 1994; revised manuscript received Oct. 27, 1994.

National Chiao Tung University assisted in meeting the publication costs of this article.

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