A Novel Ion-Bombarded and Plasma-Passivated Charge Storage Layer for SONOS-Type Nonvolatile Memory

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***Abstract*—A novel technique combination of ion bombardment (IB) and NH_3 plasma treatment (PT) has been presented to yield a highly effective charge storage layer for Si/SiO2/Si3N4/SiO2/Si (SONOS)-type nonvolatile memory applications. The IB technique creates additional trap sites within the charge storage layer strikingly to enhance the charge trapping/detrapping efficiency of the storage layer, and the NH_3 PT passivates shallow trap sites significantly to improve reliability characteristics. The distribution of trap sites corresponding with various energy levels is clearly described by discharge-based multipulse analysis. As compared with the control sample (without IB and NH_3 PT), the ion-bombarded and NH_3-plasma-passivated memory device has faster program/erase speeds and larger memory window. In addition, the competent reliability properties of the ion-bombarded and NH_3-plasma-passivated memory, such as good endurance, long data retention, and acceptable disturbance, were also demonstrated in this letter.**

***Index Terms*—Discharge-based multipulse (DMP), Flash memory, ion bombardment (IB), metal/Al2O3/Si3N4/SiO2/Si (MANOS), NH_3 plasma treatment (PT).**

I. Introduction

RECENTLY, a large-capacity and highly reliable nonvolatile memory (NVM) has been one of the most serious issues in the consumer electronics market. In order to pursue the goal, scaling down is an essential means and a main approach for pushing next-generation NVM development [1]. However, the recent NVMs have been still dominated by the floating-gate (FG) structure [2], [3]. As continually shrunk, the FG memory will face a critical challenge of data retention for high-density array. Thus, the SONOS-type memory devices have attracted much more interest recently due to simple process, low-voltage operation, and good shrinking capability [4]–[6]; even so, they still have a serious issue in insufficient storage charges as shrunk below 2x nm [7]. It is because the number of trap sites within the storage layer decreases with decreasing the physical thickness of the charge storage layer. It will easily cause the faults in differentiating memory states, particularly in serious charge losses or sensitive disturbance situations.

To increase the number of trap sites within the storage layer under no change in the physical thickness of the charge storage layer, the authors present a novel technique combination of ion bombardment (IB) and NH_3 plasma treatment (PT) to achieve it. However, this ion-bombarded and NH_3-plasma-passivated charge storage layer has high charge trapping/detrapping efficiency and competent reliability for SONOS-type NVMs. The $TaN/Al_2O_3/Si_3N_4/SiO_2/Si$ (MANOS) structure was employed in this experiment since it has fast program/erase (P/E) speeds and highly reliable properties as compared with the traditional SONOS memory [8]–[10]. It is attributed to the combination of the high-k blocking layer (Al_2O_3) and the metal gate (TaN) [11]. The electrical characteristics, including P/E speeds, device endurance, data retention under the different temperatures (room temperature (RT) and 125 °C), and disturbance properties, were demonstrated in this letter.

II. Experiments

The samples were prepared on $\langle 100 \rangle$ p-type silicon wafers. After the local oxidation of silicon formation, a 3-nm-thick tunneling SiO_2 film was thermally grown by a vertical furnace in an N_2O ambient, followed by a bottom Si_3N_4 film that was deposited at 780 °C in a low-pressure chemical vapor deposition (LPCVD). Subsequently, an argon IB process was performed on the surface of the bottom Si_3N_4 at 375 °C for 5 s by high-density plasma chemical vapor deposition (HDPCVD). The RF and dc powers of the IB were 200 and 5 W, respectively. The thickness of the ion-bombarded Si_3N_4 sample was 3 nm. Afterward, the NH_3 PT was used on the ion-bombarded Si_3N_4 sample at 375 °C for 60 s by HDPCVD. The RF power of the NH_3 PT was 900 W. A 4-nm-thick top Si_3N_4 was deposited at 780 °C by LPCVD, and then, a 12-nm-thick Al_2O_3 was deposited as a blocking layer by metal organic chemical vapor deposition. A TaN film was then deposited as a control gate. Finally, the standard MOSFET processes were performed to complete a MANOS memory device. In addition, the MANOS with IB (without NH_3 PT) and the control sample (without IB

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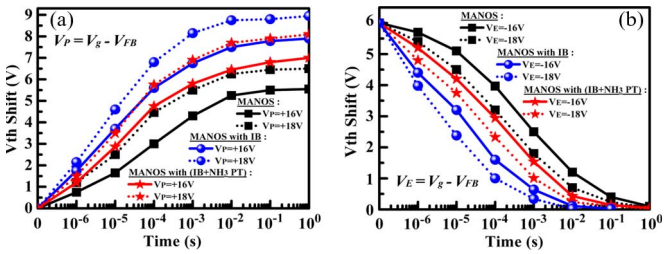

Fig. 1. (a) Program and (b) erase speeds of the MANOS memory devices. For the erase measurement, all the devices were initially tested at the program state ($V_{\rm th}$ shift $= 6$ V).

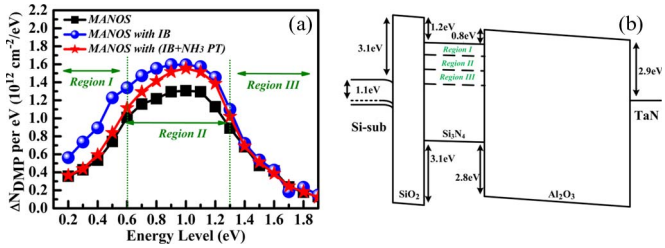

Fig. 2. (a) Energy-level distribution of trap sites within the Si_3N_4 trapping layer. (b) Energy diagram of the MANOS structure.

and NH_3 PT) were also prepared. The channel width and length of the devices were 10 and 0.35 μm, respectively.

III. Results and Discussion

The P/E transients of the MANOS memory devices are shown in Fig. 1(a) and (b), respectively. The Fowler–Nordheim tunneling was used for programming and erasing. The conditions of programming were 16 and 18 V, respectively. In Fig. 1(a), the threshold-voltage ($V_{\rm th}$) shift increases with increasing the applied voltage. It is because a large number of electrons are induced to inject into the storage layer [4]. In addition, it is obvious that, with either the MANOS with (IB + NH_3 PT) or the MANOS with IB, they exhibit faster program speeds and larger memory windows than the control sample. For the erase measurement, the erasing conditions were -16 and -18 V, respectively. Likewise, both the erase speeds of the MANOS with (IB + NH_3 PT) and the MANOS with IB are faster than that of the control sample. The results indicate that the ion-bombarded charge storage layer has better charge trapping/detrapping efficiency than the normal charge storage layer without IB. However, the improvement is attributed to the increasing of the number of trap sites within the storage layer, and those additional trap sites are created by the IB process. On the other hand, as compared with the MANOS with IB, the MANOS with (IB + NH_3 PT) has low charge trapping/detrapping capacity due to the NH_3 plasma passivating shallow trap sites within the storage layer. In spite of that, for reliability, the passivation of shallow trap sites is a significant contribution.

The distribution of trap sites corresponding with various energy levels is further analyzed by the discharge-based multipulse (DMP) technique [12], as shown in Fig. 2(a). Fig. 2(b) displays the related energy diagram of the MANOS structure. Regions I, II, and III in Fig. 2(a) and (b) are mutually corresponding. In the two figures, the energy levels of trap sites in the Si_3N_4 trapping layer are divided into three regions, i.e., the shallow (Region I), middle (Region II), and deep (Region III) energy levels. It is shown in Fig. 2(a) that the MANOS with IB has much more trap sites than the control sample. The IB process increases ca. 53% and 27% the number of trap sites in the shallow and the middle energy levels, respectively. Also, it can be found that most of the shallow trap sites and parts of the middle trap sites of the ion-bombarded charge storage layer are passivated after NH_3 PT. This implies that the NH_3 plasma passivation is sensitive to shallow trap sites and insensitive to deep trap sites. The result explains why the MANOS with (IB + NH_3 PT) has low charge trapping/detrapping efficiency as compared with the MANOS with IB. However, the decrease in shallow trap sites is a significant benefit for reliability. Aside from that, Naich et al. reported that the charge centroid is in the upper part of Si_3N_4 for the $SiO_2/Si_3N_4/SiO_2$ dielectric stack [13]. As compared with intrinsic trap sites of the control Si_3N_4 sample, hence, IB-induced trap sites are definitely closer to the channel. This explains that the centroid of the ion-bombarded Si_3N_4 sample is closer to channel than that of the control Si_3N_4 sample. It implies that charge trapped in the ion-bombarded Si_3N_4 sample has a larger influence on $V_{\rm th}$ than that trapped in the control Si_3N_4 sample. As can be easily seen, the higher charge trapping/detrapping efficiency for the ion-bombarded charge storage layer is attributed to the contribution of additional trap sites and charge centroid variation.

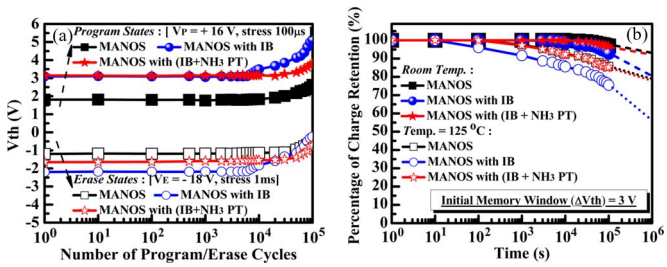

Fig. 3. (a) Endurance properties of the MANOS memory devices. The programming and erasing stresses were $V_P = +16$ V at 100 μs and $V_E = -18$ V @ 1 ms, respectively. (b) Date retention characteristics of the MANOS memory devices.

Fig. 3(a) shows the endurance characteristics. In Fig. 3(a), all the devices exhibit good endurance properties with invisible memory window narrowing, but there occurs a $V_{\rm th}$ upward shift after frequent P/E cycles. It is because that it is easy for charges to be stored in deep trap sites during high P/E cycles and it is difficult for them to be removed under erasing [4]. Aside from that, the MANOS with IB has a larger $V_{\rm th}$ upward shift than the others. This is due to the fact that, through the assistance of shallow trap sites, it is easy for charges to be injected into the top dielectric layer and it is also hard for them to be removed. The data retention characteristics at RT and 125 °C are also demonstrated in Fig. 3(b). It is shown that both the MANOS with (IB + NH_3 PT) and the control sample show better retention properties than the MANOS with IB, and they have the approximate retention characteristics. The MANOS with IB has 17% and 25% charge losses for 10^6 s at RT and 125 °C, respectively. Nevertheless, the MANOS with

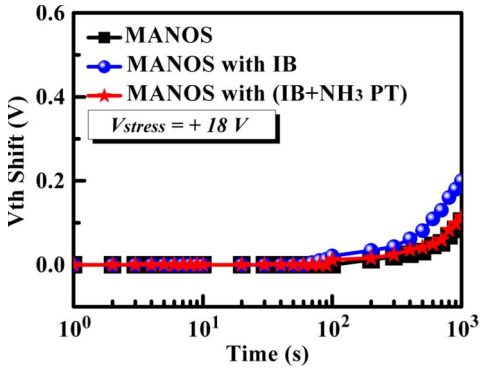

Fig. 4. Disturbance characteristics of the MANOS memory devices. All the devices were measured at the initial state by applying a gate stress up to 10^3 s.

(IB + NH_3 PT) shows 5% and 14% charge losses for 10^6 s at RT and 125 °C, respectively. This significant improvement is attributed to the NH_3 plasma passivating most of the shallow trap sites created by the IB process.

Because of the array arrangement in the practical NAND-type memory design, the continuous stressing on a device may influence the states of surrounding devices. Therefore, the disturbance phenomena of the MANOS memory devices were demonstrated to ensure the devices' reliability [14]. Fig. 4 shows the disturbance characteristics at $V_{\rm stress} = 18$ V. In the figure, a 0.22-V $V_{\rm th}$ shift is obtained at $V_{\rm stress} = 18$ V after 10^3 s for the MANOS with IB, whereas only a 0.11-V $V_{\rm th}$ shift is observed under the same stress condition for both the MANOS with (IB + NH_3 PT) and the control sample. This illustrates that the NH_3 PT significantly improves the disturbance phenomenon caused by the IB process. This is because most of the shallow trap sites created by the IB are eliminated through the NH_3 PT, and these shallow trap sites are sensitive to external voltage.

IV. Conclusion

In this letter, the IB process strikingly increases the number of trap sites within the storage layer to induce high charge trapping/detrapping efficiency. However, parts of the additional trap sites created by the IB are in relatively shallow energy levels as compared with natural trap sites. It is easy for charges stored in shallow trap sites to escape from the storage layer and to cause reliability degradation. In spite of that, through the NH_3 PT, this reliability degradation caused by the IB has been significantly improved. The NH_3 PT is sensitive to shallow trap sites and insensitive to deep trap sites. Through the combination of the IB process and the NH_3 PT, therefore, the charge storage layer efficiency can be significantly enhanced under no damage to reliability properties for MANOS NVM.

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