Suppressing Device Variability by Cryogenic Implant for 28-nm Low-Power SoC Applications

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***Abstract*—In this letter, we have demonstrated that cryogenic implant in the source and drain formation offers advantages for reducing the threshold voltage mismatch in pMOSFET. A discrete dopant profiling method is used to verify the presence of boron out-diffusion from the drain, which further induces the random dopant fluctuation. Results show that this boron out-diffusion can be greatly reduced in this new process. Two major factors in improving the device variability by cryogenic implant are discussed, i.e., the polysilicon grain size control and the embedded-SiGe dislocation defect reduction during source and drain formation.**

***Index Terms*—Cryogenic implant, ion implantation, logic device, novel process technology, random dopant fluctuation.**

I. Introduction

JUNCTION depth scaling and the suppression of threshold voltage ($V_{\rm th}$) variation are two critical issues for further scaling of CMOS devices. Various sources of statistical variability have been reported [1]–[5]; in particular, the implant-induced defect engineering becomes critical to control the final doping profile distribution in the source/drain (S/D), e.g., dopant activation and transient enhanced diffusion (TED), and the $V_{\rm th}$ variability. Recently, studies [1]–[5] have reported the mechanisms of nMOSFET variability. However, few studies have been paid on pMOSFET, particularly the point defect generation during S/D formation. In this letter, the use of cryoimplant in suppressing the variability of 28-nm pMOSFET using diamond-shape embedded SiGe (eSiGe) with high germanium concentration will be demonstrated. The improved variability was achieved by the poly-Si grain size modulation and the effective control of boron TED by reducing the eSiGe dislocation defect. We will demonstrate the $V_{\rm th}$ mismatch improvement of pMOSFET based on the results of discrete dopant profiling (DDP) [6] and transmission electron microscopy (TEM) measurements.

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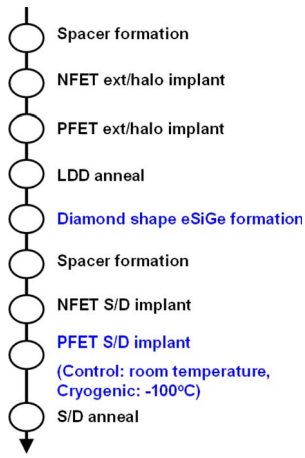

Fig. 1. Twenty-eight-nanometer CMOS process flow with advanced strain formation and annealing process. The diamond-shape eSiGe process is implemented before the second spacer formation. Cryoimplant ($-100\,^{\circ}$C) is applied for pMOSFET S/D formation along with RT control. The complete details can be found in [7].

II. Cryogenic Implantation of pMOSFET and Experimental Results

A 28-nm CMOS process flow is shown in Fig. 1 [7], [8]. The source and drain junctions of pMOSFET are formed by the ion implantation of boron into diamond-shape eSiGe with high germanium concentration. Also, cryoimplant (at a very low temperature of $-100\,^{\circ}$C) has been used in the S/D formation, and the control one made at room temperature (RT) implant was used as references. To check the cryoimplant effects on the device variability, the correlation between saturated $V_{\rm th}$ and linear $V_{\rm th}$ is shown in Fig. 2. The inverse relationship between the threshold voltage and the square root of device area, i.e., the Pelgrom plot [9], was derived based on the linear $V_{\rm th}$. This plot is not valid in the saturation region, and therefore, the plot in Fig. 2 can better be used to explain the superiority of the new cryoimplant process and the comparison with that of the RT implant.

All of the threshold voltages were taken from seven different dimensions (from a to g); each dimension has 63 dies. The median of each dimension was taken from 63 data sets. The linear threshold voltages $V_{\rm th,lin}$ were measured by the $g_{m,\max}$ method at a drain bias of -0.1 V, and the saturated threshold voltages $V_{\rm th,sat}$ were measured from the tangent of the $\sqrt{I_D}$-*versus*-$V_{\rm GS}$ curves at a drain bias of -1 V. From the comparison in Fig. 2, among all the samples, the comparison for same-dimension samples, control (triangular) and cryoimplant (diamond), shows a consistent trend in that the saturated $\sigma V_{\rm th}$

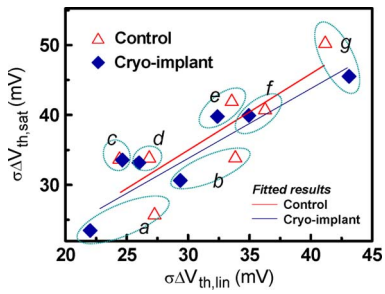

Fig. 2. Comparison between saturated $\sigma V_{\rm th}$ and linear $\sigma V_{\rm th}$ of pMOSFETs with various dimensions. Devices with the same dimension are circled together. The (diamonds) cryoimplant devices show a smaller saturated $V_{\rm th}$ variation than the (triangles) control ones, which show a consistency with the fitting curves.

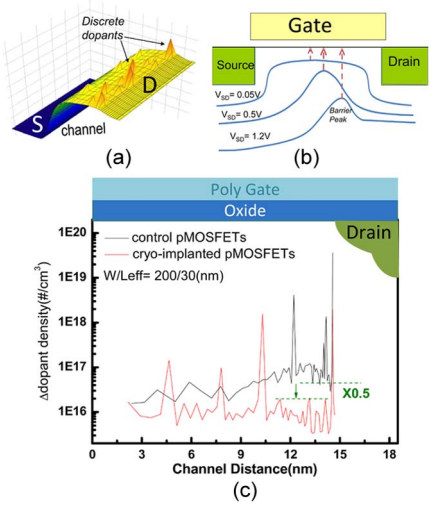

Fig. 3. Methodology of DDP along the channel direction for random dopant analysis. (a) Discrete dopant in the channel is the source of threshold voltage variations. (b) By varying the source-to-drain bias, the channel barrier peak is shifted from the channel middle to the drain side, from which we can calculate the position of the discrete dopant. (c) Channel DDP results for two control and cryoimplanted pMOSFET devices.

values of the cryoimplant process are smaller than those of the control samples. In other words, the cryoimplant process exhibits smaller values of the saturated $\sigma V_{\rm th}$ with respect to the linear ones, which is believed to be from the dopant effects near the drain junction region, as will be explained later. In other words, the cryoimplant process shows efficient reduction of the $V_{\rm th}$ variation in comparison to the control ones.

In lieu of an experimental approach that was developed in [6], the dopant distribution along the channel can be obtained. The discrete dopant can be treated as a delta function located in the channel randomly which results in the $V_{\rm th}$ variation, but only those discrete dopants at the peak position of the channel barrier will affect the carrier transport [Fig. 3(a)]. As shown in Fig. 3(b), by increasing the source-to-drain bias $V_{\rm SD}$, the channel barrier peak will be moved from the middle of the channel to the drain side, from which we can calculate the dopant density as a function of the channel position from the measured threshold voltages.

The changing of the peak position is the location of the dopant such that the dopant density can be determined along the channel direction [Fig. 3(c)]. Results show that the cryoimplant devices demonstrate excellent suppression of the discrete

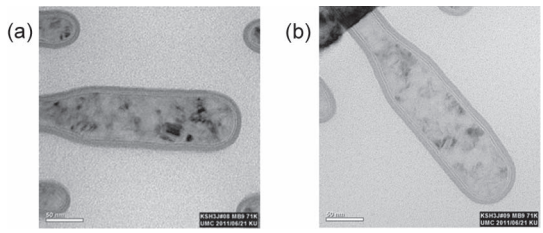

Fig. 4. Polysilicon grain after S/D anneal analyses via PVTEM with pMOSFET S/D implants at (a) RT or (b) cryogenic temperature. Cryoimplant results in smaller grain size.

dopant fluctuation, as compared to the control, in two folds. The first one is the fact that the cryoimplant process exhibits a smaller variation of the delta dopant density in the middle of the channel, e.g., from 2 to 10 nm (along the channel). As we further examine the distribution of the control (the black curve) from 10 to 15 nm, the delta dopant density not only increases toward the drain but also exhibits huge peaks. This is believed to come from the boron impurities out-diffused into the channel. These out-diffused impurities induce the fluctuation of the channel dopant concentration. The magnitude of the delta dopant density is an indication of the out-diffused ions of the boron impurities. In comparison, the cryoimplant process shows 50% less delta dopant fluctuations, and particularly, the three peaks induced by boron out-diffusion were suppressed. This is consistent with Fig. 2, in which a smaller value of saturated $\sigma V_{\rm th}$ was observed for cryoimplant devices in comparison to the control ones. Thus, we believe that the cryoimplant process is efficient in providing a better control of the dopant fluctuation as well as the suppression of boron-induced fluctuations.

III. Discussions

To explain the device variability improvement, it is important to understand the role of S/D implant in eSiGe and polysilicon. The S/D implant is used to increase dopant activation in eSiGe as well as in polysilicon. For polysilicon, it has been shown that the benefits of an amorphous structure [10] from an as-deposited polysilicon film are vanished during the reoxidation step after polysilicon patterning. The implant-induced amorphization becomes critical to suppress the random channeling and reduce the electrical fluctuation. Enhanced diffusion along the grain boundaries can degrade the doping uniformity within the poly-Si gate and results in a localized dopant penetration from the higher doping gate regions down to the channel [11]. Fig. 4 shows the polysilicon grain planar-view TEM (PVTEM) views of the RT implant and cryoimplant after the S/D anneal. Smaller grain sizes were observed for the device with cryoimplant. The modification of the polysilicon grain size can help reduce dopant random movement in polysilicon and minimize device threshold voltage variability [12]. However, from Fig. 3(c), the delta dopant density of the cryoimplanted sample shows result slightly better than or comparable to that of the control sample in the channel middle region. It indicates that the grain size change by the cryoimplant process does not show much influence to the device mismatch improvement.

For strained channel pMOSFET, higher channel stress levels and lower S/D resistance can be achieved with high Ge content of eSiGe epitaxial growth (EPI) and high boron concentration

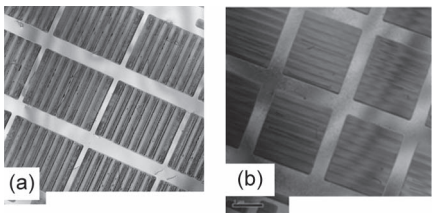

Fig. 5. Planar views of TEM analysis after spike/anneal S/D formation implants at (a) RT or (b) cryogenic temperature. Cryoimplant enables the defectivity reduction by 90%.

via the S/D implant. The subsequent spike rapid thermal process (sRTP) and millisecond (msec) anneal relax the strain by forming misfit and threading dislocations during the lattice regrowth and dopant activation [13], [14]. This leads to a lower hole mobility and a higher junction leakage and, therefore, degrades the device performance. The high-resolution X-ray diffraction rocking curves [14] after eSiGe deposition, S/D implants, sRTP, and msec anneal show that, after sRTP and msec anneal, the SiGe peak is broadened and the peak position shifted with decreased peak intensity. This indicates that most of the strain relaxations were resulted from the recrystallization after the sRTP and msec anneal steps. Such localized relaxation may result in the variation of device drain current.

PVTEM has also been performed to demonstrate the merits of cryoimplant on the eSiGe defectivity (Fig. 5). The cryoimplant results in reduced defect/dislocation by 90%. In fact, the end-of-range (EOR) defects, formed around the amorphization/crystallization interface, are the dominant factor of strain relaxation. Post eSiGe amorphization implant with different Ge energies can modulate the amount of interstitials released from the EOR defects toward the SiGe/Si interface and introduce various degrees of strain relaxation from different damaged eSiGe layers after recrystallization anneal. By using the cryogenic-temperature amorphization implant, the strain relaxation can be improved from RT 28% to nearly no relaxation [14]. The defect reductions in the Si substrate from cryoimplant for lower energy Ge from PVTEM (Fig. 5) as well as XTEM [14] are in agreement with an overall improvement of the dopant variability as revealed in Fig. 3(c). The dislocation defect reduction of the eSiGe by the cryoimplant process results in a smaller impurity out-diffusion and lowers the fluctuation of the channel dopant concentration, comparing to the higher value of the dopant density distribution of the control sample near the drain edge [Fig. 3(c)]. The lower leakage from the cryoimplant can also be explained by a defect-related mechanism. Relaxation of the misfit strain can generate misfit dislocation and threading dislocation which may propagate into the depletion region in the silicon substrate and hence increase the leakage current by reducing the generation lifetime [13], [15]. Therefore, we believe that the elimination of dislocation defects also helps to reduce the defect-related dopant diffusion variability.

In short, by reducing eSiGe defects as well as improving the controllability of polysilicon grain size, cryogenic implant has been demonstrated to be very efficient in reducing the pMOSFET device variability.

IV. Summary and Conclusion

A novel cryoimplant process for the S/D formation has been able to reduce the $V_{\rm th}$ mismatch of pMOSFETs. Experimental results indicate that the boron out-diffusion from the eSiGe S/D in pMOSFET and the amorphized control of polysilicon grain size are the two major advantages in reducing the random dopant fluctuation. This novel cryoimplant technique is very promising for high-performance device design with excellent variability.

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