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Study of La_2O_3/ HfO_2 Gate Dielectric for n-InAs Metal-Oxide-Semiconductor Capacitor

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In this study, we investigate the composite La_2O_3/HfO_2 high k dielectric as the gate oxide for n-InAs metal-oxide semiconductor (MOS) capacitor. The La_2O_3 was used for its high k value and HfO_2 was used as the diffusion barrier and was deposited between La_2O_3 and InGaAs to prevent the Inter-diffusion between InAs and La_2O_3 layers after post deposition annealing (PDA). Finally, we demonstrate the La_2O_3/HfO_2 composite oxide structure as the high K dielectric for n-InAs MOS capacitor with enhanced capacitance for the MOS capacitor.

Introduction

The IC performance improves rapidly in the past decade due to the continuous scaling of metal–oxide–semiconductor field effect transistors (MOSFET). However, as channel lengths are scaled to the 22nm node, conventional Si-based technology comes to the scaling limit. III-V MOSFET is regarded as one of the promising candidates for next generation devices, due to the high electron mobility of III-V materials compared to that of Si. The integration of high mobility Ⅲ-Ⅴ compound semiconductors with high-k dielectrics is very important for further scale down the MOSFET devices for high speed logic applications. Previous study has focused on deposited SiO_2 gate oxides [1]. However, SiO_2 would induce serious gate leakage and high bulk charge densities. Recently, several high-k materials had been studied as gate dielectrics for III-V devices, such as Al_2O_3, HfO_2, and Gd_2O_3 et al [2-3].

The $In_{0.7}Ga_{0.3}As$ MOS devices with Al_2O_3 and HfO_2 as gate dielectrics have been demonstrated [4-5]. Among III-V materials, InAs has the highest electron mobility and also the InAs based device has the lowest turn on voltage. On the other hand, InAs which does not contain Ga atoms will avoid Gallium oxide formation which can't be avoided for $In_XGa_{1-X}As$ layer, the Gallium oxide usually has high surface trap density and is difficult to remove by surface treatment [6]. Therefore, InAs is an excellent candidate as channel material for next generation low power, high-speed III-V CMOS logic applications. Furthermore, HfO_2 and La_2O_3 are known to have dielectric constant 4-5 times higher than SiO_2 [7]. In this study, n-InAs MOS capacitors with HfO_2 and La_2O_3 dielectric films are fabricated and the electrical characteristics of the MOS capacitors are evaluated.

Experiments

The MOS capacitor structure includes: a 10nm n-$In_{0.53}Ga_{0.47}As$ layer, a 3nm n-$In_{0.7}Ga_{0.3}As$ layer and a 5nm n-InAs layer with Si doping concentration of $5x10^{17}$ (cm^{-3}), the structure was grown on a n-InP substrate. For the device process, first, 5nm HfO_2 dielectric layer and 10nm La_2O_3 dielectric layer were deposited sequentially by MBE method on the epi-taxy InP wafer and followed by 500℃ RTA annealing. Then, the W electrode was deposited on the top of the dielectric and Au Ohmic was deposited on the back of the substrate to form the MOS capacitor.

Results and Discussion

The interface of the HfO_2/n-InAs MOS capacitor was investigated by cross-sectional transmission electron microscopy (TEM), and the interface area is as shown in Figure 1(a). Compared to the HfO_2/n-$In_{0.53}Ga_{0.47}As$ MOS capacitor (Figure 1(b)) with similar process conditions, there is no obvious interface oxide layer between HfO_2 and n-InAs layer. The oxide layer at the HfO_2/n-$In_{0.53}Ga_{0.47}As$ interface was identified as gallium oxide, which was absent at the interface of HfO_2/n-InAs MOS capacitor as can be observed from Figure 1(a).

Figure 2 shows the gate leakage current of the La_2O_3 (10nm)/HfO_2 (5nm) n-InAs MOS capacitor. Lower leakage current was obtained by inserting the HfO_2 barrier layer. Less than $3x10^{-6}$ (A/cm^2) of leakage current was observed. The capacitance enhancement in the accumulation region due to the addition of La_2O_3 was observed. The increase of the capacitance from 0.71 ($\mu F/cm^2$) to 1.26 ($\mu F/cm^2$) was observed as compared to pure HfO_2 n-InAs capacitor. The composite dielectric capacitor also shows small frequency dispersion with strong inversion property as shown in Figure 3.

Conclusion

The La_2O_3(10nm)/HfO_2(5nm) n-InAs MOS capacitor exhibits enhanced capacitor capacitance as compared to HfO_2(15nm) n-InAs MOS capacitor The device also shows strong inversion property, small frequency hysteresis, and low gate leakage current. The improvement of the MOS capacitance is believed to be due the high k value of the La_2O_3. materials in the composite La_2O_3/HfO_2 dielectric

Acknowledgments

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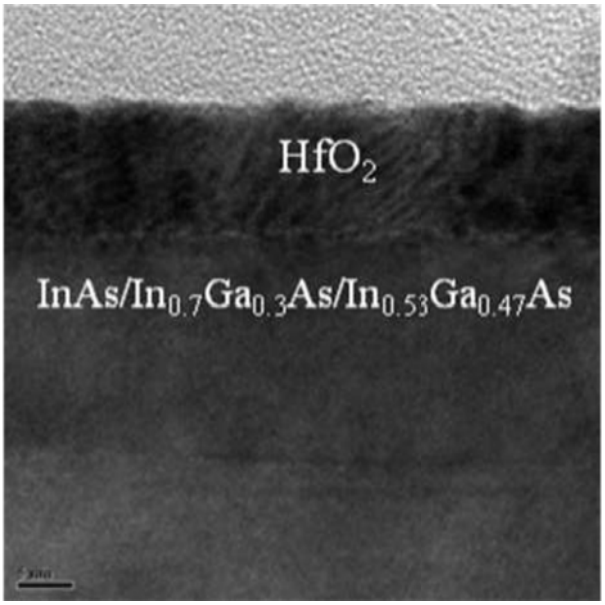
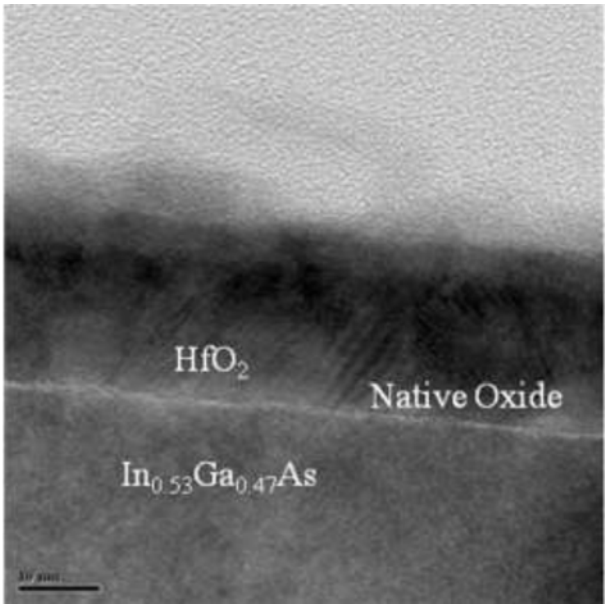
Figures



(a)



(b)

Figure 1. Cross sectional TEM images of (a) the HfO_2/n-InAs MOS capacitor and (b) the HfO_2/n- $In_{0.53}Ga_{0.47}As$ MOS capacitors, with PDA temperature at 500°C.

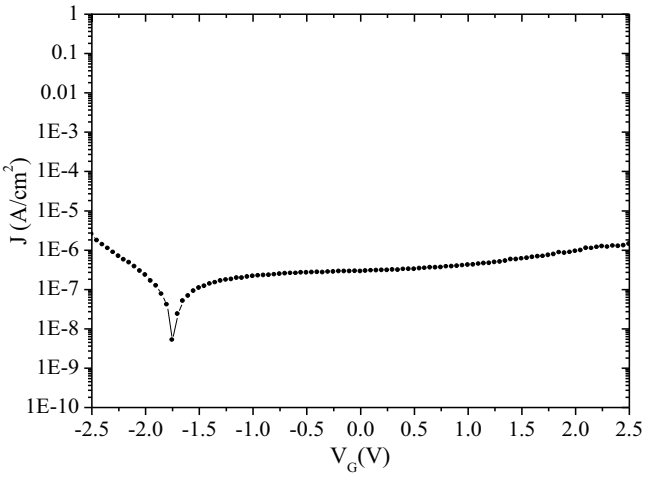
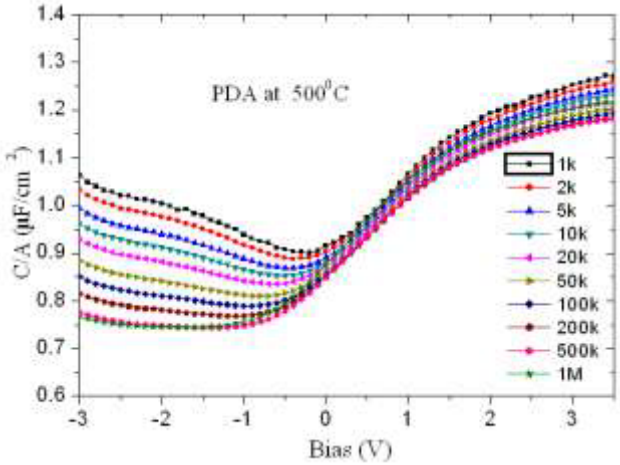
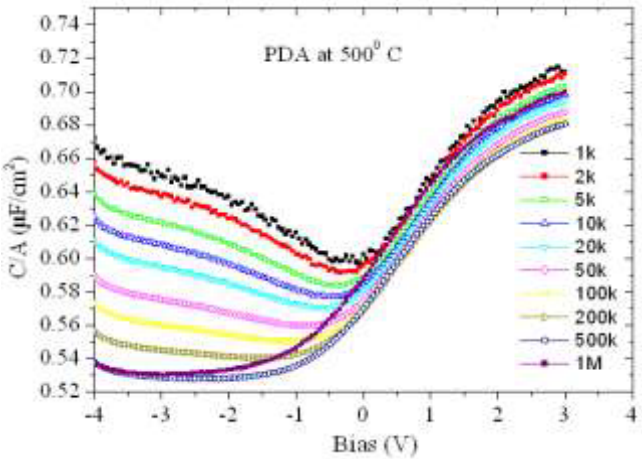


Figure 2. The gate leakage current of the La_2O_3 (10nm)/HfO_2 (5nm) n-InAs MOS capacitor.



(a)



(b)

Figure 3. The C-V characteristics of (a) the composite La_2O_3 (10nm)/HfO_2 (5nm) n-InAs MOS capacitor and (b) HfO_2 (15nm) n-InAs MOS capacitor.