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# The Reliability Study and Device Modeling for p-HEMT Microwave Power Transistors

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In this paper, the commercial 0.5-μm AlGaAs/InGaAs/GaAs pseudo-morphic high electron mobility transistors were subjected to both high-drain voltage and high-temperature stresses for investigating reliability issues. The results reveal that the stress-induced trapping phenomena near two-dimensional electron gas layer should be responsible for the different drain current collapses. The decay level of the DC and the small-signal characteristics increases with the stress voltage and/or the operation temperature. The self-consistent model was established through the de-embedded and the non-linear fitting processes, which can be used to estimate the DC and RF small-signal characteristics degradation under high-drain voltage and high-temperature stress.

## Introduction

Due to advantages of high electron mobility, high breakdown voltage and low conductivity substrate, GaAs-based pseudo-morphic high electron mobility transistor (p-HEMT) is a preferred choice to realize monolithic microwave integrated circuits (MMICs), especially for high power handling capability applications, as power amplifiers (PAs) (1)-(10) and switches (11)-(15). In practical PA designs, transistors are commonly biased at a high supply voltage to acquire high output power and good power efficiency. However, significant hot carrier effect (HCE) generally accompanies with a high lateral electric field and therefore generates microscopic defects interior transistors. In addition, the dissipation power eventually converts into heat and increases the operation temperature. In past researches, performance degradation of GaAs-based p-HEMTs is commonly observed (16)-(19) during high voltage and/or high-temperature operations. With the rapid growing of communication requirements, the p-HEMTs reliability issue has become an important topic for high power MMICs designers.

The degradation mechanisms of p-HEMTs under high-drain voltage stress can be attributed to two major categories. One is the ohmic contact damage due to joule heat generated by a large current (16); the other is the increased interface traps caused by hot carrier bombardments. Interface traps will form the undesired surface depletion and reduce the channel electron density (17), (18) or cause the threshold voltage shifting (19). These degradations not only reduce the DC driving current at the same bias condition, but also affect the RF performance of transistors, such as power gain and linearity. Although major causes of degradation have been clarified, the actual dominated mechanism is still

dependent on bias conditions and device structures, as gate length, gate-recess, surface treatment and layer construction (20). Therefore, the reliability issues of p-HEMTs with different structures still remain to be investigated.

In this paper, we focused to analyze the failure mode of AlGaAs/InGaAs/GaAs p-HEMTs under high-drain voltage and high-temperature stresses, as a real operating environment of PA circuits. Based on the non-linear fitting between the measured and simulated data, the stress-dependent model was also established.

## Experimental Procedure

The test device used for this study is a depletion-mode AlGaAs/InGaAs/GaAs p-HEMT fabricated by WIN Semiconductor. Fig. 1(a) shows the cross-section view of the test device, where an un-doped AlGaAs layer is used for Schottky layer, and Au/Ge/Ni layers are patterned for ohmic contacts. The un-doped InGaAs channel layer is sandwiched by two planar δ-doping silicon layers for high current considerations. The micro-photograph of the test device is shown in Fig. 1(b). The test device has 16 gate fingers, a 0.5μm of the channel length ($L_{ch}$) and a 200μm of the unit channel width ($W_{ch}$). Biased at $V_{gs}$=0V, $V_{ds}$=3V, the average threshold voltage ($V_{th}$), saturation DC current ($I_{dss}$) and trans-conductance ($g_m$) of the test device are -1.6V, 265mA/mm and 165mS/mm, respectively.

Two type reliability tests were applied in this study. One is high-drain voltage stress ($V_{gs}$=-0.5V, $V_{ds}$=9V) in room temperature ambient (T=25°C), the other is medium drain voltage stress ($V_{gs}$=-0.5V, $V_{ds}$=8V) with high temperature (T=125°C). The stress condition of $V_{gs}$=-0.5V, $V_{ds}$=8V, T=25°C was also used as a control condition in comparison with the acceleration rate of high-temperature stress (HTS) and high voltage stress (HVS). The stress time for each condition is 18000 minutes. Before and after stress, the DC characteristics are measured by HP4156. The RF small-signal and large-signal performances were observed by HP8510 and ATN-load pull measurement system, respectively. To analyze the influence of stress on the interior device parameters, the non-linear fitting based on the ADS models provided by WIN Semiconductor was performed to establish the stress-dependent model.

## Result and Discussion

Fig. 2 compares the $I_d$-$V_d$ characteristics of the fresh and the stressed devices. The drain current shows less degradation in the device under the stressed conditions of $V_{gs}$=-0.5V and $V_{ds}$=8V, which is ascribed to trap-related effect on the drain side. It is thought that the presence of defect traps near the two-dimensional electron gas (2DEG) may lead to the drain current instability due to charge filling under the constant drain voltage stress. In contrast, a serious drain current collapse occurs under constant stressed $V_{ds}$ of 9V (HVS). This large current collapse can be attributed to the ohmic contact degradation, since the on-resistance ($R_{on}$) at the linear region significantly increases but the $I_{dss}$ in high $V_{ds}$ and high $V_{gs}$ region shows less degradation. On the other hand, the device was also stressed by $V_{gs}$=-0.5V and $V_{ds}$=8V with high-temperature of T=125°C (HTS). An apparent current collapse was observed in HTS condition, even the stressed device is biased at high-drain voltage. It can be seen that the current collapse in low $V_{ds}$ bias may result from ohmic contact degradation as expected, but the lowered drain current in high

$V_{ds}$ bias is seemly related to stress-induced defect formation in the drain side or near the 2DEG channel.

Fig. 3 shows the trans-conductance ($g_m$) degradations of the test devices under HVS and HTS. The $g_m$ shifting toward positive gate bias was observed, which can be attributed to the non-uniform current collapse in the drain region. In addition, the apparent $g_m$ variation was also observed in low $V_{gs}$ bias, rather than high $V_{gs}$ bias. Thus, the destructive failure mechanism caused by high-voltage or high-temperature stress should greatly affect the channel trans-conductance due to additional defect traps formation in the drain region. Although the stress-induced $\Delta V_{th}$ may also cause the trans-conductance shifting, the observed small quantity of $\Delta V_{th}$ less than 100 mV cannot completely explain such significant $g_m$ profile shifting.

Fig. 4 shows the output power at 1-dB compression point ($P_{out,\ 1dB}$) decline of the test devices under HVS and HTS. Under a long-time stress, the $P_{out,\ 1dB}$ of HTS condition shows a small variation due to the saturation phenomena of charge trapping. It also implies that the influence of stress-induced defects on large-signals' linearity is complicated. In this study, we only focused on the change of small-signal characteristics after stress, since the small-signal characteristics have strong dependence on the first-order properties of transistors and directly relate to the DC operation point. In addition, the long-time stress process inevitably changes the input and the output impedances of the transistor. In real high-frequency amplifiers, the impedance variation may cause the matching network to lose original function, thereby resulting in the degradation of power gain.

To analyze the impact of HTS and HVS on DC and small-signal characteristics, the ADS device model provided by WIN Semiconductor was used to model the DC characteristics and the S-parameters of the fresh devices. Although the original interior parameters of transistors can be extracted through this foundry model, adding variable resistances at the drain and the gate terminals are sometimes required due to the small process variation of different test devices. The after-stressed DC characteristics can be modeled by adjusting parameters related to equivalent electron mobility ($\mu_{eff}$), saturation voltage ($V_{sat}$), and $V_{th}$. The simulated $I_d$-$V_d$ curves and $g_m$ profiles are plotted in Fig. 2 and Fig. 3, respectively.

To analyze the change of the small-signal characteristics, we used a $\pi$-type equivalent circuit to model the test device, as shown in Fig. 5. The de-embedded process with the measured S-parameters from the open, the short and the through kits is required to remove the parasitic effects of the probing pads and the outward metal connections before fitting. In addition to adjusting the physical parameters used in the DC characteristics modeling as mentioned, here we assume that the stress-induced impedance change in high frequency operations can be mainly attributed to the variation of the equivalent resistance at the drain end and the gate-to-drain capacitance. The measured and simulated S-parameters of each stress condition are shown in Fig. 6. It apparently shows that the HTS and HVS lead to the $S_{22}$ shifting and the $S_{21}$ reduction. In real circuit implementations, these variations can cause the gradually degraded output matching and power gain.

In high-frequency amplifier designs, the cut-off frequency ($f_t$) of transistors is an important parameter, which defines that the frequency of the short circuit current gain ($h_{21}$) approaches to one. In general, the common expression of $f_t$ is

$$f_t \cong \frac{g_m}{2\pi(C_{gs}+C_{gd})} \quad [1]$$

where $C_{gs}$ and $C_{gd}$ represent the gate-to-source and the gate-to-drain capacitances, respectively. Therefore, the transistor $f_t$ may decrease due to the degradation of $g_m$ and the increased $C_{gd}$. To obtain the transistor $f_t$, the modeled $h_{21}$ was calculated by S-parameters simulation results, based on the following relation

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \quad [2]$$

while $h_{21}$ is calculated, the corresponded $f_t$ can be obtained by extrapolating $|h_{21}|^2$ to 0dB. The measured and simulated $|h_{21}|^2$ are shown in Fig. 7, where the stressed devices present 2.3, 3.73 and 5.1GHz of $f_t$ degradations for the control, HVS and HTS conditions, respectively. The good agreement between simulated and measured results indicates that the model under HTS and HVS is self-consistent, which can be useful in predicting DC and small-signal performance degradation under long-time operation with high-drain voltage and high environmental temperature conditions.

## Conclusion

We have investigated the DC and RF performance of AlGaAs/InGaAs/GaAs p-HEMTs under high-drain voltage and high-operation temperature stress. The prediction model for DC and small-signal characteristics changes was also established through the accurate de-embedded process and non-linear fitting.

## Acknowledgments

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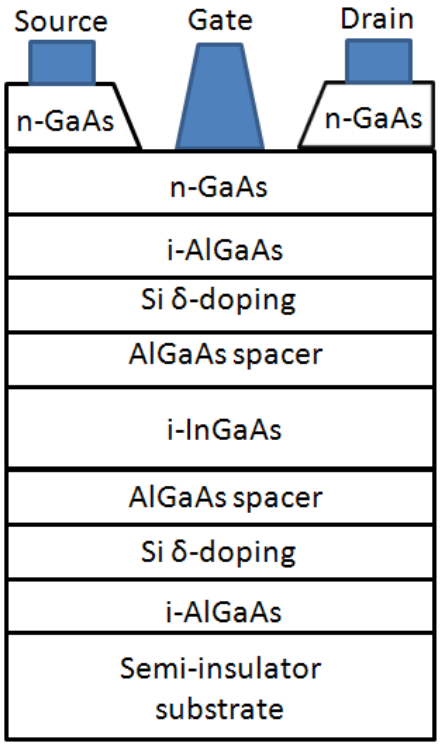


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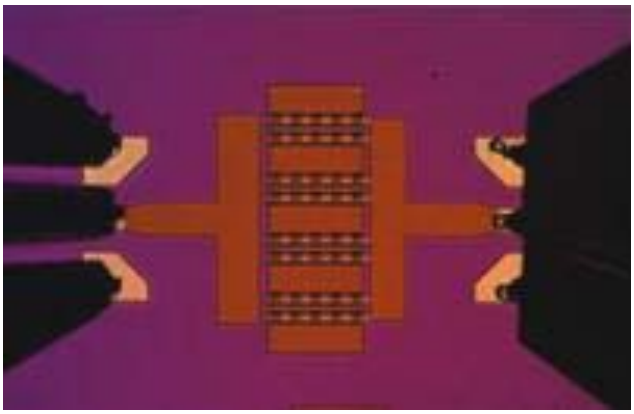
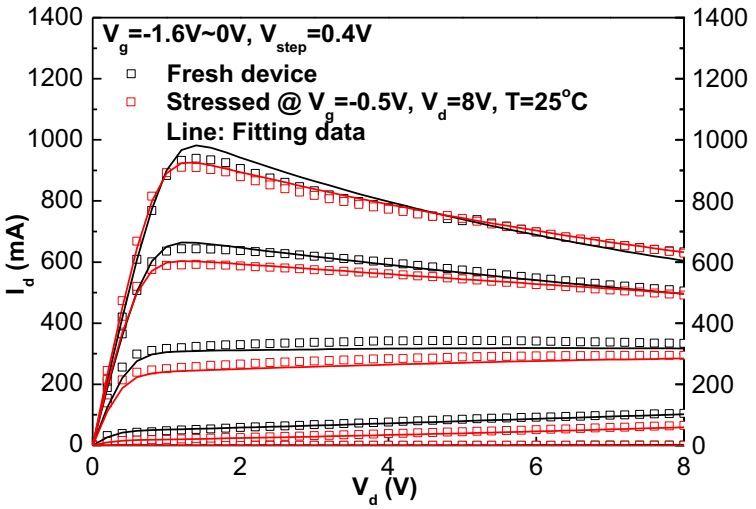


(b)

**Figure 1.** (a) The cross-section view of the test device and (b) the photograph of test device.

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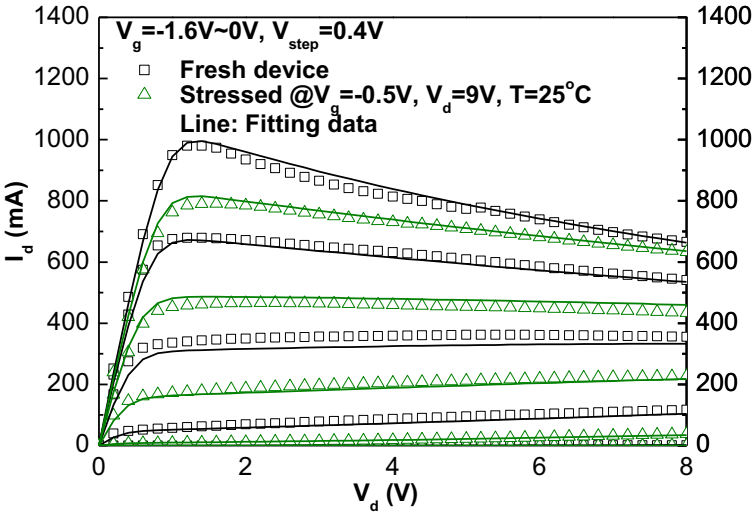


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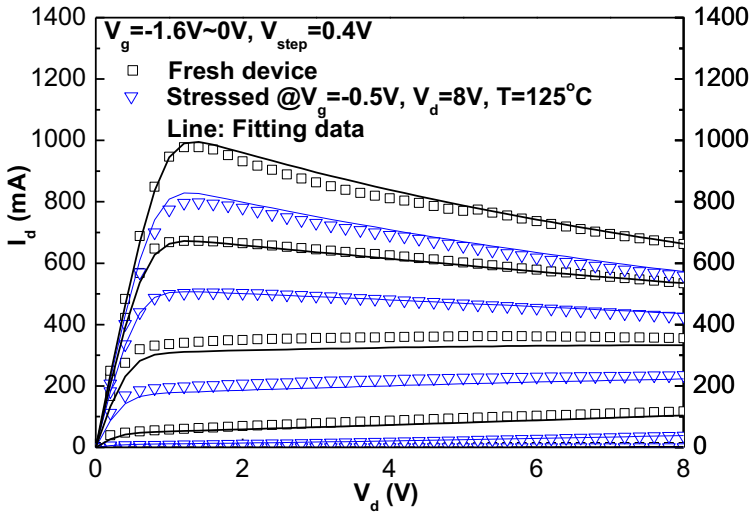



(c)

**Figure 2.** $I_d$-$V_d$ characteristics at the different stress conditions: (a) $V_{gs}$=-0.5V, $V_{ds}$=8V, T=25°C, (b) $V_{gs}$=-0.5V, $V_{ds}$=9V, T=25°C and (c) $V_{gs}$=-0.5V, $V_{ds}$=8V, T=125°C.

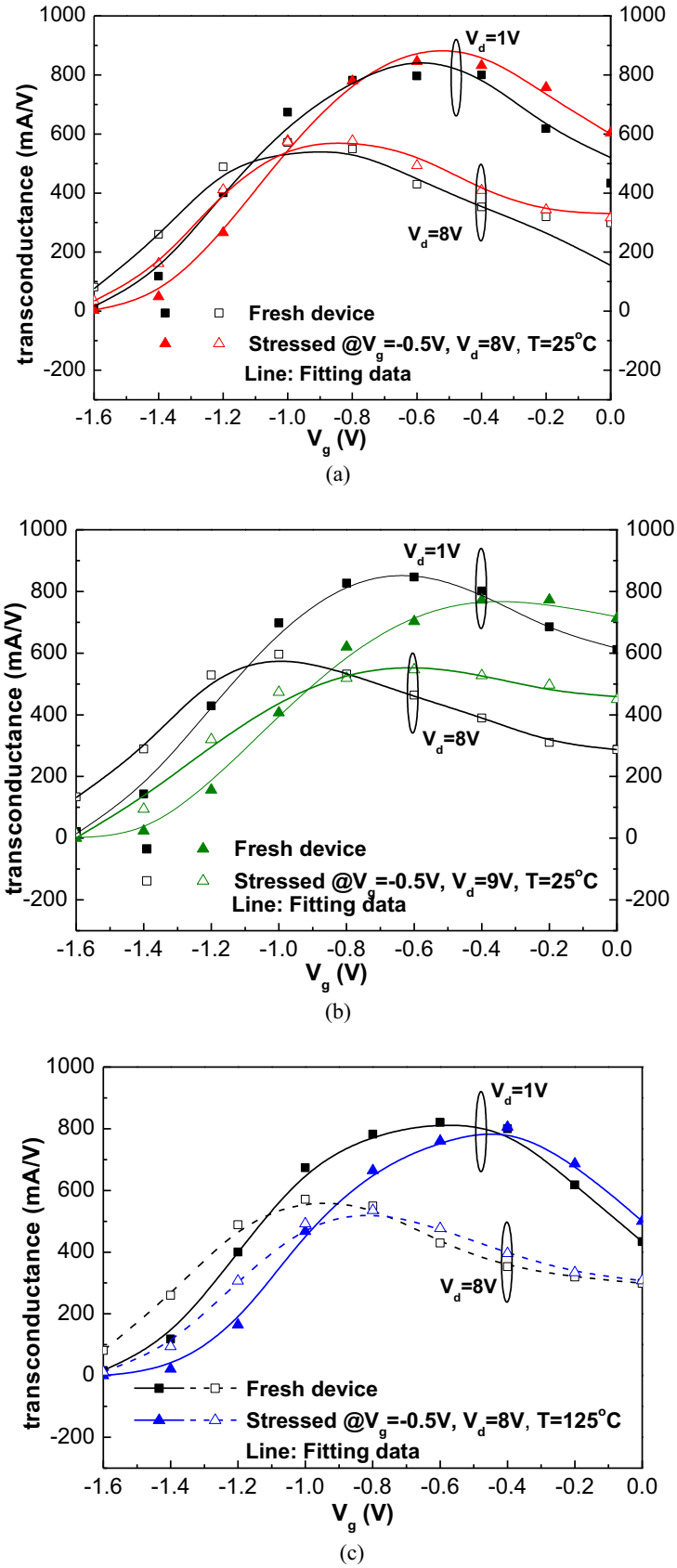



**Figure 3.** The trans-conductance ($g_m$) degradation at different stressed conditions of (a) $V_{gs}$=-0.5V, $V_{ds}$=8V, T=25°C, (b) $V_{gs}$=-0.5V, $V_{ds}$=9V, T=25°C and (c) $V_{gs}$=-0.5V, $V_{ds}$=8V, T=125°C.

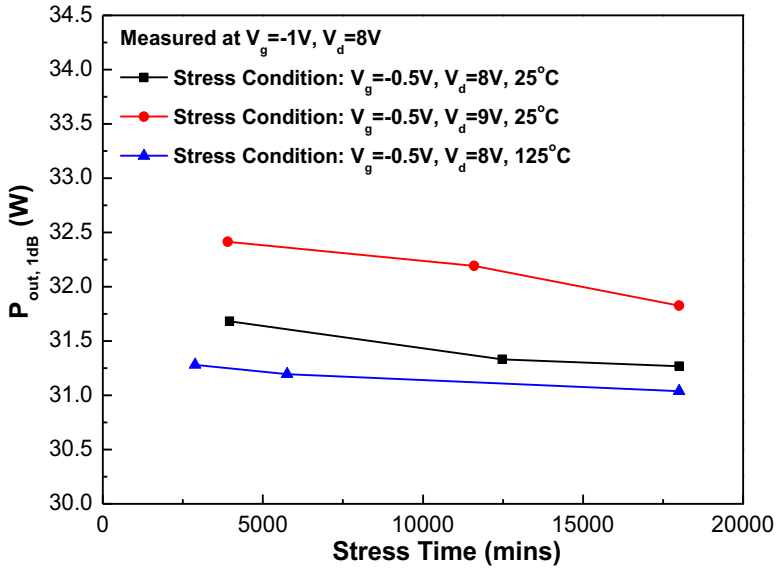



**Figure 4.** The output power degradation at 1-dB compression point of the test devices after stress.

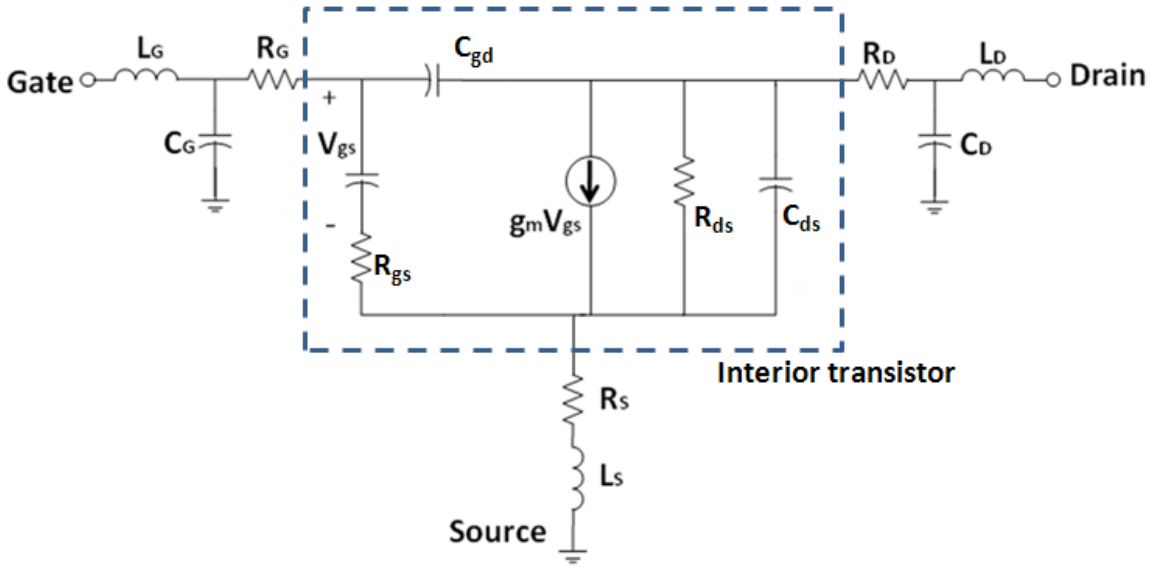
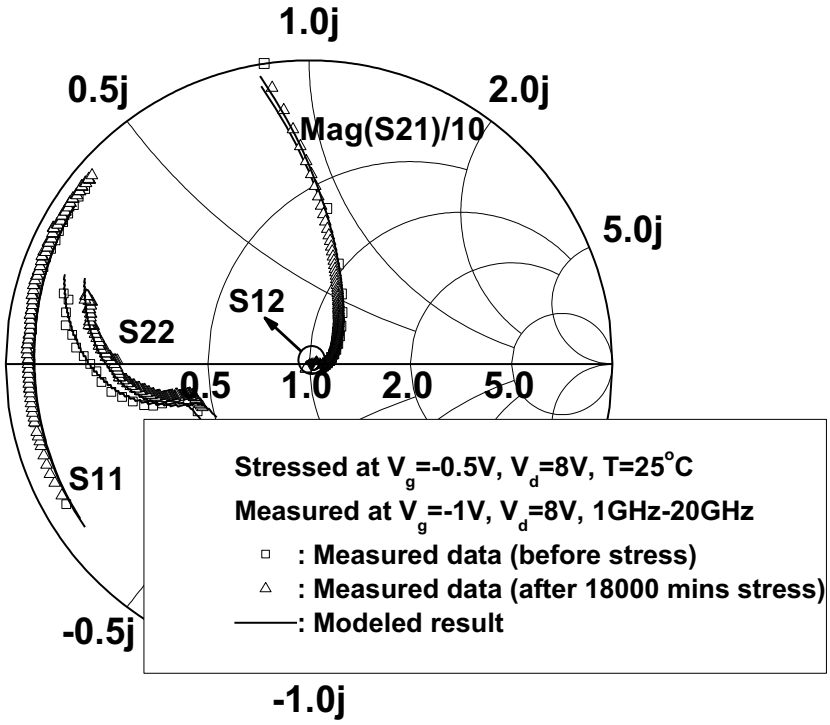



**Figure 5.** The equivalent small-signal model used to analyze high-frequency characteristic degradation of the test devices.

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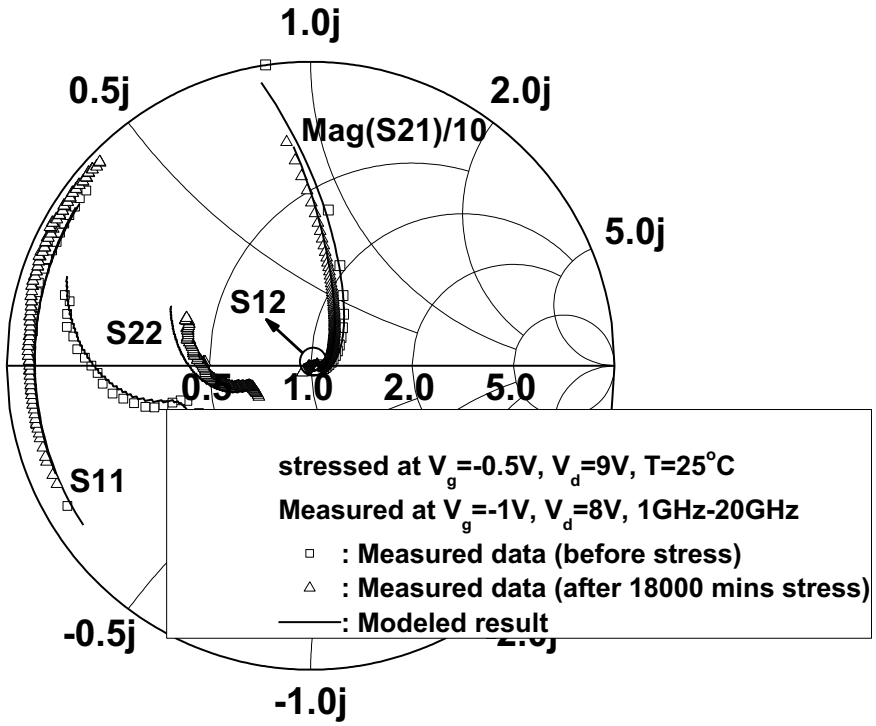


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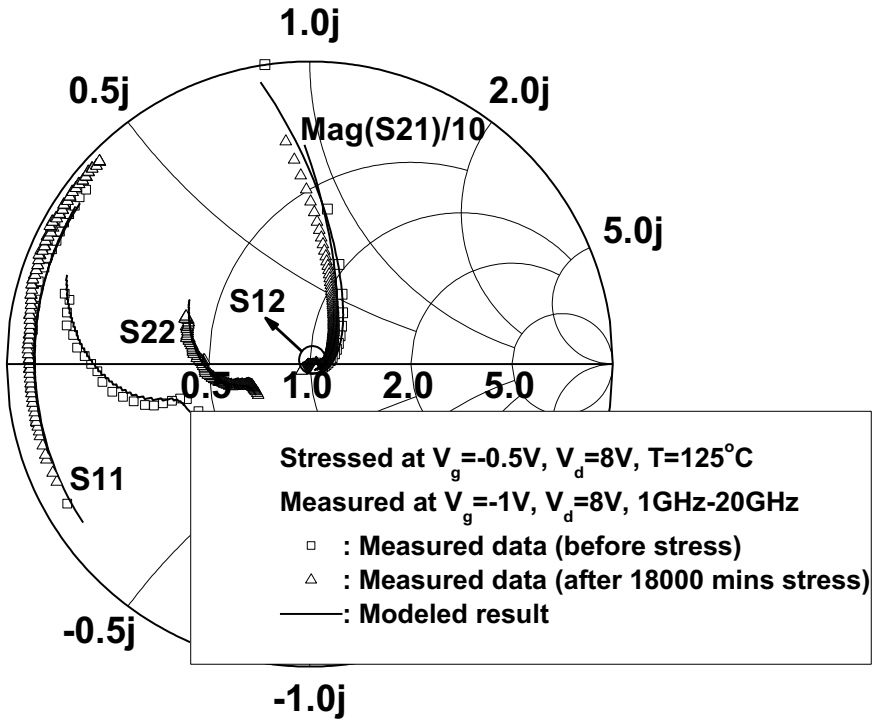
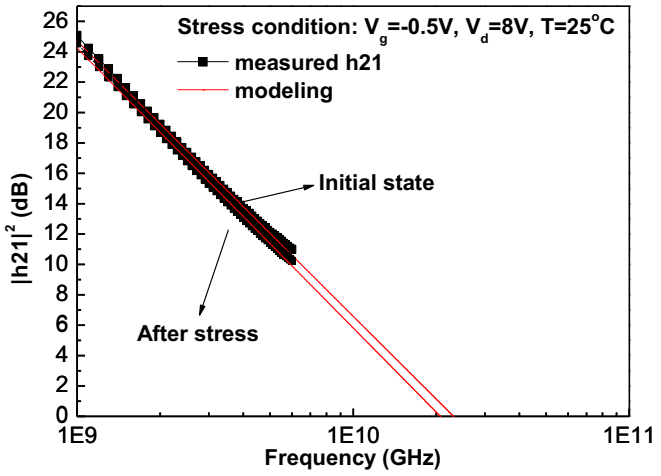



(c)

**Figure 6.** The measured and simulated S-parameters: (a) $V_{gs}$=-0.5V, $V_{ds}$=8V, T=25°C, (b) $V_{gs}$=-0.5V, $V_{ds}$=9V, T=25°C and (c) $V_{gs}$=-0.5V, $V_{ds}$=8V, T=125°C.

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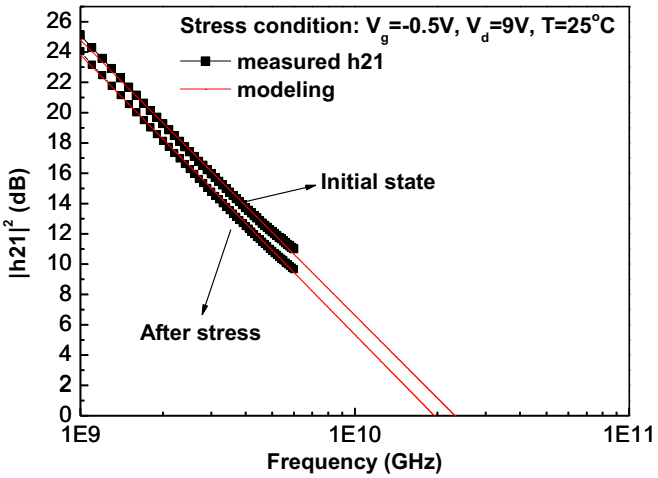


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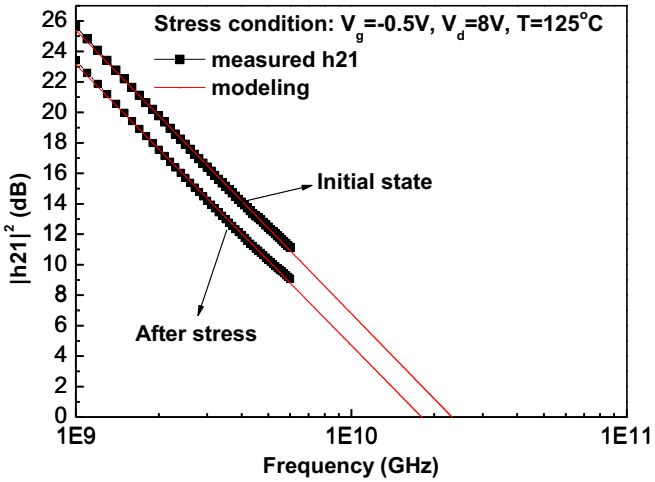


(c)

**Figure 7.** The measured and simulated $h_{21}$: (a) $V_{gs}$=-0.5V, $V_{ds}$=8V, T=25°C, (b) $V_{gs}$=-0.5V, $V_{ds}$=9V, T=25°C and (c) $V_{gs}$=-0.5V, $V_{ds}$=8V, T=125°C.