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Extension of Moore's Law Via Strained Technologies-The Strategies and Challenges

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In order to extend the *Moore's law*, the interests have been devoted to several different areas, such as the use of strained technology, the high-k/metal-gate, high mobility channel materials etc. Among these efforts, strained technology seems to be the most successful one for its development over several generations and more *Moore* becomes the most recent interest. However, the reliability and variability become a great concern.

In this paper, we will first give an overview on the strain-silicon technology, such as eSiGe, eSi:C, stress memorization technique (SMT), dual stress liners (DSL), and replacement high-k/metal-gate (RMG) process, after the 90nm CMOS generation. Then, the reliability and the design guideline for a trade-off between performance and reliability will be addressed. A technology roadmap in terms of the ballistic transport theory will be outlined. Then, the variability of the strained CMOS devices with focus on the experimental discrete dopant profiling will be demonstrated. Finally, the strategies and challenges of strained-silicon devices on advanced 3D device structure and IC will be discussed.

Introduction

For recent manufacturable CMOS technologies to extend the *Moore's law* [1], the interest in the strain engineering has been speed-up in recent years as a need in a rapid scaling of CMOS devices for high speed and low power applications. Among those reported strain schemes [1-10], process-induced stress technique such as SiGe eS/D [2-3], Si:C eS/D [4-5], capping layer [6-7], DSL(Dual Stress Liner) in a CMOS process [8-9] , strained-SiGe channel devices [10-11], stress memorization technique (SMT) [12], substrate engineering, and hybrid substrate technology [13] have been attractive for high speed and low power logic CMOS technologies. As a consequence, strain-silicon technology has lasted for several generations beyond the 90nm generation node and it now comes to the cross-road of whether we want to use the planar CMOS structure for 20nm-16nm node and beyond. Strained technology seems to be one of the efficient approaches whatever the changes of device structure might be. Although some exciting strain schemes may achieve current enhancement that are expected, the reliability issues of strain CMOS devices need to be taken into consideration in the using of strained structures [14-15]. Also, with the further scaling of device dimensions, variability becomes increasingly important. More efforts on the study of strain-induced reliability,

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variability [16-17], device drain current enhancement etc., become more interested and raised more attention.

In this paper, the strain-silicon technology since 90nm generation node will be first introduced. Then, the reliability and the design guideline for a trade-off between performance and reliability will be addressed. A technology roadmap in terms of the ballistic transport theory will be demonstrated [18-19]. Then, the variability of the strained CMOS devices will be discussed, in which a more recently developed discrete dopant profiling in the monitoring of the Ge and Carbon out-diffusion will be demonstrated [20]. Finally, the strategies and challenges of strained-silicon device design with the trade-off between reliability, variability, and performance will be discussed.

Fundamentals of Strain Technology

Reasons on Choosing Strain Materials

For the advanced logic technologies, such as CPU, high speed graphics IC, DSP(Digital Signal Processor) etc., we need a higher current, called drain current I_{dsat} or on-current, I_{on}. This current is described by $I_{dsat}= \mu C_{ox}(W/L)[V_{GS}-V_{th}]^2$. In order to achieve a higher I_{dsat}, three different approached can be used. First is by the using of device scaling in channel length L which is limited by the lithography. The second one is using a thinner gate oxide to achieve a larger unit area capacitance, C_{ox}, or by using a high-k material with larger dielectric constant while a smaller EOT(Equivalent Oxide Thickness). The last one is through the enhancement of the device mobility, μ, Strained technique with the mismatch of two different lattice materials which provides such an opportunity to serve this purpose. Basically, there are different kinds of strain, e.g., tensile strain and compressive strain, depending on the lattice constants of two different materials. For example, an epi-Si layer grown on a SiGe material (with larger lattice constant), a tensile stress is exerted on the top-Si layer which causes a so-called tensile strain, Fig. 1(a). In another case, if a SiGe(with larger lattice constant than the silicon) is used in the pMOS device, the source/drain will induce a compressive strain to the channel, Fig. 1(b).

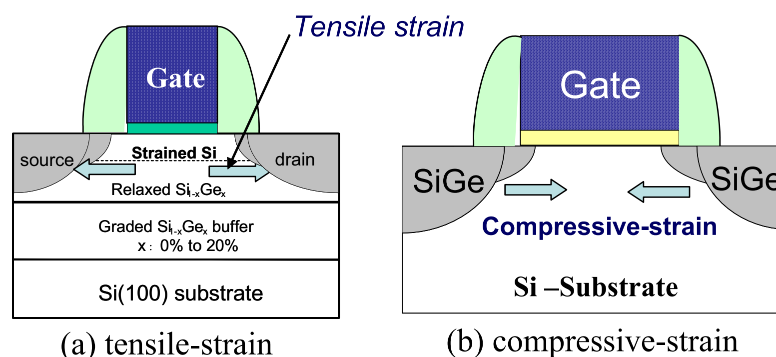

Fig. 1 (a) Example of tensile strain induced in the channel with an epi-Si layer (served as channel) on top of a SiGe/Si-substrate layer. (b) The compressive strain with SiGe as the source/drain of a pMOS where a compressive strain is induced in the channel, where SiGe has a larger lattice than the Si one.

The process of strain technologies is simple such that we can easily achieve the purpose of increasing the channel mobility and the I_{ON} as well. As a consequence, it has become the mainstream technologies for 90nm CMOS and beyond. In general, the strain technology can be divided into two different categories, one is the substrate-strain based, the other one is the process-induced strain. The former is more straightforward by using a

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planar strain(two-dimensional strain) material to induce the strain [10-11], e.g., Fig. 1(a). The latter, Fig. 2, is more popular since the process is simple and easy to make. Uniaxial strain can be achieved by trench isolation, silicide, nitride capping layer [6-9], and recessed S/D etc. [2-5]. Depending on process types and device structures, these devices exhibit mobility enhancement with a factor of up to 100% or even higher over that of conventional process/device structures.

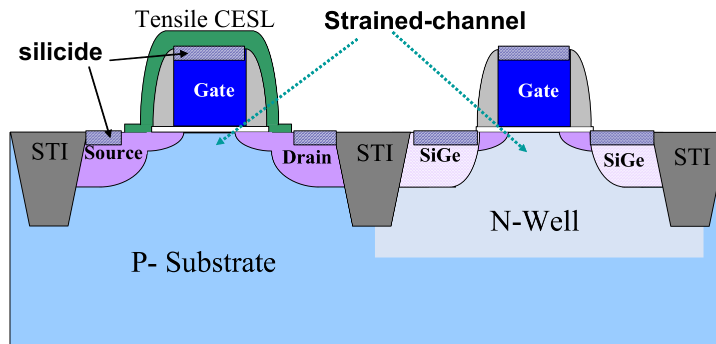

Fig. 2 Basic schemes of the CMOS structure using process-induced strain (locally), in which CESL is more popular for nMOSFET(tensile strain) and SiGe is used for pMOSFET (compressive strain).

Local Strain versus Global Strain

From the point view of the strains, there is another category to tell the differences between those aforementioned technologies, local strain and global strain. Normally, if the strain is on one direction, we call it **local strain**, while on the other hand, a two-dimensional (areal) strain on the device is called **global strain**. Table 1 lists various schemes which can be categorized into **global**, **local**, and **hybrid** strains. The comparison of local and global strains along with the pros and cons of the technology are also provided.

The **global** strain crated a biaxial strain through making an epi-grown strain layer on top of the substrate, as shown in Fig. 3. It requires a special graded buffer layer to connect the strained Si(the channel) and the substrate, This substrate can be silicon or SOI(Silicon-On-Insulator) wafers. It involves SiGe in most of the cases, and therefore, Ge out-diffusion becomes a great concern. Also, significant dislocation issues are emerged due to a large area strain. Moreover, this technique has an inherent disadvantage of high manufacturing cost. The **local** strain is mostly unaxial strain which is induced through the process. There are many stressors to implement local strain, such as SiGe eS/D[2-3], Si:C eS/D [4-5], and capping layer[6-9]. The most typical process-induced strain is shown in Fig. 4(a) with a Contact Etch Stopped SiN Layer (CESL) [6-7]. This SiN-cap layer can induce the tensile or compressive strain such that the tensile strain can be used for the nMOSFET and compressive strain for the pMOSFET. This comprises the so-called DSL(Dual Stress Liner) in a CMOS process [8-9], Fig. 4(b). Their mobility enhancements are more conservative, i.e., with less I_{ON} current enhancement, in comparison with the global strain technology. Different from global strain, dislocation and lattice misfit issues are prevented in the local strain. Finally, it is low cost for manufacturing simplicity. The last one is **hybrid** substrate strain [13]. Hybrid strain involves a combination of nMOSFET and pMOSFET with different substrate orientations for mobility enhancement schemes. But it faces the big challenge of complex manufacturing.

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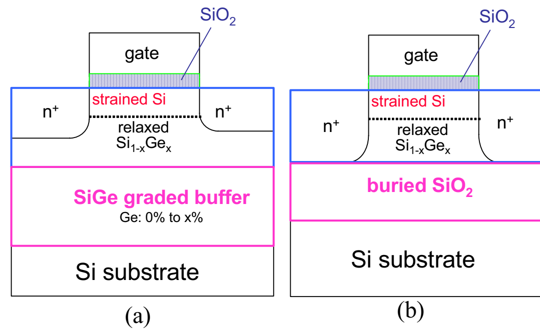
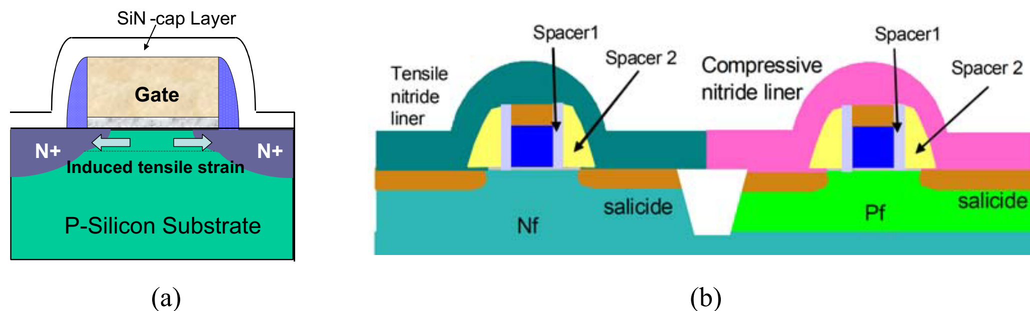
	Global	Local	Hybrid
Strain Direction	**biaxial**	**uniaxial**	mixed
Manufacturing	**Wafer based** (epi-layer)	**Process induced**	mixed
Examples	1. SiGe on Substrate 2. SSOI	1. SiN-Capping layer 2. eSiGe for pFET 3. eSiC for nFET	1. (100) for nMOSFET 2. (110) for pMOSFET
Pros	Good current enhancement	**1. Few Defeats** 2. Low cost **3. Many stressors**	**Optimized for CMOS Design**
Cons	**1. Many Defects** 2. High cost 3. Hard to make	**Process issues involving new materials/processes**	**Challenge in manufacturing**

Table 1 The comparison between local strain and global strain.



(a) (b)

Fig. 3 Global strain: (a) The strained Si/SiGe structure on bulk-Si substrate and (b) the strained Si/SiGe on SOI substrate.



(a) (b)

Fig. 4 Local strain: (a) The contact etched stop layer (CESL) and (b) the structure of tensile/compressive CESL on n- and p-MOSFETs respectively [6-7].

Various Strain Engineering

In the 2007 ITRS report [21], it was pointed out that the strain silicon technology has to enhance the driving current of CMOS devices to 180% ultimately. As aforementioned, there are many strain options for us to choose from. Depending on process types and device structures, these devices exhibit different degrees of mobility enhancement comparing to conventional process/device structures. Followings are a simple review on those popular strain techniques such as: (1) process-induced strain with CESL [6-7], DSL(dual stress liner)[8-9], embedded SiGe (eSiGe) [2-3], embedded Si:C (eSi:C) [4-5], stress memorization technique (SMT)[12] etc. (2) global strain with strain-Si/SiGe and the hybrid techniques with different substrate orientations[13]. More recently, with the advent of high-k/metal-gate (HK/MG) also brings in additional strain effect with its metal

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gate stressor (MGS) and replacement gate (RMG) process in the gate-last process [22].

The Process-Induced Strain

The MOSFET with a strained-Si/SiGe channel has been the prime initiative for mobility enhancement schemes. Figs. 5(a) and (b) show the n-MOSFET and p-MOSFET drain current and mobility, respectively [15]. It shows that Si/SiGe n-MOSFET mobility has been increased 70% over that of bulk device. However, there is one disadvantage of the SiGe strained devices in that p-MOSFET does not get much gain.

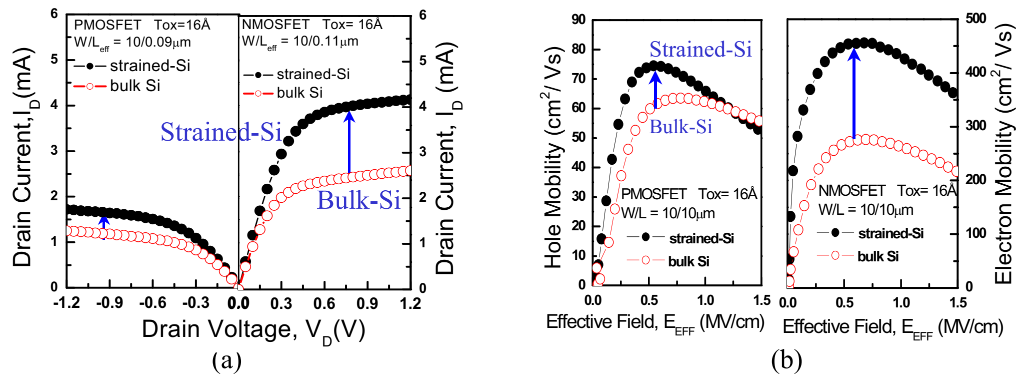

Fig. 5 (a) The comparison of the I_D current for strained-Si and bulk-Si devices, (left) p-MOSFET (right) n-MOSFET. (b) The comparison of the mobility for strained-Si and bulk-Si devices, (left) p-MOSFET, (right) n-MOSFET.

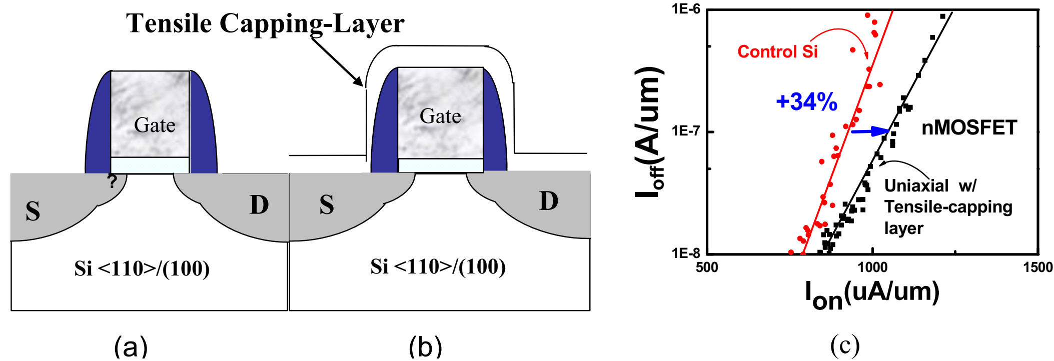

Fig. 6 The cross-sectional view of (a) the control-Si device and (b) Si channel <110> with tensile-cap layer. (c) The comparison of the Ion-Ioff current enhancements for nMOSFETs. Tensile-cap device shows 34% current gain over that of the control-Si device.

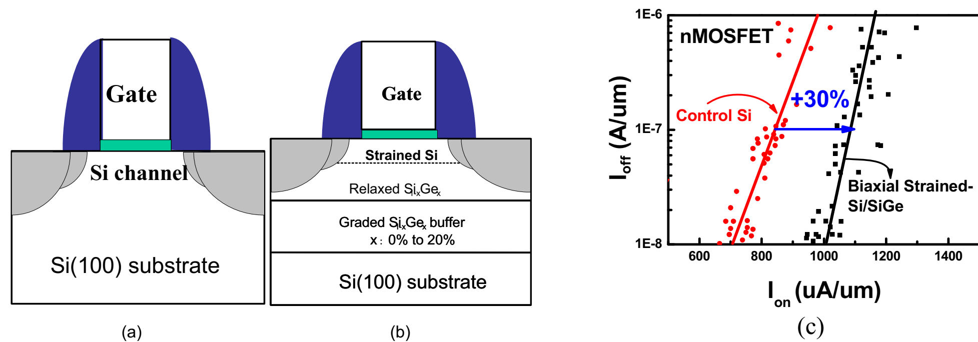

Fig. 7 (a) The cross-sectional view of (a) control-Si device and (b) biaxial strained-Si/SiGe nMOSFET. (c) The comparison of the Ion-Ioff current enhancements for nMOSFETs. The biaxial-strain shows 30% current gain over that of the control-Si device.

By comparing to the biaxial-strain in Fig. 5, if instead we use the CESL in nMOSFET, comparable current enhancement can be achieved. Fig. 6 shows the comparison of the

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drain currents between uniaxial-strain (CESL) and the control ones. And, Fig. 7 shows the comparison of the I_{on} currents between biaxial, strain-Si/SiGe nMOSFETs and the control ones. Considering the simple process involved in the CESL strained devices, the uniaxial strain seems to be a better approach.

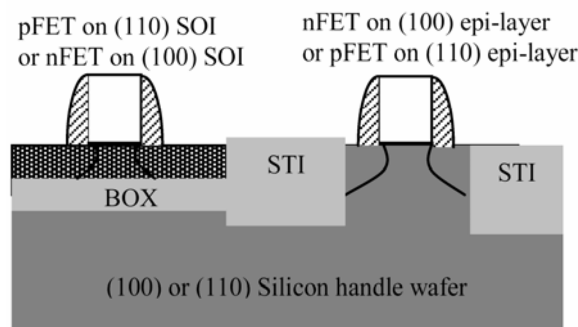

Fig. 8 The hybrid substrate technique with nFET and pFET on different substrate orientations [13].

The Hybrid-Substrate Engineering

In order to maintain a simultaneous current gain in a CMOS technology, we can take advantage of the n-MOSFET on (100) substrate while p-MOSFET is made on (110) substrate. This constitutes the hybrid substrate technology[13] as shown in Fig. 8. Here, p-MOSFET mobility can be more than doubled on (110) Si-substrate with current flow on the (110) direction comparing to that along the (100) direction. Also, electron mobility is the largest along the (100) direction. As a result, an idea of the so-called hybrid substrate CMOS technology becomes a feasible solution.

For a real demonstration of the results [23], Fig. 9 shows the drain currents and mobilities for both nMOSFET and pMOSFET on (100) and (110) substrates. It reveals that pMOSFET has a 50% enhancement in its mobility using (110) substrate, while nMOSFET mobility is reduced. The result is just the opposite to that of strained-Si devices.

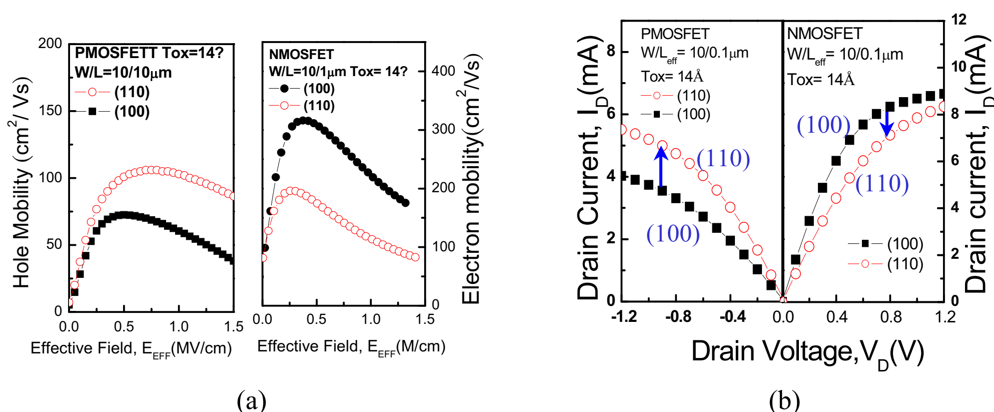

Fig. 9 (a) The comparison of the mobility for (110)and (100) substrate devices, p-MOSFET (left) and n-MOSFET (right). (b) The comparison of the I_D current for (110) and (100) substrate p-MOSFET (left) n-MOSFET (right).

The Raised Source/Drain Engineering

As aforementioned, uniaxial strain offers several advantages over the biaxial strain. In more recent years, different techniques have been adopted for n-channel MOSFET and p-

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channel MOSFET indenpendently, with an attempt to provide more flexible tuning of the strain effects in terms of design and manufacturing purposes. In p-MOSFET, hole mobility can be boosted by the usage of silicon-germanium (SiGe) stressor in the source/drain(S/D)[2-3], which induces uniaxial compressive-strain effect into the channel, via the lattice-mismatch induced strain between the interface of SiGe S/D and silicon channel regions. On the other hand, in nMOSFET [4-5], silicon-carbon (Si:C) in S/D with an induced tensile-strain effect becomes feasible as a counter part of pMOSFET in the CMOS structures [2-3].

For the design of pMOSFET, comparisons between the bulk, SiGe on channel (biaxial,) and SiGe on S/D(uniaxail) devices, Fig. 10, have been compared. The I_{on}-I_{off} characteristics of both the splits and control sample are given in Fig. 10. We can find SiGe on S/D devices exhibit high driving current enhancement comparing to SiGe in the channel with the same value of I_{off}, that is because the stressor of SiGe on S/D devices is closer to channel than that of SiGe on channel devices. The closer the stressor is to the channel, the higher the effect of the strain becomes. Hence, SiGe on S/D devices (uniaxial) may achieve a much higher I_{on} than that of SiGe channel (biaxial) devices.

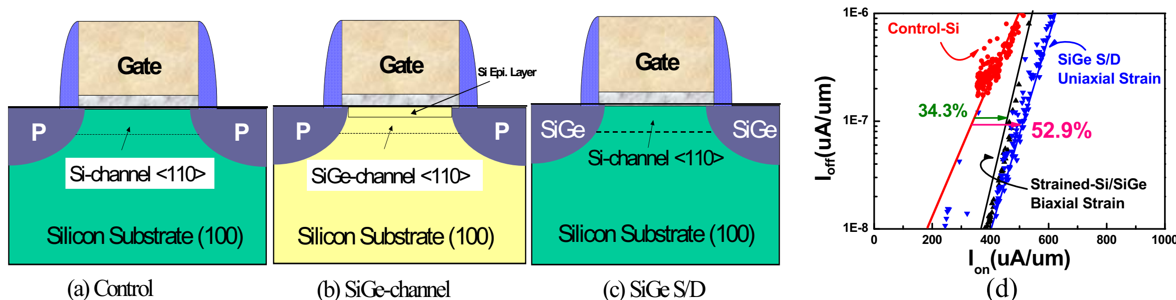

Fig. 10 The cross-sectional view of (a) bulk-Si device and (b) SiGe-channel, and (c) SiGe Source/drain compressively strained pMOSFETs. (d) Comparison of the Ion-Ioff current enhancements for pMOSFETs shown in (a)(b)(c). Note that SiGe S/D structure (uniaxial) exhibits a largest I_{on} current enhancement.

As a counterpart of the raised SiGe S/D pMOSFET, raised Si:C S/D has also been able to enhance the performance of nMOSFETs. The Si:C source/drain are formed by implant with Solid Phase Epitaxy (SPE) anneal [4] or in-situ doped [5]. Excellent performance can be achieved, Fig. 11. Comparing to the bulk device, it revealed good drive current I_{ON} (+27%), high $I_{D,sat}$ current (+67%), enhanced channel mobility (+105%), in a real practice of the poly-gate 40nm-node Si:C/eSiGe S/D CMOS technology.

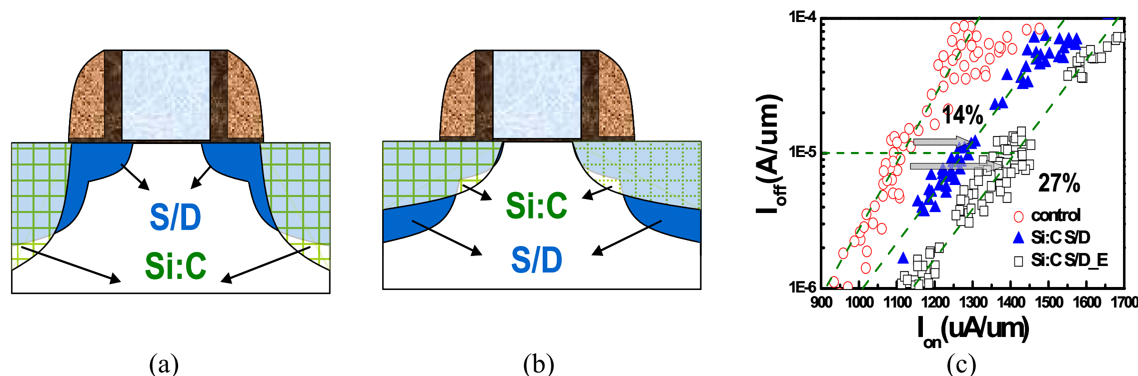

Fig. 11 The Si:C S/D nMOS devices with (a) a doped Silicon in the drain/source extension region, (b) a Si:C in the extension region which can bring in more strain effect to the channel. (c) The comparison of the I_{on}-I_{off} characteristics among two different structures in (a), (b), and the control device.

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The Replacement Gate HK/MG

More recently, by taking the advantage of a gate last high-k/metal gate process, the replacement gate can induce the stress to the channel with the so-called SMT(Stress Memorization Technique) [12, 24], which can really provide a good integration down to the 20nm node CMOS technology [25]. As a consequence, this similar technology can also be applied to the SiGe pMOSFET with the above SMT technique for achieving a very high I_{on}> 1mA/um.

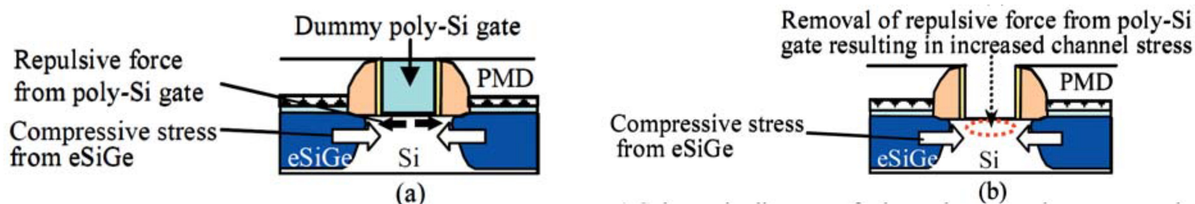

Fig. 12 The schematic of gate last process by (a) a dummy poly-Si gate is formed, and then (b) the poly-Si gate is removed and induced an increased strain in the channel [24].

Benchmarks

Table 2 summarizes several reported strain schemes, including uniaxial, biaxial, and hybrid schemes [4,7-8,10-13, 26-32]. Some exciting strain schemes may achieve current enhancement near 80%.

	nMOS							pMOS					Hybrid	
Strain Direction	**Uniaxial**					**Biaxal**		**Uniaxial**				**Biaxial**		
Strain Approach	CESL (tensile)	SMT (tensile)	FinFET (Si:C S/D+CESL)	Si:C S/D Extension	Tungsten Liner for HK	Relaxed SiGe sub	SSOI	SiGe on S/D +EDB	Replace -ment Gate for HK	CESL (compressive)	Diamond -like carbon cap	SiGe-channel + cap	T-CESL for nFET C-CESL for pFET	pFET on (110) nFET on (100) substrates
?I_{on}(%)	+12	+12%	+56	+27%	+17%	+13	+18	+25	+16%	+14	+69	+80	nFET→60% pFET→55%	pFET →45% nFET→ 20%
Lg(nm)	37	35	25	40	45	60	25	45	32	60	70		40	28
EOT(A^0)	18.8	N/A	20	12	9	22	17.5 (TiN/HfO_2)		8.5	14				
Ref.	[7]	[12]	[26]	[4]	[27]	[10]	[28]	[29]	[30]	[31]	[32]	[11]	[8]	[13]

Table 2 Several reported strain engineering schemes developed in the past ten years.

The Carrier Transport of Strained Devices

Carrier Transport- the Basics of Strain Technologies

As is well known, carrier transport behaves differently from the conventional theory as we reach the sub-100nm domain. From the scattering theory [18], the two fundamental transport parameters, the **backscattering** (or **ballistic efficiency**) and the **carrier injection velocity** from the source side, are strongly dependent on the strain techniques. The drain current for a device in the ballistic regime is governed by

$$I_{D,sat} = WC_{eff}V_{inj}\,B_{sat}\,(V_G\text{-}V_T) \qquad (1)$$

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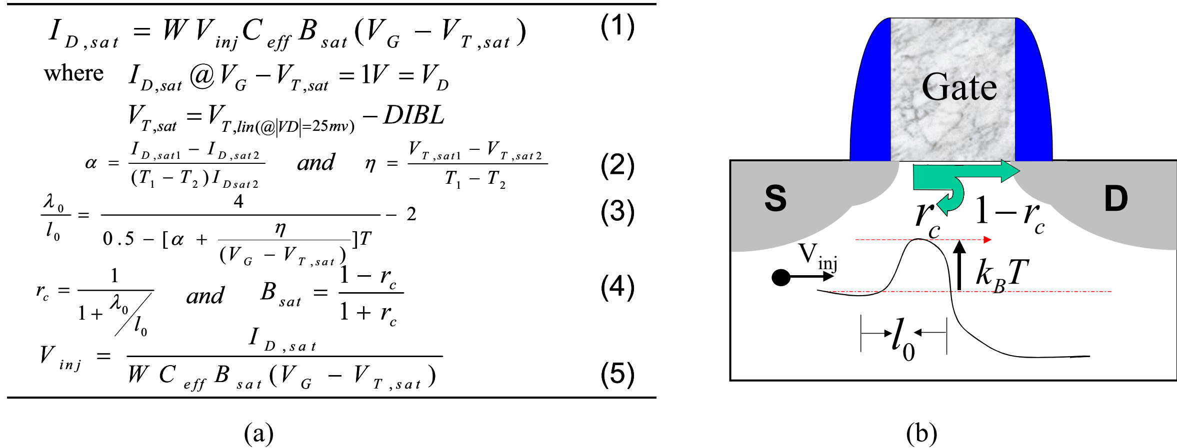
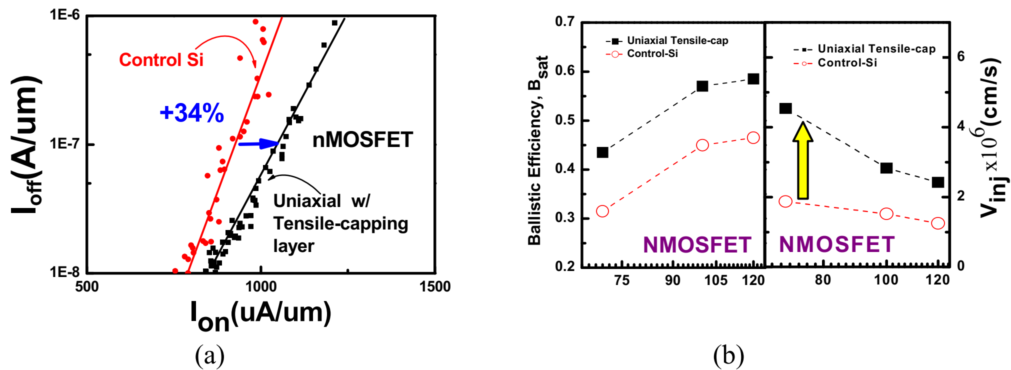
where V_{inj} and B_{sat} are the injection velocity and the ballistic efficiency respectively. The coefficient of B_{sat} is equal to the $(1-r_c)/(1+r_c)$, where r_c is the **reflection coefficient**. Fig. 13(a) shows the formulas to experimentally determine the ballistic efficiency, B_{sat}, and the injection velocity, V_{inj}. Fig. 13(b) is the schematic diagram of the transport theory. The carriers with the injection velocity, V_{inj}, are injected from the thermal source side, traveling to the drain side, while those which can not surmount the barrier height will be reflected to the source region. This reduces the drain current. As a consequence, we need a lower r_c or larger B_{sat} for better achieving device drain current. In other words, the larger is the value of B_{sat} , the lower the reflection is.



(a) (b)

Fig. 13 (a) The formulas used to calculate the transport parameters from the experiments, (b) The schematic showing the carrier transport. r_c is the reflection coefficient. $k_B T$ is the barrier determining the injection velocity, V_{inj} [33].

Figure 14(a) shows the I_{on}-I_{off} characteristic of uniaxial strained nMOSFET, which shows an enhancement of about 34% than the control sample. The ballistic efficiency B_{sat} under saturation operation is calculated and plotted in Fig. 14(b), in which we can see that uniaxial tensile-cap suffers less reflection near the source side. This can be explained that while the lattice is tensile-strained by the capping layer; carriers transport through the channel suffer less phonon scattering, and can pass through the channel quickly. It also shows the V_{inj} versus channel lengths, in which we see that uniaxial strained sample has higher velocity with about 2 times larger than the control sample. From the above results, uniaxial strained nMOSFET exhibits better transport behavior than that of the control sample.



(a) (b)

Fig. 14 (a) The comparison of the I_{on}-I_{off} current enhancements for nMOSFETs. Tensile-cap device shows 34% current gain over control-Si device, (b) Calculated ballistic efficiency, B_{sat}, and injection velocity, V_{inj}, where tensile-cap layer shows huge increase of V_{inj} for short channel devices.

From the past experiences in published report [33], a roadmap, Fig. 15(a), has been established for both the standard-CMOS and the strained-CMOS technologies. The strained technology shows a much better scalability than the conventional CMOS

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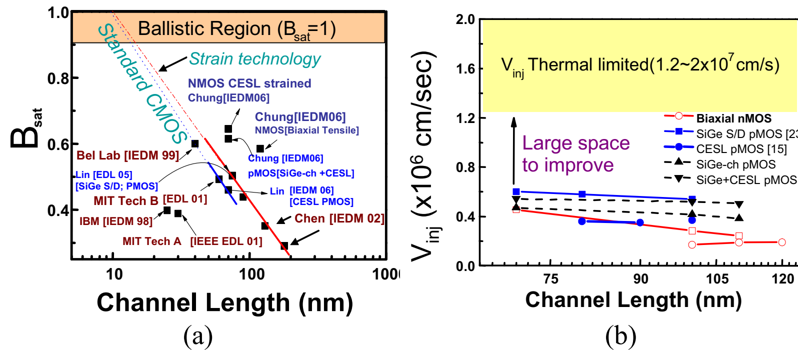
technology, i.e., at the same channel length, a much lower B_{sat} can be obtained. There are still rooms to improve V_{inj} to a higher level (Fig. 15(b)) using different mobility enhancing schemes or channel materials to achieve this goal. Moreover, a better design of strained CMOS can be understood from the characterized transport parameters.



(a) (b)

Fig. 15 A roadmap of the (a) ballistic efficiency and (b) injection velocity from reported results.

The Reliability of Strained Devices

As first reported in [14], a larger enhancement of mobility may adversely degrade the device reliability. As a consequence, it is important to understand the various strain-induced stress effect incurred by different strained techniques. To investigate the degradation effect, the tested devices have been given appropriate reliability test, in which the most typical one is the HC(hot-Carrier) stress and FN-stress, from which we measure the generated interface traps by the charge pumping technique [15].

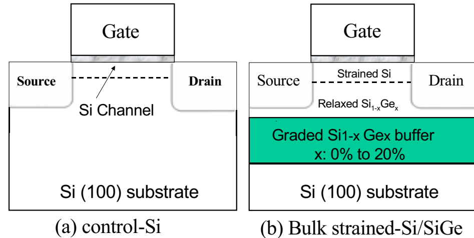


Fig. 16 (Left) The cross-sectional view of the experimental (a) bulk-Si and (b) biaxial strained-Si/SiGe devices.

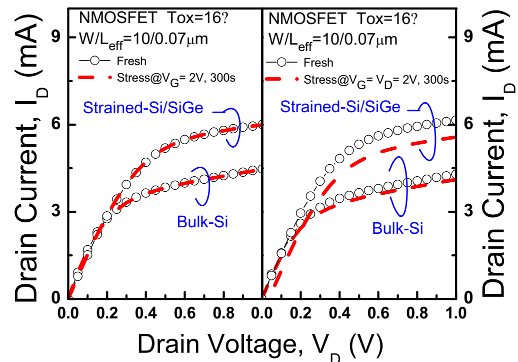
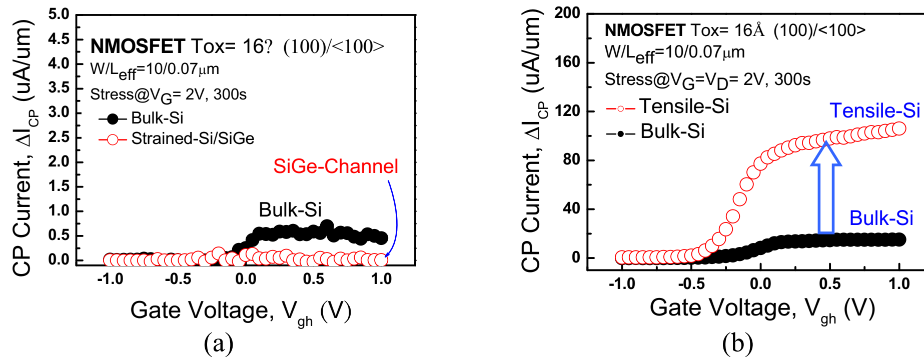


Fig. 17 (Right) The drain current degradation for devices in Fig. 16 under FN(left) and HC(right) stresses. The strained-Si/SiGe device exhibits a larger I_D degradation after HC stress.



(a) (b)

Fig. 18 (a) The comparison of the ΔIcp after FN stress. Note that the enhancement of ΔIcp is very close for strained-Si/SiGe and bulk-Si of n-MOSFET devices. (b) Comparison of the ΔIcp after HC stress for the devices in Fig. 16. Note the ΔIcp for strained-Si/SiGe is greatly enhanced comparing to FN stress in (a).

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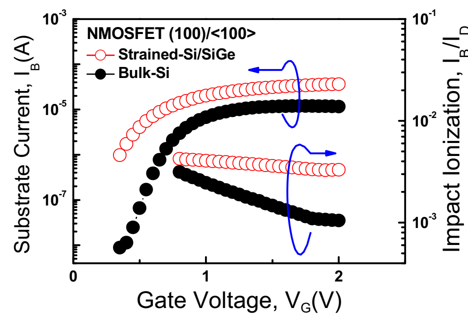

Fig. 19 The comparison of the substrate current and impact ionization rate(I_B/I_D) between strained-Si/SiGe and bulk-Si devices. I_B/I_D is greatly enhanced in biaxial strained-Si/SiGe devices.

Figure 16 shows the comparison between strained-Si/SiGe and bulk-Si nMOSFETs. Fig. 17 shows their respective I_D-V_{DS} characteristics (at the same gate bias, V_G= 2V) before and after the FN-stress (left) and HC-stress respectively. Here we see a much larger deviation of the drain current degradation, ΔI_D, for the strained-Si/SiGe device comparing to the bulk-Si ones. As reported in [14], the origin of the drain current degradation is related to the mobility enhancement. And, to further differentiate its degradation mechanisms, the vertical and lateral field effects have been evaluated by the IFCP technique [34]. Fig. 18(a) shows the measured ΔI_{CP} for studying the vertical field effect using FN stress. Since ΔI_{CP} is proportional to the generated N_{it}, we do not see a major difference. However, the comparison for bulk and strained devices under V_G= V_D HC stress as shown in Fig. 18(b), we have seen a huge difference of ΔI_{CP}, in which lateral field becomes dominant. It was found that during the FN stress, the $I_{CP,max}$ values do not show big difference, while those values for the devices after the HC stress have been increased largely comparing to the control sample ones. In other words, the huge increase of the ΔI_{CP} for the strained devices in Fig. 18(b) is caused by a large impact ionization rate (I_B/I_D) in the strained devices. This can be justified from the plots of the substrate current and impact ionization rate in Fig. 19. It shows that strained device exhibits a higher impact ionization rate. In other words, with an enhancement of the mobility in the strained devices, it will give rise to a much higher impact ionization rate and hence a much worse HC reliability. This is consistent with what we learned from the comparison shown in Fig. 18.

An extensive study has also been reported in [15] for the correlation between the strain and reliability for pMOSFET and the way on how to improve the pMOSFET NBTI reliability has been suggested for a good S/D engineering in designing a SiGe S/D pMOSFET. Different strategies for designing highly reliable CMOS devices using various strain techniques have been proposed. Several major results on the HC and NBTI reliabilities in strain engineered devices can be drawn as the following: (1) For **nMOSFETs**, tensile-stress with CESL seems to be much better in terms of reliability and performance, while SiGe strained structure has a drawback for the enhanced I_D degradation with large impact ionization rate. (2) For **pMOSFETs**, SiGe S/D structure with a special design of the raised S/D seems to be most promising in terms of performance, HC and NBTI reliability, while biaxial strained SiGe-channel has much worse NBTI and with process complexity.

The Variability Issues

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In the further scaling of CMOS devices, the variations from the process become increasingly important as a good measure of the manufacturing and yield. There are two sources of variation at the transistor level: (1) process variation which include the line-edge and line-width roughness (LER and LWR [17]), shallow trench isolation, STI [35], and variations in the gate dielectric, oxide thickness variations [36], and (2) random dopant fluctuation (RDF [37-28]), variation associated with implants and anneals [39] etc.

Table 3 Derivation of the A_{VT} in Pelgrom plot, B_{VT} in Takeuchi plot, and the standard deviation of the threshold voltage, σV_{TH}.

Derivation of Coefficients for V_{TH} standard deviation :

$$\begin{cases} V_{TH} = V_{FB} + \Phi_S + \dfrac{qN_{sub} W_{dep}}{C_{inv}} \\ \sigma V_{TH} = \dfrac{q}{C_{inv}} \sqrt{\dfrac{N_{sub} W_{dep}}{3LW}} \end{cases}$$

$$\Rightarrow \sigma V_{TH} = \frac{q}{C_{inv}} \sqrt{\frac{q(V_{TH} - V_{FB} - \Phi_S)}{3LW}} \quad \text{...(1)}$$

1. Pelgrom's coefficient, A_{VT}:

$$\sigma V_{TH} = \frac{A_{VT}}{\sqrt{LW}} \quad \text{...(2)}$$

2. Takeuchi's coefficient, B_{VT}:

$$\sigma V_{TH} = B_{VT} \sqrt{\frac{T_{inv}(V_{TH} - V_{FB} - \Phi_S)}{LW}} \quad \text{...(3)}$$

The random fluctuation can be gauged by the Pelgrom plot [16] or Takeuhi plot [40], as derived in Table 3. Historically, the Pelgrom plot is to measure the variation as a function the area, in which σV_{th} can be plotted as an inverse of $(LW)^{1/2}$, i.e.,

$$\sigma V_{th} = \frac{A_{VT}}{\sqrt{LW}}. \qquad (2)$$

Here, the slope of the curve is term as A_{VT}. The other one is proposed by Takeuchi by ruling out the contributions from the gate oxide thickness and V_{th} variations as given by

$$\sigma V_{th} = B_{VT} \sqrt{\frac{T_{inv}(V_{th} + 0.1V)}{LW}}, \qquad (3)$$

in which the slope in the expression is given by B_{VT}. A comparison of both the Pelgorm plot and the Takeuchi plot measured on the same device is shown in Fig. 20(a), where both plots keep the same straight line and the only difference is the scale of the horizontal axis. Although there is not a consensus on which plot is better, however, as long as either one is used in your study, it would be fine in expressing the consistency of your results.

For a long time, the study of dopant effect on the RDF induced V_{th} variation has been mostly studied by the simulations [17, 38, 41-42]; until more recently, an experimental approach becomes feasible [20]. One successful example is shown in Fig. 20 which demonstrated a visual observation of the dopants through a measurement of the threshold voltage and a reliable V_{th} model. Here, the first comparison is Pelgrom plot, in Fig. 20(a), in which the V_{th} variation is compared for the control n- and p-MOSFETs. The A_{VT} of nMOSFET is larger than that of pMOSFET. In Fig. 20(b), the large fluctuation in nMOSFETs is observed as a result of the boron clustering effect. Furthermore, very high dopant distributions are found near the drain side that are assumed coming from the diffusion of drain impurities.

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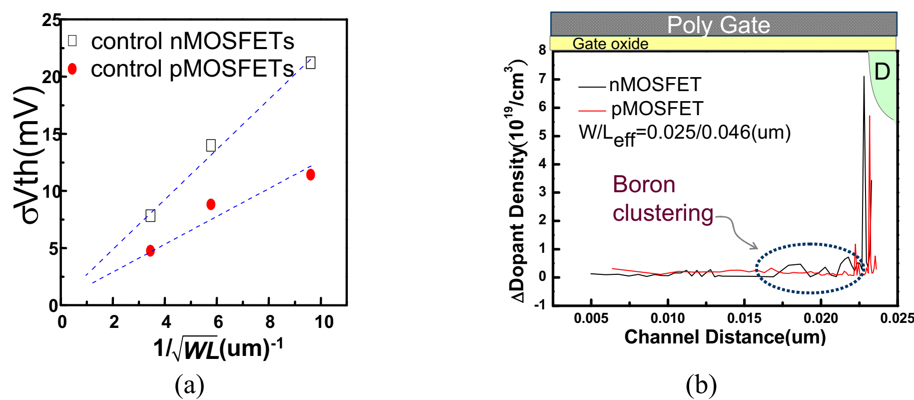

Fig. 20 (a) The comparison of the Pelgrom plots for the control n- and pMOSFETs. Note the values of nMOSFETs are larger than those of pMOSFETs. (b) The experimental results of the channel discrete dopant profiles for the control n- and p-MOSFETs. Larger fluctuation in nMOSFETs was observed.

To study the effect of **discrete dopant,** extensions of the approach to study the C or Ge out-diffusion in advanced strained devices were also demonstrated [20], which has been proved to be a powerful diagnostic tool for the monitoring of dopant variations in the strained CMOS devices.

The Perspectives on 3-D Transistor Structures

As we are looking forward in the further scaling of CMOS technology down to 20nm and beyond, there is an increasing need in finding a substitute for non-planar structures. Also, because of the depletion parasitic capacitance (C_d) of a planar CMOS and the need in a good control of the channel conduction, FinFET [43], TriGate [44], and/or nanowire [45-46], the so-called beyond CMOS devices, have evolved as a potential candidate in the near future.

Starting from the basic structure of FinFET [44], shown in Fig. 21(a), it has features of a well control of the channel which enables good control of the short channel effect, as well as a high I_{ON}. Also, one thing in common with the FinFET, Tri-Gate, and nanowire is the double-gate or Tri-gate feature which also serves as a potential candidate for future 3D transistor structure. Not only the gate controllability of a FinFET but also the lower doped channel can be used such that FinFET can achieve a better V_{th} variation. This is the biggest advantage for the device scaling. However, there are certain limitations such as the drain/source series resistance, the large gate overlap capacitance between the gate and the drain, which might degrading the device performance. For the Tri-Gate structure, there are a variety of changes in the transistor structure, such as the MuGFET(Multi-Gate FET) [47], the segmented FET [48] using the STI technique, Fig. 21(b), etc. The MuGFET equipped with a suitable strain might be able to achieve certain performance comparing to the conventional FinFET. The segmented-FET took the advantage of using STI to form a trench to isolate the fins (serving as the channel) while the device channel can keep as perfect as a pure-Si channel with good dopant variation. By doing so, the device can be configured as a MuGFET or Tri-Gate. Better performance can be achieved and with good SRAM performance provided in this specific structure.

By learning the experiences from the 90nm to 28nm CMOS in terms of the strain technologies, certain arrangements can be made by using the combination of HK/MG and

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the strain techniques in this class of devices such that higher performance, good variability, and reliability can be achieved, in which several recent reported results demonstrated a very high I_{on} >1.2mA/um and 1.1mA/um for N-FinFET and p-FinFET respectively [25, 49]. All of these efforts provide the opportunity for us to achieve a 3D transistor and IC in the near future. However, challenges are still there since we need to face the lithography problem, e.g., a highly skillful process technology to overcome the optical issue, the variability issues with fin width limitation etc. [50].

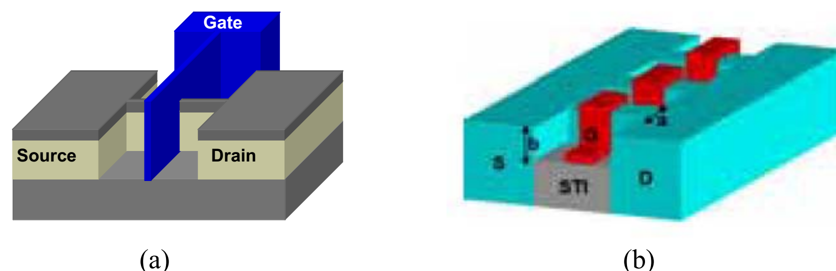

Fig. 21 (a) The FinFET structure (b) The segmented-FET structure [48].

In summary, the introducing of the strain techniques has been able to extend the Moore's law for several generations after the 90nm CMOS. It has become the most successful technique for the state-of-the-art planar CMOS technologies. Several important strain techniques have been given extensive review. The strained device can be interpreted by the ballistic carrier transport and the characterization methodology has also been demonstrated. One important issue with the reliability is that most of the strained CMOS devices face the same problem in the need of a good control of the device design in making a comparable reliability as the control ones. Also, the variability has been discussed, especially for the strained CMOS which needs further efforts to study its impact on the device characteristics. In the perspectives for the ULSI technology beyond 20nm, we are facing the challenges of further scaling in selecting appropriate transistor structure for 3D IC applications, in which the successful experiences in the strain techniques with multiple solutions might still play a major role in extending more *Moore* applications.

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