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Polycrystalline silicon thin-film transistor with nickel–titanium oxide by sol–gel spin-coating and nitrogen implantation

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ABSTRACT

This study demonstrates polycrystalline silicon thin-film transistors (poly-Si TFTs) integrated with a high-κ nickel–titanium oxide ($NiTiO_3$) gate dielectric using sol–gel spin-coating and nitrogen channel implantation. This novel fabrication method of the high-κ $NiTiO_3$ gate dielectric offers thin equivalent-oxide thickness and high gate capacitance density, favorable for increasing the current driving capability. Introducing nitrogen ions into the poly-Si using implantation effectively passivates the trap states not only in the poly-Si channel but also at the gate dielectric/poly-Si interface. The poly-Si $NiTiO_3$ TFTs with nitrogen implantation exhibit significantly improved electrical characteristics, including lower threshold voltage, a steeper subthreshold swing, higher field-effect mobility, a larger on/off current ratio, and less threshold-voltage roll-off. Furthermore, the nitrogen implantation improves the reliability of poly-Si $NiTiO_3$ TFTs against hot-carrier stress and positive bias temperature instability.

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1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted considerable attention because of their applications on peripheral driving circuits of system-on-panel (SOP) and high-performance active matrix liquid crystal displays (AM-LCDs), as well as active matrix organic light-emitting diode displays (AM-OLEDs) [1,2]. Poly-Si TFTs demonstrate numerous advantages such as higher driving current, larger field-effect mobility, and improved reliability, as compared with conventional amorphous silicon thin-film transistors (α-Si TFTs). Because a low process temperature below 600 °C is necessary to fabricate poly-Si TFTs on glass substrates of commercial flat-panel displays, the solid-phase crystallization (SPC) technique is widely adopted for phase transformation from amorphous to polycrystalline silicon at low cost [3]. However, the driving current of the SPC poly-Si TFTs with conventional thick SiO_2 gate dielectrics is limited. Although the thickness scaling of SiO_2 boosts the driving current, it also unavoidably increases gate leakage current [4]. High-κ gate dielectrics can increase gate capacitance while maintaining sufficient physical thickness. Therefore, the poly-Si TFTs with high-κ gate dielectrics not only increase the driving current but also suppress the gate leakage current simultaneously.

Several techniques, including atomic layer deposition (ALD), physical vapor deposition (PVD), and chemical vapor deposition (CVD), have been developed to deposit high-κ gate dielectrics. Another simple fabrication method, sol–gel spin-coating, has also been used to form high-κ gate dielectrics, charge trapping layers of memory devices and active channel layers of oxide-based transistors [5–7]. The sol–gel spin-coating method is attractive because of its inexpensive precursors and simple facilities requiring no high vacuum. Additionally, the low process temperature of the sol–gel spin-coating method is compatible with the fabrication on glass substrates. Several high-κ materials, including Al_2O_3 and Ta_2O_5, have been proposed to replace conventional SiO_2 in poly-Si TFTs [8,9]. However, the device performance was compromised by the lower dielectric constant of Al_2O_3 ($\kappa < 9$) and the narrow bandgap of Ta_2O_5. By contrast, $NiTiO_3$ fabricated using sputter methods was shown to have high dielectric constant, low leakage current and excellent reliability [10]. Furthermore, $NiTiO_3$ prepared by sol–gel spin-coating was proposed to be the high-κ gate dielectric of poly-Si TFTs [11].

The poly-Si TFTs with high-κ gate dielectrics is known to suffer from undesirable off-state leakage current because of field-enhanced emission through grain-boundary trap states [12]. Several methods have been proposed to reduce the grain-boundary trap states. The hydrogen-based plasma treatment technique has been most widely used [13]. However, the hydrogenated poly-Si TFTs is subjected to long-term device instability under electrical stress

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because of the weak Si–H bonds [14,15]. Nitrogen channel implantation has also been proposed to passivate the trap states at the grain boundaries [16,17]. Additionally, robust Si–N bonds significantly improve the device reliability.

This paper reports a high-performance and highly reliable n-channel poly-Si TFT with a sol–gel spin-coating $NiTiO_3$ gate dielectric and nitrogen channel implantation. This study demonstrated a gate capacitance density of 410 nF/cm^2, threshold voltage (V_{TH}) of 1.1 V, subthreshold slope (S.S.) of 200 mV/dec, field-effect mobility (μ_{FE}) of 51 cm^2/V-s, on/off current ratio (I_{on}/I_{off}) over seven orders of magnitude, and robust reliability against hot carrier stress and positive bias temperature instability (PBTI). The proposed poly-Si TFT achieves excellent characteristics using only the conventional SPC, and is thus cost-effective and compatible to present flat-panel display manufacturing.

2. Experimental procedures

Fig. 1 illustrates the fabrication steps for the proposed poly-Si TFTs with the $NiTiO_3$ dielectric and nitrogen ion implantation. First, a 50-nm undoped amorphous silicon (α-Si) layer was deposited on 550-nm SiO_2 by low-pressure chemical vapor deposition (LPCVD) at 550 °C. The nitrogen ions were implanted with a projected range at the middle of the α-Si film and a dosage of 5×10^{13} cm^{-2} [Fig. 1a]. The SPC and dopant activation of nitrogen ions were performed at 600 °C for 24 h in N_2 ambient. After patterning the active region by conventional lithography and dry etching, phosphorous ion implantation was performed at 20 keV with a dose of 5×10^{15} cm^{-2} at the source/drain regions [Fig. 1b], followed by dopant activation annealing at 600 °C for 12 h. After the RCA clean process, a 3-nm SiO_2 layer was deposited on the poly-Si channel to improve the interface with the $NiTiO_3$ gate dielectric by LPCVD using diluted tetraethyl orthosilicate (TEOS) of 10 sccm as the precursor at 30 m torr. The $NiTiO_3$ film was deposited on the SiO_2 layer using sol–gel spin-coating at 3000 rpm (rpm) for 30 s and then baked at 200 °C for 10 min to remove the solvent. The sol–gel solution was synthesized by dissolving nickel acetate tetrahydrate [$Ni(OOCCH_3)_2 \cdot 4H_2O$] and titanium isopropoxide $Ti\{OCH(CH_3)_2\}_4$ in 2-methoxyethanol. The $NiTiO_3$ spin-coating processes were repeated three times to obtain a film thickness of approximately 50 nm. The sample was then subjected to a two-step thermal treatment to improve the $NiTiO_3$ quality, first at 400 °C in O_2 ambient for 20 min followed by additional rapid thermal annealing (RTA) at 500 °C in N_2 ambient for 30 s. The TaN gate electrode with a thickness of 100 nm was defined using a lift-off process to prevent the plasma damage and over-etching using traditional dry etching [Fig. 1c]. After depositing a 300-nm SiO_2 passivation layer using plasma-enhanced chemical vapor deposition at 300 °C, the contact holes were opened using a two-step wet etching process. A buffered oxide etch (BOE) solution and a HF:H_2O = 50:1 were used to etch SiO_2 and $NiTiO_3$, respectively. Finally, a 400-nm Al film was deposited and patterned as metal pads [Fig. 1d]. No additional hydrogen plasma treatment or thermal sintering was performed after the Al pad patterning. For comparison, control poly-Si $NiTiO_3$ TFTs without nitrogen implantation were also prepared using the same process flow.

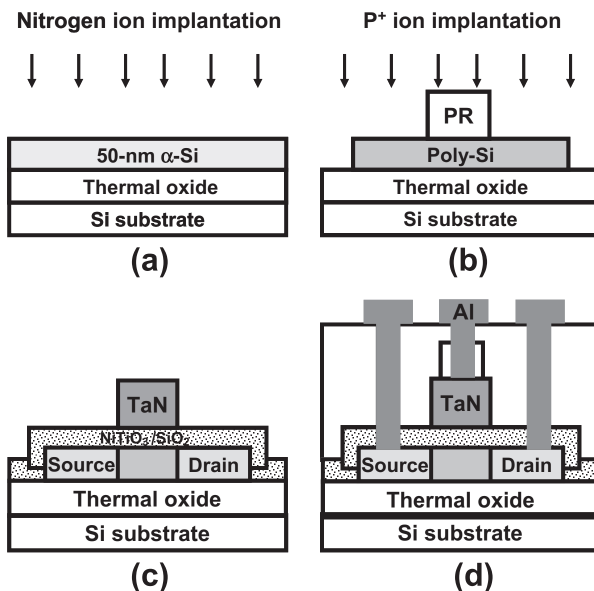


Fig. 1. Schematic diagrams of the process steps for the poly-Si $NiTiO_3$ TFT with nitrogen channel implantation.

3. Results and discussion

3.1. Material analyses

Fig. 2 presents the grazing incident X-ray diffraction (GI-XRD) spectra of the $NiTiO_3$ films annealed at various RTA temperatures. The samples remained amorphous at 500 °C and 600 °C, but crystallized at 700 °C with preferred orientations at (104), (111), (113), (116), (214), and (300). Fig. 3a–c illustrates the atomic force microscopy (AFM) images of $NiTiO_3$ films annealed at 500 °C, 600 °C, and 700 °C. The root-mean-square (rms) values of the surface roughness in the films annealed at 500 °C, 600 °C, and 700 °C were 0.348 nm, 0.671 nm, and 2.501 nm, respectively. The polycrystalline $NiTiO_3$ shows rough surface morphology that may cause high leakage current [11] and adhesion problems with the TaN metal gate. Therefore, the RTA temperature of 500 °C was chosen to fabricate our TFT devices.

The chemical composition of the $NiTiO_3$ gate dielectric was determined using X-ray photoelectron spectroscopy (XPS), as shown in Fig. 4. The oxygen 1s spectrum included two different metal–oxygen bonds, Ni–O and Ti–O, with binding energy near 530.5 eV. After background removal using the Shirley method, the atomic ratio of Ni:Ti:O was estimated at 1:1:3 by integrating the intensity from 854 eV to 880 eV for the nickel 2p spectrum, from 453 to 468 eV for the titanium 2p spectrum, and from 526 to 535 eV for the oxygen 1s spectrum.

3.2. Gate dielectric integrity of $NiTiO_3$

Fig. 5 shows the cross-sectional transmission electron microscopy (TEM) micrograph of the proposed poly-Si TFT with the Ni-

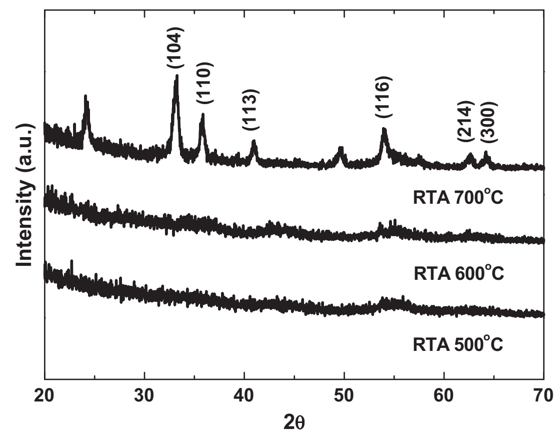


Fig. 2. GI-XRD spectra of spin-coating $NiTiO_3$ films annealed at various RTA temperatures.

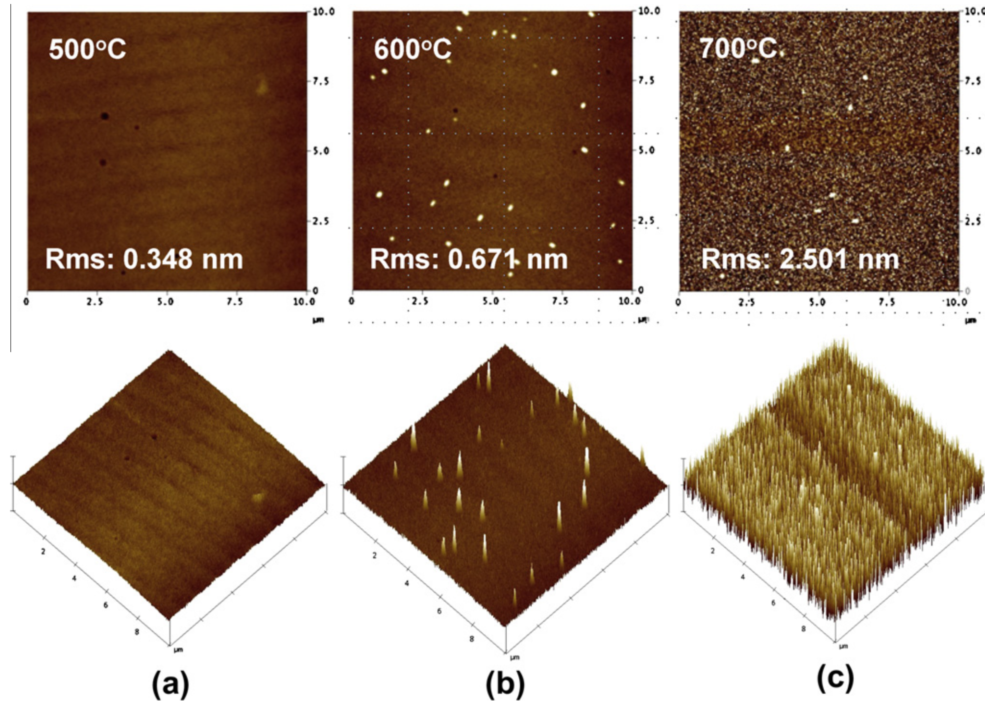


Fig. 3. AFM images of $NiTiO_3$ films annealed at (a) 500 °C, (b) 600 °C, and (c) 700 °C. The corresponding RMS values of the surface roughness are 0.348 nm, 0.671 nm, and 2.501 nm, respectively.

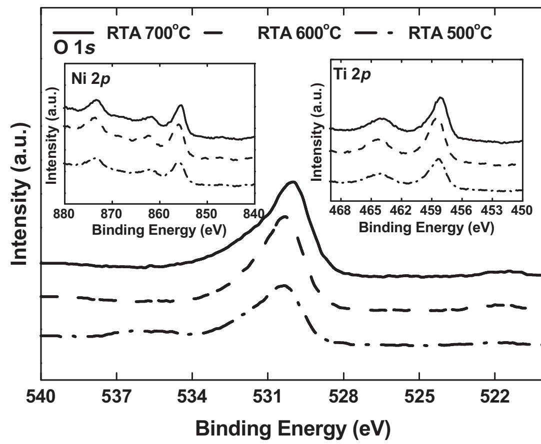


Fig. 4. XPS spectra of the Ni 2p, Ti 2p, and O 1S core levels for the $NiTiO_3$ gate dielectric.

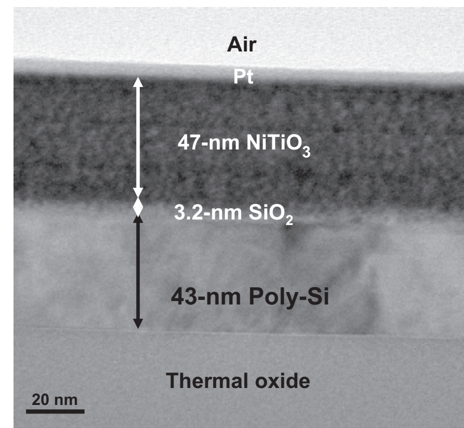


Fig. 5. Cross-sectional TEM micrograph of the proposed poly-Si $NiTiO_3$ TFT. The top Pt capping layer was deposited for the purpose of TEM imaging only.

TiO_3 gate dielectric. The physical thicknesses of the $NiTiO_3$ gate dielectric and the poly-Si channel were approximately 47 nm and 43 nm, respectively, with a 3.2-nm SiO_2 interfacial layer in between. Fig. 6 shows a typical capacitance–voltage (*C*–*V*) characteristic at 1 MHz with an 8.4-nm equivalent-oxide thickness (EOT) extracted from the accumulation gate capacitance of 410 nF/cm^2. The *C*–*V* was measured from a $NiTiO_3$ metal–oxide–semiconductor (MOS) capacitor fabricated on the Si wafers using the identical $NiTiO_3$ deposition process. The dielectric constant of $NiTiO_3$ was estimated at 35, comparable to that in the sputtered $NiTiO_3$ [10], using the following equation:

$$EOT = T_{SiO_2} + (\kappa_{SiO_2}/\kappa_{NiTiO_3}) \times T_{NiTiO_3} \quad (1)$$

where κ_{NiTiO3} and κ_{SiO2} are the dielectric constants of $NiTiO_3$ and SiO_2, respectively, and T_{NiTiO3} and T_{SiO2} are the physical thicknesses of these two films. Furthermore, the inset in Fig. 6 shows the gate current density versus the electric field (*J*–*E*) characteristic of the $NiTiO_3$ gate dielectric. The *J*–*E* characteristic was measured by applying gate voltage and grounding the source and drain of the TFT device. The breakdown field E_{bd} of 3 MV/cm was close to other high-κ dielectrics with similar dielectric constant using the empirical relation [18] as follows:

$$E_{bd} = 35 \times \kappa^{-0.64} \quad (2)$$

The high gate capacitance density and dielectric breakdown field suggest that the $NiTiO_3$ is a promising high-κ gate-dielectric to replace SiO_2 in poly-Si TFTs.

3.3. Device characteristics

Fig. 7a illustrates the transfer characteristics (I_{DS}–V_{GS}) of the poly-Si $NiTiO_3$ TFTs with and without nitrogen implantation at V_{DS} = 0.1 V and 1 V. The channel width (*W*) and channel length

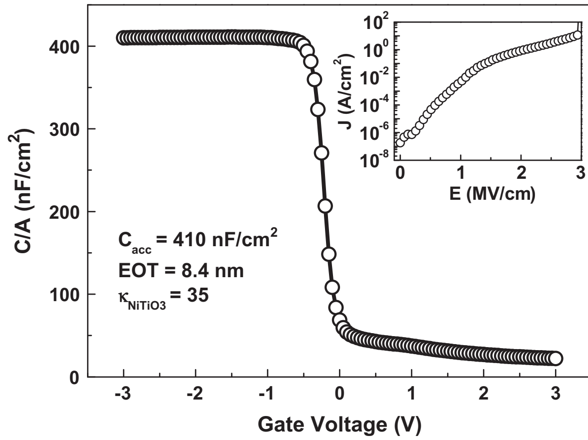


Fig. 6. *C–V* curve of the $NiTiO_3$ MOS capacitor. Inset is the gate current density versus the electric field (*J–E*) characteristic of the poly-Si $NiTiO_3$ TFT. The electric field is defined by the applied voltage divided by the physical film thickness.

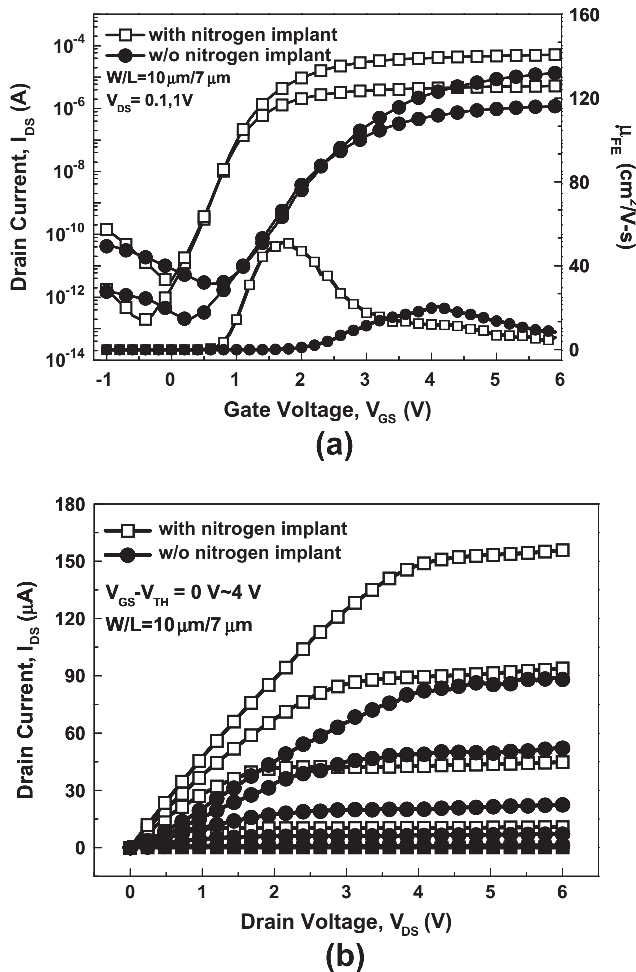


Fig. 7. (a) Transfer characteristics and (b) output characteristics of the poly-Si $NiTiO_3$ TFTs with and without nitrogen channel implantation.

(L) were 10 μm and 7 μm, respectively. The V_{TH}, S.S., and μ_{FE} were extracted at V_{DS} = 0.1 V. The V_{TH} was defined as the gate voltage with a normalized drain current of $(W/L) \times 100$ nA. The I_{on}/I_{off} was defined as the ratio of the maximum on-state current to the minimum off-state leakage current at V_{DS} = 1 V. The V_{TH}, S.S., and I_{on}/I_{off} were 3 V, 353 mV/dec, and 5.2×10^6 for the device without implantation; and 1.1 V, 200 mV/dec, and 1.6×10^7 for the device with implantation. The electrical characteristics of the poly-Si $NiTiO_3$ TFTs with nitrogen implantation were significantly improved, as compared with those without nitrogen implantation. Additionally, the maximum field-effect electron mobilities of the poly-Si $NiTiO_3$ TFTs with and without nitrogen implantation were 51 and 21 cm^2/V s, respectively, as shown in Fig. 7a. The output characteristics (I_{DS}–V_{DS}) of poly-Si $NiTiO_3$ TFTs with and without nitrogen implantation are shown in Fig. 7b. The driving current of the poly-Si $NiTiO_3$ TFT using nitrogen implantation shows 80% improvement, as compared with that without implantation at V_{GS}–V_{TH} = 4 V because of the superior electron mobility. Table 1 summarizes the critical TFT device parameters obtained in this study.

Interface trap states and grain boundary traps have been reported to dominate the electrical characteristics of poly-Si TFTs, where the deep trap states at grain boundaries mainly affected V_{TH}, and the deep interface trap states degraded S.S. [19,20]. Previous analysis of secondary ion mass spectrometry (SIMS) on TFTs with channel nitrogen implantation revealed that substantial nitrogen piled up at the interface of gate dielectric and poly-Si channel and also diffused deeply into the bulk poly-Si film [16]. The significant improvement on the TFT characteristics has been attributed to the nitrogen passivation effect on the interface states of the gate dielectric/poly-Si channel interface and the Si dangling bonds at the grain boundaries of the poly-Si channel. The formation of Si–N bonds has been postulated to be responsible for the effective passivation [16,17,21]. Although difference in grain size may also explain the improved TFT characteristics, we presume that the grain size was not significantly altered by the nitrogen channel implantation because the projected range of implantation at the middle of the α-Si film is difficult to interfere with the nucleation process at the α-Si/bottom SiO_2 interface [22].

3.4. Trap-state density

The effective grain-boundary trap state density (N_{trap}) was calculated using the grain-boundary trapping model proposed by Levinson and Proano [23,24]. Fig. 8 exhibits the $\ln[(I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ at V_{DS} = 0.1 V and high gate voltage for the poly-Si $NiTiO_3$ TFTs with and without nitrogen ion implantation, where V_{FB} is the flatband voltage. N_{trap} can be calculated from the square root of the slope in Fig. 8. The N_{trap} in the devices with and without nitrogen ion implantation were 3.8×10^{12} cm^{-2} and 1.26×10^{13} cm^{-2}, respectively. This result indicates that the nitrogen incorporation can effectively passivate the trap states in the grain boundaries, in excellent agreement with the improved device performance.

3.5. Short-channel effect

The V_{TH} as a function of channel length is shown in Fig. 9. The channel width was fixed at 10 μm. Noticeable V_{TH} roll-off was observed in the poly-Si TFTs without nitrogen implantation, but not in those with nitrogen implantation. In the undoped poly-Si TFT, V_{TH} was governed by the grain boundary traps. The V_{TH} roll-off in

Table 1
Extracted device parameters for the poly-Si $NiTiO_3$ TFTs with and without nitrogen implantation.

Poly-Si $NiTiO_3$ TFT	V_{TH} (V)	S.S. (mV/dec.)	μ_{FE} (cm^2/V-s)	I_{on}/I_{off} ratio
With nitrogen	1.1	200	51	1.6×10^7
W/O nitrogen	3	353	21	5.2×10^6

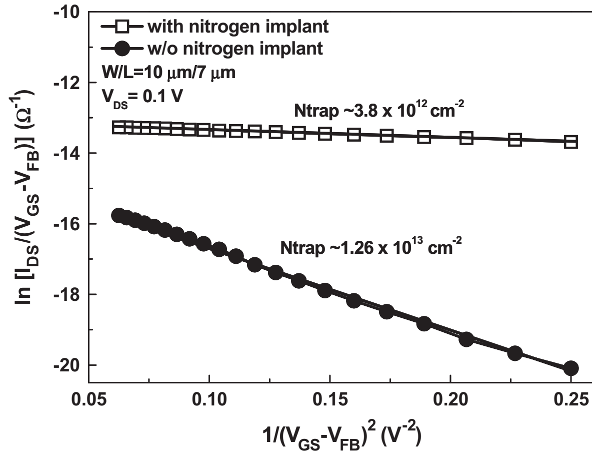
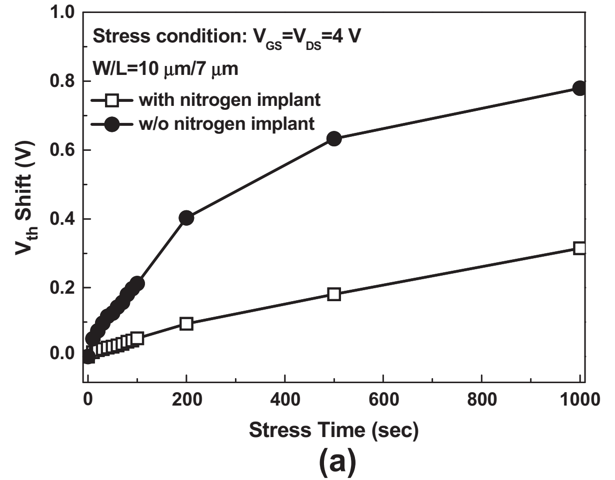


Fig. 8. Effective trap state densities of the poly-Si $NiTiO_3$ TFTs with and without nitrogen channel implantation.



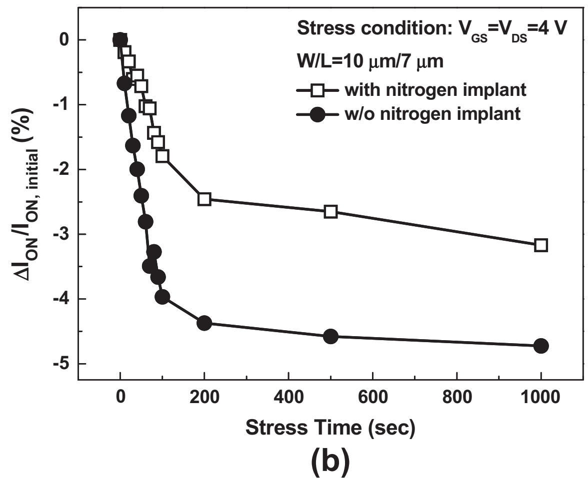


Fig. 10. (a) Threshold-voltage shift and (b) on-current degradation versus hot-carrier stress time for the poly-Si $NiTiO_3$ TFTs with and without nitrogen channel implantation.

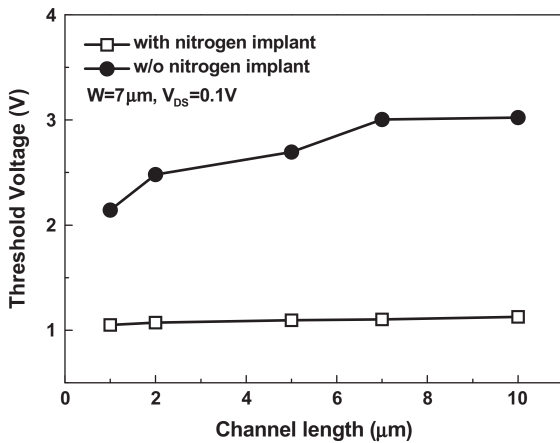


Fig. 9. Threshold-voltage roll-off characteristics of the poly-Si $NiTiO_3$ TFTs with and without nitrogen channel implantation.

the scaled poly-Si TFTs was attributed to the reduced number of grain boundaries in the poly-Si channel and less grain-boundary trap states [25,26]. In the nitrogen-implanted poly-Si TFT, V_{TH} was less susceptible to the poly-Si grain boundary because of the nitrogen passivation effect, as evidenced by the much lower V_{TH}. Therefore, the V_{TH} roll-off became less significant even the grain size was presumed to be comparable to that in the undoped channel.

3.6. Device reliability

Hot-carrier stress at room temperature under $V_{GS} = 4$ V and $V_{DS} = 4$ V was performed to investigate the reliability of the poly-Si $NiTiO_3$ TFTs with and without nitrogen implantation. The accelerated stress condition allowed TFT on-current higher than that required for the use condition of AM-OLED applications [27]. Fig. 10a and b shows the V_{TH} shift (ΔV_{TH}) and on-current degradation (ΔI_{on}) as a function of the hot-carrier stress time. The ΔV_{TH} and ΔI_{on} were defined as $V_{TH,\ stressed}-V_{TH,\ initial}$ and $(I_{on,\ stressed}-I_{on,\ initial})/I_{on,\ initial} \times 100\%$, respectively, where initial and stressed indicated the extracted values before and after stress. The poly-Si $NiTiO_3$ TFTs with nitrogen implantation show smaller ΔV_{TH} (0.31 V versus 0.78 V) and ΔI_{on} (3.2% versus 4.7%) as compared with the control sample after 1000 s stress. Note that ΔI_{on}

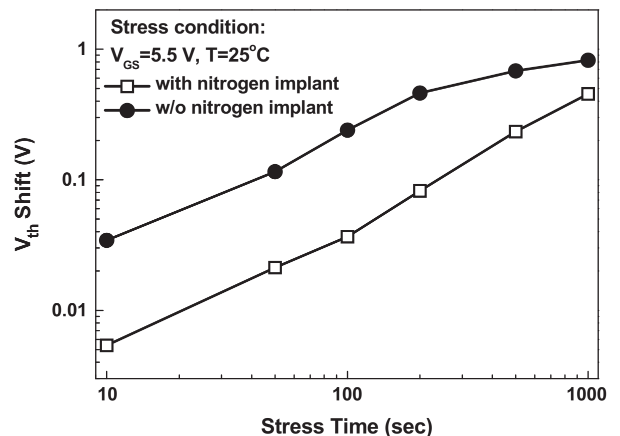


Fig. 11. Threshold-voltage shift versus PBTI stress time for the poly-Si $NiTiO_3$ TFTs with and without nitrogen channel implantation.

in an industrial standard α-Si TFT for AM-LCD backplanes was reported to be 5% after 1 h DC stress [27]. The device degradation due to the hot-carrier stress may be attributed to the following two reasons: the interface state generation at the gate dielectric/

poly-Si interface and the formation of Si dangling bonds by breaking weak Si–H bonds with a bond energy of 70 kcal/mol [29] in the poly-Si channel [15]. The improvement on the immunity against hot-carrier stress using nitrogen implantation correlated with the larger bond energy of 106 kcal/mol [28] of Si–N bonds [16,17]. Further research is necessary to confirm the formation of the robust Si–N bonds in place of the weak Si–H bonds.

Positive bias temperature instability (PBTI) is another critical reliability concern for n-channel TFT devices with high-κ gate dielectrics. V_{GS} = 5.5 V was applied to study the PBTI of the poly-Si $NiTiO_3$ TFTs at 25 °C, as shown in Fig. 11. The electrons accelerated by the applied positive gate voltage may break the weak bonds at the grain boundaries of the poly-Si channel and the gate dielectric/poly-Si interface to generate the trap states, resulting in significant ΔV_{TH} during the PBTI stress [30]. Therefore, the poly-Si $NiTiO_3$ TFTs with nitrogen implantation exhibited superior immunity against PBTI because of the nitrogen passivation effect.

4. Conclusion

This study is the first to demonstrate high-performance poly-Si TFTs, utilizing nitrogen channel implantation and a spin-coating $NiTiO_3$ gate dielectric. High gate capacitance density of 410 nF/cm^2 was achieved using a 47-nm $NiTiO_3$ gate dielectric with a dielectric constant of 35 and a TaN metal gate. Additionally, nitrogen channel implantation improved the threshold voltage, subthreshold swing, field-effect mobility, and on/off current ratio because of the passivation of trap states in the poly-Si film and at the gate dielectric/poly-Si interface. Nitrogen channel implantation also improves the immunity against hot-carrier stress and positive bias temperature instability. Therefore, the proposed poly-Si TFTs requiring no expensive phase crystallization techniques is a highly promising candidate for system-on-panel applications and high-speed active-matrix addressing.

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