High-Performance Polycrystalline-Silicon Nanowire Thin-Film Transistors With Location-Controlled Grain Boundary via Excimer Laser Crystallization

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***Abstract*—High-performance polycrystalline-silicon (poly-Si) nanowire (NW) thin-film transistors (TFTs) are demonstrated using excimer laser crystallization to control the locations of grain boundaries two-dimensionally. Via the locally increased thickness of the amorphous-silicon (a-Si) film as the seeds, the cross-shaped grain boundary structures were produced among these thicker a-Si grids. The NW TFTs with one primary grain boundary perpendicular to the channel direction could be therefore fabricated to achieve an excellent field-effect mobility of 346 $cm^2/V \cdot s$ and an on/off current ratio of 3×10^9. Furthermore, the grain-boundary-location-controlled NW TFTs also exhibited better reliability due to the control of grain boundary locations. This technology is thus promising for applications of low-temperature poly-Si TFTs in system-on-panel and 3-D integrated circuits.**

***Index Terms*—Excimer laser crystallization (ELC), location controlled, nanowire (NW), polycrystalline silicon (poly-Si).**

I. Introduction

LOW-TEMPERATURE polycrystalline-silicon (poly-Si) thin-film transistors (TFTs) have attracted considerable attention for the applications in active-matrix flat-panel displays and 3-D integrated circuits (3-D ICs) [1]–[3]. Several technologies and device structures have been proposed to improve the device performance. The poly-Si nanowire (NW) TFTs have been fabricated to enhance gate controllability, and the short-channel effects and subthreshold leakage current can be suppressed owing to their high surface-to-volume ratio [4], [5]. Most of them used solid-phase crystallization (SPC) and thus induced the numerous grain boundaries as well as intragrain defects, resulting in poor performance [6]–[8]. Excimer laser crystallization (ELC) of amorphous silicon (a-Si) has been proven to be a promising method to produce high-quality silicon grains and led to better device performance. Therefore, the modified ELC technologies such as sequential lateral solidification (SLS) for controlling the location of grain boundary have been adopted on the fabrication of NW-based poly-Si TFTs [9], [10]. However, the NW TFTs fabricated with SLS exhibited large variations of device characteristics due to the randomly distributed grain boundaries along the channel direction since the SLS process controlled the location of the grain in only one dimension by lateral solidification.

In this letter, a method to enable the 2-D location control of the grain boundaries has been proposed. Consequently, grain-boundary-location-controlled (GBLC) NW TFTs with one primary grain boundary perpendicular to the channel direction could be artificially designed and fabricated to exhibit much excellent device performance.

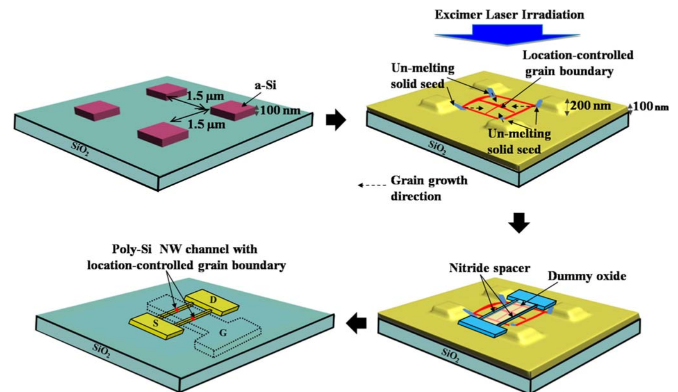

Fig. 1. Schematic diagram of the key fabrication processes for the GBLC NW TFTs: a-Si island formation, a-Si deposition and ELC process, dummy oxide and nitride spacer formation, and NW channel and gate electrode formation.

II. Device Fabrication

Fig. 1 shows the schematic diagram of the key processes for the fabrication of poly-Si NW TFTs with the proposed crystallization method. First, a 1000-Å-thick a-Si thin film was deposited using a low-pressure chemical vapor deposition (LPCVD) system at 550 °C on an oxidized silicon substrate. Then, the a-Si layer was patterned as the grid structures of 1.5-μm-sized square islands by reactive ion etching (RIE) with an interspacing of 1.5 μm between the adjacent islands. Next, another a-Si thin film with a thickness of 1000 Å was deposited by LPCVD at 550 °C. Laser crystallization was performed using KrF excimer laser ($\lambda = 248$ nm) in a vacuum chamber pumped down to 10^{-3} torr. The laser energy density was controlled at 540 mJ/cm^2, and the number of laser shots per area was 20 shots. After ELC, a tetraethyl orthosilicate (TEOS) oxide with a thickness of 2000 Å was deposited by LPCVD and patterned as the dummy strips with 2000-Å step profile by RIE, followed by a 1800-Å-thick nitride deposition using LPCVD.

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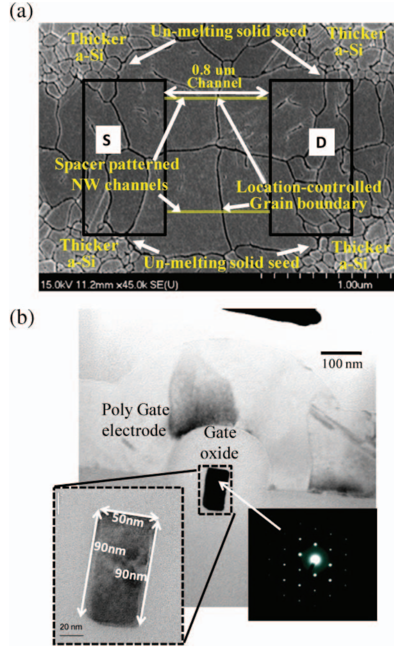

Fig. 2. (a) Plan view of Secco-etched SEM image of the grain structure via the proposed crystallization method. (b) Cross-sectional TEM image of the GBLC NW TFT via the proposed crystallization method. The insets of (b) show the enlarged views of the NW channel and electron diffraction pattern for the grains in the channel.

Subsequently, source and drain (S/D) pads were defined by photoresist, and then, anisotropic etching was carried out to form the nitride hard mask for the active region formation of NW channels. Next, the dummy oxide strips were removed by buffered oxide etch. Then, the S/D pads and ELC poly-Si NWs were formed by the nitride spacer layer via anisotropic etching of the poly-Si layer. Subsequently, the nitride was etched away using hot H_3PO_4 at 165 °C. After nitride removal, a 1000-Å-thick TEOS gate oxide and a 2000-Å-thick *in situ* phosphorus-doped poly-Si were deposited using LPCVD, and then, the poly-Si and gate oxide layers were etched to form the gate structure (G). With the location-controlled grain boundary structure, the channel region of the poly-Si NW TFTs could be placed to be with one primary grain boundary perpendicular to the channel direction, as shown in Fig. 1. After gate patterning, self-aligned phosphorus S/D ion implantation (5×10^{15} cm^{-2} and 40 keV) was conducted. Next, a passivation TEOS oxide layer was deposited using plasma-enhanced chemical vapor deposition, and the implanted dopants were activated by thermal annealing at 600 °C for 9 h in nitrogen ambient. Finally, contact hole opening and metallization were completed to fabricate the GBLC NW TFTs. For comparison, NW TFTs using conventional ELC (conv-ELC) with the super lateral growth laser irradiation condition [11] and NW TFTs using SPC at 600 °C for 12 h [12] were also fabricated as the reference samples.

III. Results and Discussion

Fig. 2(a) shows the SEM image of ELC poly-Si thin film of the proposed crystallization method with a laser energy density of 540 mJ/cm^2 after Secco etching. The thickness of the thicker a-Si grids is 2000 Å, and that of the other thinner a-Si region is 1000 Å. As the laser energy density is properly controlled at 500–560 mJ/cm^2, the thinner a-Si region completely melts, and the thicker a-Si region only partially melts; thus, a significantly thermal gradient occurs to induce the super lateral grain growth starting from the unmelted seeds of the thicker a-Si grids toward the completely melting thinner a-Si regions. Owing to the temperature gradient created not only along the x-axis but also along the y-axis direction, the 2-D grain growth with an expanded angle toward the completely melting regions is formed until the solid–melt interface impinges. As a result, a cross-shaped grain boundary structure forms in the center among these thicker a-Si grids. Therefore, the channel region of the NW TFTs can be placed with one primary grain boundary perpendicular to the channel direction, as shown in Fig. 2(a). Fig. 2(b) shows the cross-sectional TEM image of the GBLC NW TFTs. As shown in the inset of Fig. 2(b), the peripheries of each channel are about 90, 50, and 90 nm, correspondingly. In addition, the single-crystalline cross-sectional view is observed for the NW channel, and the corresponding grain structure is analyzed by its electron diffraction pattern to be [1 1 0] oriented.

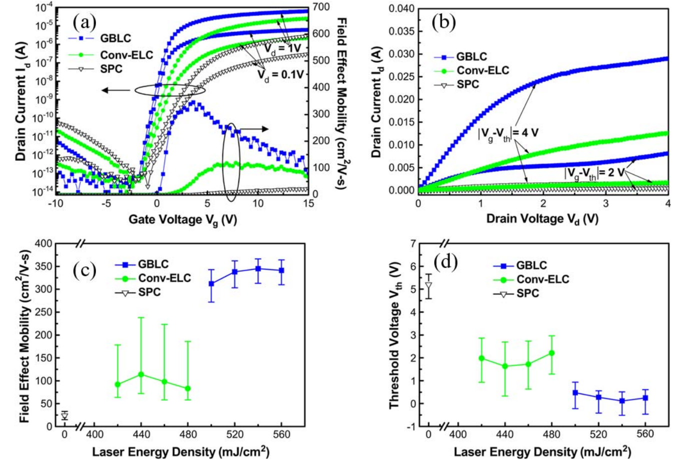

Fig. 3. (a) Transfer and (b) output characteristics of the GBLC, conv-ELC, and SPC NW TFTs. The dependences of (c) $\mu_{\rm FE}$ and (d) $V_{\rm th}$ on laser energy densities for the GBLC, conv-ELC, and SPC NW TFTs.

Typical transfer and output characteristics of the GBLC, conv-ELC, and SPC NW TFTs are compared in Fig. 3(a) and (b), respectively. These devices have a channel length (L) of 0.8 μm and a channel width (W) of 0.46 μm (0.23 μm $\times$ 2 NWs), where the channel width is defined by the cross-sectional TEM image of the NW channel, as shown in Fig. 2(b). The threshold voltage ($V_{\rm th}$) is defined according to the normalized drain current of $I_d = (L/W) \times 10^{-8}$ at $V_d = 0.1$ V. The field-effect mobility ($\mu_{\rm FE}$) is extracted from the linear region at $V_d = 0.1$ V, and the on/off current ratio is defined at $V_d = 1$ V. As compared with conv-ELC and SPC NW TFTs, the GBLC NW TFTs exhibit the smallest $V_{\rm th}$ of 0.35 V, the highest $\mu_{\rm FE}$ of 346 cm^2/V $\cdot$ s, and the largest on/off current ratio of 3×10^9. In contrast, the conv-ELC NW TFTs show $V_{\rm th}$ of 1.9 V, $\mu_{\rm FE}$ of 119 cm^2/V $\cdot$ s, and an on/off current ratio of 8.5×10^8, which are 4.9 V, 23 cm^2/V $\cdot$ s, and 5.7×10^7 for the SPC NW ones, accordingly. Owing to the location-controlled grain boundaries, the channels of the GBLC NW TFTs will contain fewer boundary potential barriers that obstruct the carrier transportation,

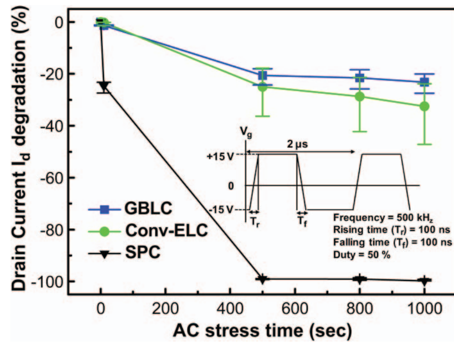

Fig. 4. Comparison of the ratio of on-current degradation for the GBLC, conv-ELC, and SPC NW TFTs during the ac stress.

leading to its better electrical characteristics. Moreover, the dependence of device performance on laser energy densities for the GBLC NW TFTs is investigated and compared with the conv-ELC and SPC ones. Thirty devices were measured for each laser irradiation condition to evaluate the device-to-device uniformity. The dependences of μ_{FE} and V_{th} on laser energy densities for these TFTs are shown in Fig. 3(c) and (d), respectively. The GBLC NW TFTs exhibit a relatively smaller spread of μ_{FE} and V_{th} and are less sensitive for different laser energy densities as compared to the conv-ELC ones. It is well known that the randomly distributed grain boundaries are strongly degrading the device uniformity. As a result, the superior device uniformity can be achieved for the GBLC NW TFTs owing to the location-controlled grain boundaries. On the other hand, the SPC ones show small μ_{FE} and large V_{th} in spite of the small variation of device performance.

To investigate the electrical reliability under the ac operation, the three types of NW TFTs mentioned previously were subjected to the dynamic bias stress test, with ten devices stressed for each type. The stress pulses were applied on the gate electrode, and S/D were grounded, as shown in the inset of Fig. 4. Fig. 4 shows the comparison of the evolution of the ratio of on-current degradation at $V_g - V_{\mathrm{th}} = 10$ V from its initial value for these three types of NW TFTs during the stress. After 1000-s stress, the GBLC TFTs exhibit the smallest on-current degradation of 23% compared to 32.5% and 99.7% of the conv-ELC and SPC ones, respectively. Since defect states frequently exist at the grain boundaries, the GBLC NW TFTs possess superior crystallinity of poly-Si thin film and thus achieve better electrical stability.

IV. Conclusion

The high-performance poly-Si NW TFTs have been successfully fabricated via a 2-D GBLC method. The GBLC NW TFTs could achieve a field-effect mobility of 346 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ which is higher than 119 and 23 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ for the conv-ELC and SPC ones, correspondingly. Furthermore, the GBLC NW TFTs exhibited superior electrical reliability under the dynamic stress. This work reveals that the proposed GBLC NW TFTs are promising for the future system-on-panel and 3-D IC applications.

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