

Low-Operating-Voltage Ultrathin Junctionless Poly-Si Thin-Film Transistor Technology for RF Applications

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Abstract—In this letter, for the first time, we experimentally investigate the radio-frequency (RF) characteristics and low-frequency noise (LFN) of n-type planar junctionless (JL) poly-Si thin-film transistors (TFTs). The fabricated JL devices show remarkable dc performance with good current drive and a high on-current/off-current ratio of 8×10^7 . Furthermore, with the implementation of an *in situ* phosphorus-doped channel architecture and a salicide process, the JL device with a channel length of $0.4 \mu\text{m}$ exhibits a cutoff frequency (f_t) of 3.36 GHz and a maximum oscillation frequency (f_{max}) around 7.37 GHz at a drain bias of 2 V. As far as LFN is concerned, the JL device shows approximately four orders of magnitude lower drain-current noise power spectral density (S_{id}) over conventional inversion-mode counterparts. These results demonstrate that the JL poly-Si TFT technique is promising for RF modules implemented in system-on-panel applications.

Index Terms—Junctionless (JL), low-frequency noise (LFN), poly-Si, radio frequency (RF), thin-film transistor (TFT).

I. INTRODUCTION

NONPLANAR multigated transistors such as FinFETs and planar ultrathin-body (UTB) silicon-on-insulator (SOI) transistors are considered as promising candidates for next-generation CMOS applications because of their excellent immunity to short-channel effects [1], [2]. Lately, the concept of junctionless (JL) transistor has been proposed to circumvent problems encountered in the junction formation and to boost the device performance [3], [4]. The reported JL devices with their channels of the same type and doping concentration comparable

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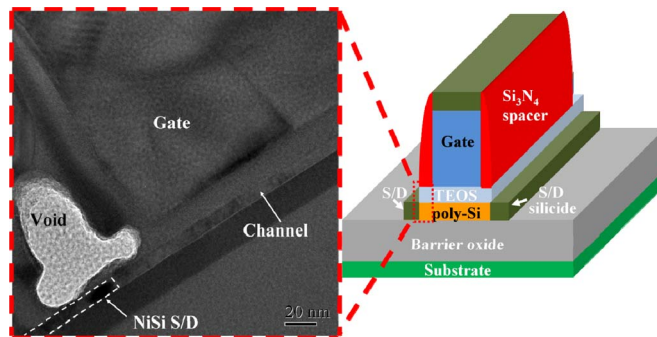


Fig. 1. Cross-sectional TEM image of a JL poly-Si TFT.

to that of the source and drain (S/D) regions were demonstrated with the FinFET [3], [4], nanowire [5], or UTB scheme [6]. This is because, for the sake of successfully shutting off the JL devices, it is essential to fully deplete the channel as operated in the OFF state, and thus, a tiny channel structure is needed. Moreover, JL devices were demonstrated not only on SOI [3], [4] but also with poly-Si-based architectures [5], [6], which are of great potential for 3-D and system-on-panel device integration. In this letter, we experimentally explore the radio-frequency (RF) characteristics and low-frequency noise (LFN) of low-voltage-operated n-type planar JL poly-Si thin-film transistors (TFTs).

II. DEVICE FABRICATION

First of all, wet oxidation was performed to form 1000-nm-thick oxide on a 6-in silicon substrate as the buried oxide, followed by the deposition of a 17-nm-thick nitride layer as the etching-stop layer. A 9-nm *in situ* heavily phosphorus-doped poly-Si layer was deposited to serve as the channel layer. The poly-Si active region was then defined by lithographic and subsequent anisotropic etching steps, followed by the successive depositions of a 13-nm tetraethyl orthosilicate (TEOS) oxide as the gate dielectric and 200-nm *in situ* n⁺ poly-Si as the gate electrode. Afterward, the gate pattern was defined by a lithographic step and subsequently etched by reactive-ion etching. Sidewall spacers were formed with a 20-nm TEOS oxide layer and a 20-nm nitride layer. To reduce the parasitic S/D resistances, a 5-nm-thick nickel layer and a 15-nm-thick titanium nitride layer were first deposited and consecutively annealed to form NiSi on the gate, and S/D regions, followed by a standard back-end process to form the metal connections. Fig. 1 shows the cross-sectional transmission electron microscopy

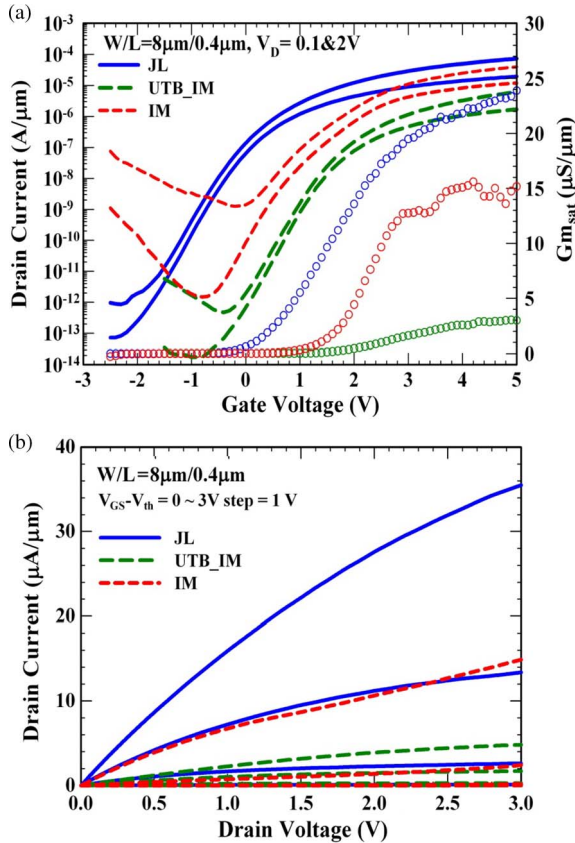


Fig. 2. (a) Transfer and (b) output characteristics of the JL, UTB_IM, and IM devices.

(TEM) image of a fabricated JL device showing NiSi in the S/D regions. In the picture, an unexpected void above the NiSi region was formed during the preparation of the test sample by focus ion beam. Two control samples, denoted as inversion mode (IM) and UTB IM (UTB_IM), were also fabricated with a similar process flow. Their major differences from the JL devices are the adoption of a 50-nm-thick undoped poly-Si channel for the IM split, which is 9 nm for UTB_IM, and the S/D junctions formed with the implant-to-silicide technique [7].

III. RESULTS AND DISCUSSION

All splits having 8-μm gate width and 0.4-μm gate length were characterized. The transfer and output I - V characteristics of the fabricated devices are shown in Fig. 2(a) and (b), respectively. In Fig. 2(a), the JL device achieves a remarkable on-current-to-off-current ratio larger than 8×10^7 , owing to the use of the ultrathin channel. In contrast, the IM device shows a high OFF-state leakage current of 10^{-9} A at $V_D = 2$ V. The worse short-channel characteristics are owing to the thicker channel of the IM device. The high OFF-state leakage current of the IM device can be suppressed with the UTB scheme at the expense of degraded on-current. Because of the heavily doped channel, the threshold voltage (V_{th}) of the JL device is -0.19 V. V_{th} is defined as the gate voltage (V_G) at a drain current (I_d) equal to $10^{-8} \times W/L$ (in amperes), where W and L are the gate width and length, respectively. The device can be adjusted to be normally off if the gate material is replaced by a metal with a higher work function (e.g., TiN).

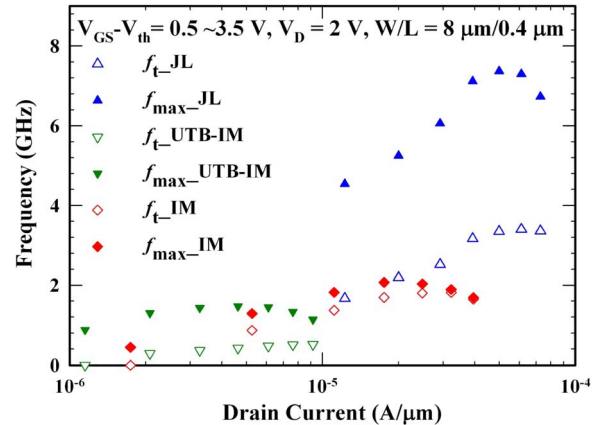


Fig. 3. f_t and f_{max} of the JL, UTB_IM, and IM devices measured at V_D of 2 V and $(V_{GS} - V_{th})$ of 0.5–3.5 V with respect to the drain current.

Shown in Fig. 2(b) are the output characteristics of the devices under various gate overdrive ($V_{GS} - V_{th}$) conditions. When $(V_{GS} - V_{th})$ is equal to 3 V, the JL device shows a drive current about 2.4 and 7.4 times higher than those of the IM and UTB_IM counterparts, respectively. This is mainly attributed to the reduction in the channel resistance with the JL schemes.

The cutoff frequency f_t and the maximum frequency of oscillation f_{max} of all splits with respect to the drain current at $V_D = 2$ V are shown in Fig. 3. The peak f_t and f_{max} are around 1.8 and 2 GHz, respectively, for the IM device and 0.51 and 1.47 GHz, respectively, for the UTB_IM device. In contrast, the JL device exhibits an f_t of 3.4 GHz and an f_{max} of 7.4 GHz, which are almost 2 and 3.7 times higher than those of the IM counterpart, respectively, owing, in large part, to the larger transconductance (g_m) of the JL device, as shown in Fig. 2(a).

Fig. 4(a) shows the frequency dependence of the measured drain-current noise power spectral density (S_{id}) operated under $(V_{GS} - V_{th})$ of 0.5 V between 10 Hz and 10 kHz for all splits at $V_D = 0.1$ V. For the JL device, the S_{id} characteristics are four orders of magnitude lower than those of the IM counterparts. This can be ascribed to the distinct conduction mechanism of the JL device [3]. In addition, the larger grain size of the *in situ* phosphorus-doped poly-Si channel can also meliorate the LFN [8]. To identify the noise source, the normalized noise power spectrum density (S_{id}/I_d^2) and the transconductance-to-drain-current ratio squared $[(g_m/I_d)^2]$ versus the drain current for the devices are shown in Fig. 4(b). From the results, it is inferred that the noise in the JL device is mainly dominated by Hooge mobility fluctuation [9] since S_{id}/I_d^2 is proportional to $1/I_d$ and the Hooge parameter is about 1.4×10^{-4} . As has been pointed out previously [10], the Hooge parameter decreases with increasing doping level. This is because an increase in doping level tends to reduce the band bending at the grain boundaries and therefore increases the current drive (higher carrier concentration and higher effective mobility). It thus improves the LFN for the heavily doped JL device as compared with the undoped channel of the IM counterparts. On the contrary, the noises in the IM and UTB_IM devices are mainly dominated by carrier number fluctuation [11] because S_{id}/I_d^2 is proportional to $(g_m/I_d)^2$ [the dashed lines in Fig. 4(b)]. The dc and ac characteristics of all splits are compared in Table I.

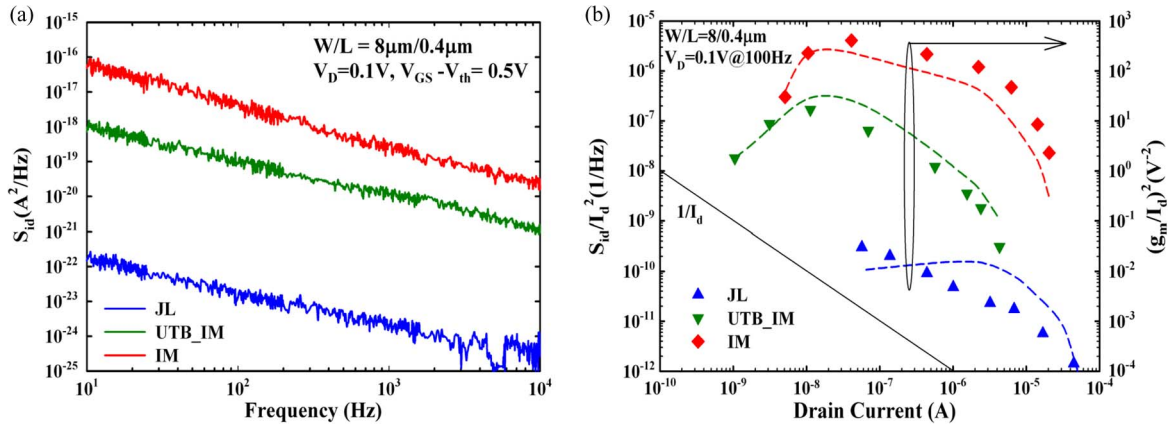


Fig. 4. (a) Drain-current noise power spectral density (S_{id}) versus frequency at $V_D = 0.1$ V and $(V_{GS} - V_{th}) = 0.5$ V. (b) (Symbols) S_{id}/I_d^2 and (dashed lines) $(g_m/I_d)^2$ versus drain current for all splits of the devices.

TABLE I
COMPARISON OF THE IM AND UTB_IM POLY-Si
TFTs AND THE JL POLY-Si TFT

	JL	UTB_IM	IM
S.S. (mV/dec)	309	305	326
DIBL (mV)	161	143	277
V _{th} (V)	-0.19	1.6	1.5
G _{msat} (μS/μm)	23.89	3.01	15.16
I _{on} /I _{off}	8 × 10 ⁷	1 × 10 ⁷	3.2 × 10 ⁴
f _t (GHz)	3.36	0.51	1.82
f _{max} (GHz)	7.37	1.47	2.07
S _{id} (A ² /Hz)@10Hz	5 × 10 ⁻²¹	3 × 10 ⁻¹⁸	2 × 10 ⁻¹⁶

IV. CONCLUSION

n-type planar ultrathin JL poly-Si TFTs have been fabricated and characterized with emphasis on RF and LFN performances. For the RF characteristics, the JL device with a gate length of 0.4 μm can achieve an f_t of 3.37 GHz and an f_{max} of 7.37 GHz at a V_D of 2 V, compared with 1.8 and 2 GHz, respectively, for the IM device. As far as LFN is concerned, the inherent bulk conduction feature of the JL devices improves the LFN and achieves higher signal-to-noise ratio as compared with that of the IM devices. Simplification in device fabrication using *in situ* doped poly-Si as channel and S/D materials, as well as the remarkable device performances verified in this work, confirms the potential of the JL scheme for system-on-panel applications.

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