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Negative current feedback OTA with application to 250 MHz Gm-C filter

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Abstract A 4th-order low-pass Gm-C filter for high speed wireless/wireline system is realized in 0.18 μm CMOS process. The high speed filter is designed based on operational transconductance amplifier (OTA) biquad sections. As well known, large transconductance is required for high speed applications, and thus the conventional source degeneration topology, which operates with the trade-off between linearity and transconductance, should be improved. In this paper, the proposed OTA uses negative current feedback topology to maintain linearity while increasing transconductance for high speed application, and a 4th-order low-pass filter is realized by using the OTA as a building block. Fabricated in 0.18 μm CMOS technology, the −3 dB filter frequency response at 250 MHz is obtained. The measured HD3 performance is about −40 dB while the filter consumes 32 mW power at a 1.8 V supply voltage.

Keywords OTA · Filter · HD3

1 Introduction

High-performance high speed filters play an important role in present communication systems. For the wireless applications, the mobile terminals require high speed filters for channel selection at inter-mediate frequency band. Usually, performance related to the linearity, group delay, noise, and power efficiency should all be taken into consideration.

The performance of the Gm-C filter is highly dependent on the OTA building block. Owing to the open loop topology, most of the papers and researches work on the linearity of the voltage-to-current conversion [1–7]. In this paper, the source degeneration structure, which has further improved linearity, is described. The linearity of the conventional source degeneration circuit would be degraded since the degenerated resistor is small when achieving large transconductance for high speed application. Voltage feedback topology [8, 9] is a solution to enhance the linearity of the traditional source degenerated structure. Based on closed-loop configurations, the linearity is proportional to the inverse loop gain. Unfortunately, the loop gain is highly degraded at high speed, and thus the improved linearity is not sufficient. Therefore, a negative current feedback circuit which features a higher gain-bandwidth would be proposed.

The basic structure of the conventional source degeneration circuit is discussed in Sect. 2. The design of the modified source degeneration circuit is introduced in Sect. 3. The 4th-order linear phase low-pass filter composed of two OTA-C biquad sections is described in Sect. 4. The cutoff frequency is designed at 250 MHz. The value is usually required by the Ultra-wide band (UWB) wireless system and the high speed read channel hard/optic disk storage. Results are shown in Sect. 5. Finally, some conclusions are addressed in Sect. 6.

2 Conventional source degeneration OTA

Figure 1 shows the circuit of the conventional source degenerated OTA [10]. The output current is related to the input voltage by the following equation:

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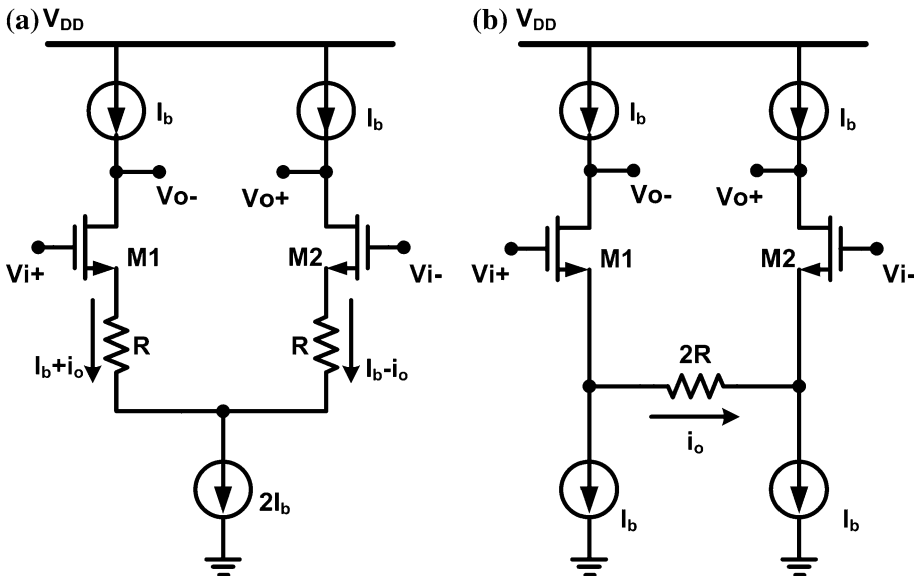

Fig. 1 Implementation of the conventional source degeneration OTAs

$$i_O = v_{id}\left(\frac{\sqrt{2K_{(1,2)}I_b}}{1+N}\right)\sqrt{1-\left(\frac{v_{id}}{2(1+N)V_{DS(1,2)(sat)}}\right)^2} \quad (1)$$

$$G_m = \frac{1}{R}\left(\frac{N}{1+N}\right) \quad (2)$$

$$HD_3 = \frac{1}{32}\left[\frac{v_{id}}{(1+N)\left(V_{DS(1,2)(sat)}\right)}\right]^2 \quad (3)$$

where $v_{id} = V_{i+} - V_{i-}$, $V_{DS(1,2)(sat)} = V_{GS(M1,M2)} - V_{tn}$, and $N = g_{m(1,2)}$ R is the source degeneration factor. By using the equation, we can find the transconductance is reduced by a factor of 1 + N and the third harmonic distortion is reduced by the square of the same factor. It is clear that N should be a large value. This condition not only makes the OTA tunable, as shown in (2), but also increases the linearity performance, as shown in (3). The disadvantage of the technique is the higher current and larger aspect ratio as compared with the fully differential pair. For the same power consumption condition at high speed operation, we need to decrease R for larger transconductance, and thus the performance of HD3 would be highly degraded.

Although the circuits in Fig. 1(a, b) show the same voltage-to-current relationship, they present different properties. In Fig. 1(a), the resistor will provide a voltage drop, and then the range of the common-mode voltage is reduced. In Fig. 1(b), the noise of the current source will appear at the output, and this source will dominate the noise performance. Mismatch of the current sources would also reflect as the input offset.

3 Proposed source degeneration OTA

Figure 2 shows the circuit of proposed source degenerated OTA. In this figure, transistors M1 to M4 are the input stage of the OTA, and transistor M17 would operate in the linear region to replace the passive resistor. The linear region transistor adds the ability of continuous tuning with the cost of degraded linearity. Thus, we can adjust the voltage at node Vt to obtain desired transconductance. These transistors discussed above work on the same functions as the traditional degenerated OTA. In this circuit, transistors M5 to M8 are added to form the negative current feedback circuit, and the resistance seen from the source of transistors M1 and M2 would become small when the feedback loop gain is large. Therefore, the factor N shown in (3) can be increased without using large value of R. Thus, we can conclude the OTA has the same transconductance with improved linearity. Through the use of current mirrors M9 and M10, transistors M11 to M16 form the output stage for high output impedance. In this circuit, the output common-mode voltage would be fixed to a reference value by using a common-mode feedback (CMFB) circuit to adjust the voltage at node Vcm.

The proposed circuit operates as follows. At first, an increased input voltage V_{i+} is given, but the voltage at node V_x does not follow this variation. This will make the voltage between the gate and the source of transistor M1 to increase. The drain current of transistor M1 increases and so does the drain current of transistor M9. Because the drain current of transistor M9 increases, the voltage across the drain and the source of transistor M9 also increases. For this reason, the gate voltage of transistor M5 decreases. Then, the

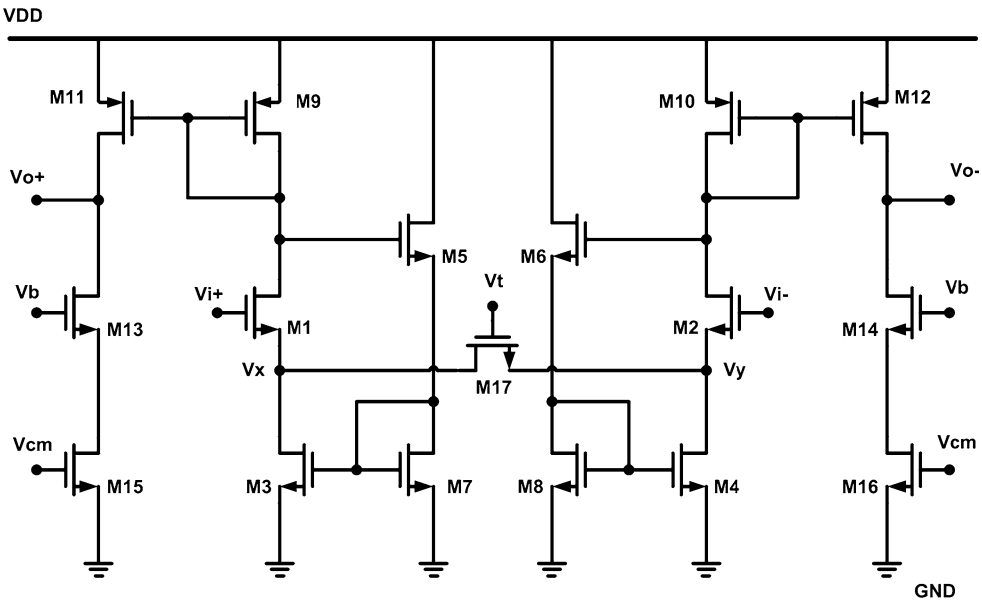

Fig. 2 Implementation of the proposed negative current feedback OTA

gate-to-source value of transistor M5 decreases and so does the drain current of transistor M5. The decreased current will mirror through transistor M3. Therefore, the drain current of transistor M1 will be pulled down, and the voltage at the source node will be pushed up. Therefore, the negative current feedback circuit would enforce the voltage at node V_x to follow the variation of the input voltage.

In this circuit, the drain currents of transistors M1 and M2 can be expressed as

$$I_{D1} = I_B + g_{m(1,2)}(V_{i+} - V_x) \tag{4}$$

$$I_{D2} = I_B + g_{m(1,2)}(V_{i-} - V_y) \tag{5}$$

where I_B is the drain current of transistors M1 and M2 when biased at only the input common-mode voltage. The current which flows through the transistor M17 is given by

$$i_{xy} = \frac{V_x - V_y}{r_{ds17}} \tag{6}$$

where r_{ds17} is the resistance of linear region transistor M17. Also, the drain current of M1 and M2 can be described by

$$I_{D1} = I_{D3} + i_{xy} \tag{7}$$

$$I_{D2} = I_{D4} - i_{xy} \tag{8}$$

where $I_{D1} + I_{D2} = I_{D3} + I_{D4} = 2I_B$. Combining the equations shown in (4–8), the differential output current can be given by

$$i_o = I_{D1} - I_{D2} = g_{m(1,2)}(v_{id} - V_x + V_y) = 2i_{xy} + I_{D3} - I_{D4} \tag{9}$$

Now, the drain current of transistors M3 and M4 are determined by the drain current in transistors M5 and M6 due to the current mirror pairs. Therefore, the current can be obtained by

$$I_{D3} = \frac{1}{2}K_{n(5,6)}(V_{DD} - V_{sg9} - V_{gs(7,8)} - V_{thn(5,6)})^2 \tag{10}$$

$$I_{D3} = \frac{1}{2}K_{n(5,6)}(V_{DD} - V_{sg10} - V_{gs(7,8)} - V_{thn(5,6)})^2 \tag{11}$$

where $K_n = \mu_n C_{ox}(W/L)$ is the NMOS device parameter. We should note that the gate-source voltage of transistors M9 and M10 can be given by

$$V_{sg9} = \frac{2I_{D1}}{g_{m(9,10)}} + |V_{thp(9,10)}| \tag{12}$$

$$V_{sg10} = \frac{2I_{D2}}{g_{m(9,10)}} + |V_{thp(9,10)}| \tag{13}$$

By substituting (12) and (13) into (10) and (11), we can find that

$$I_{D3} - I_{D4} = (I_{D2} - I_{D1})\alpha \tag{14}$$

where $\alpha = (2V_{DD} - V_{gs(7,8)} - V_{thn(5,6)} - |V_{thp(9,10)}| - \frac{4I_B}{K_{p(9,10)}(V_{sg(9,10)} - |V_{thp(9,10)}|)}) \frac{K_{n(5,6)}}{K_{p(9,10)}(V_{sg(9,10)} - |V_{thp(9,10)}|)}$

The factor α defines the negative feedback gain of the feedback topology. By substituting (14) into (9), the relationship between the differential output current and the voltage across transistor M17 is shown to be

$$I_{D1} - I_{D2} = 2\frac{V_x - V_y}{r_{ds17}} - (I_{D1} - I_{D2})\alpha \tag{15}$$

Furthermore, using the equations shown in (15) and (9), the voltage across transistor M17 can be described as

$$V_x - V_y = \frac{(1+\alpha)N_n}{(1+\alpha)N_n + 2} v_{id} \tag{16}$$

where $N_n = g_{m(1,2)} \times r_{ds17}$ is again the source degeneration factor. From the saturation formulas of transistors

M1 and M2, we can get the relationship between differential output current and the input voltage

$$I_{D1} = \frac{1}{2}K_{n(1,2)}\left(V_{i+} - V_x - V_{thn(1,2)}\right)^2 \quad (17)$$

$$I_{D2} = \frac{1}{2}K_{n(1,2)}\left(V_{i-} - V_y - V_{thn(1,2)}\right)^2 \quad (18)$$

Substituting (16) into (17) and (18), the relationship of the output current and the input voltage is given by

$$i_o = v_{id}\left(\frac{\sqrt{2K_{n(1,2)}I_B}}{2+(1+\alpha)N_n}\right) \times \sqrt{1-\left(\frac{v_{id}}{2(2+(1+\alpha)N_n)V_{DS(1,2)(Sat)}}\right)^2} \quad (19)$$

$$G_m = \frac{1}{r_{ds17}}\left(\frac{N_n}{2+(1+\alpha)N_n}\right) \quad (20)$$

Again, the HD3 can be derived by using the Taylor series expansion and obtained as follows:

$$HD_3 = \frac{1}{32}\left[\frac{v_{id}}{(2+(1+\alpha)N_n)V_{DS(1,2)(sat)}}\right]^2 \quad (21)$$

From (21), the HD3 could be improved by giving a larger α, and the linearity could be improved without large resistance of r_{ds17}. Therefore, the proposed negative current feedback circuit provides a loop gain of α to increase the performance of HD3 as described. The simulated loop gain at the 250 MHz is about 15 dB. Compared with the voltage feedback topology proposed in [9], an enhancement of 6 dB is achieved.

For high speed application, thermal noise is more important than the flicker noise. The thermal noise can be modeled by a current source connected between the drain and the source with a spectral density and can be given by

$$\overline{I_n^2} = 4kT\gamma g_m \quad (22)$$

where k is the Botzmann constant, T is the absolute temperature, γ is the device operation point parameter, and g_m is the source conductance of a transistor. Using the thermal noise model, the total output noise spectral density of the modified source degeneration circuit can be derived:

$$\overline{I_{out,n}^2} = 4\left(4kT\gamma g_{m(9,10)}\right) + 2\left(4kT\gamma g_{m(1,2)}\right) + \left[2(4kT\gamma g_{m17}) + 4(4kT\gamma g_{m3}) + 2(4kT\gamma g_{m5})\right] \times \left(\frac{(1+\alpha)g_{m(1,2)}r_{ds17}}{1+(1+\alpha)g_{m(1,2)}r_{ds17}}\right)^2 \quad (23)$$

Therefore, the input-referred noise spectral density could be calculated as

$$\overline{V_{in,n}^2} = \overline{I_{out,n}^2}\left(\frac{2+(1+\alpha)g_{m(1,2)}r_{ds17}}{g_{m(1,2)}}\right)^2 \quad (24)$$

From (23), the added current feedback circuit provides additional noise to the output nodes. As well, the large aspect ratios of the input transistors and small aspect ratios of the load transistors should be designed to keep required noise performance.

Since the supply the circuit bias point depends on the voltage between supply and ground, the circuit operation point is set by the supply voltage directly. The main advantage of this self-biasing circuit is no extra bias circuit, which will not consume power. The transconductance variation affected by power supply will be suppressed by the current loop gain, and the PSRR to the output node is also suppressed by the output resistance of transistors M11/M12.

4 The 4th-order filter structure

In this section, the 4th-order filter circuit will be presented. There are two design approaches to design active filters. One is based on realizing the pole-zero locations of the filter with cascaded first-order and second-order stages, and the other is based on synthesizing the RLC prototype of passive elements. For higher order filter synthesis in RLC network, it is hard to control the sensitivity and stability. Therefore, we choose the first method owing to simple circuit topology.

In order to have maximum flatness of the group delay, the equiripple prototype of the filter is implemented. The transconductances of the OTAs and loading capacitors for the individual biquad sections are given in Table 1. Moreover, the fourth-order low-pass filter composed of two OTA-C biquad sections is shown in Fig. 3. In the filter circuit, only two CMFB circuits are required for each biquad section because some output nodes of OTAs are connected to each other. The −3 dB cutoff frequency of the filter is adjusted by tuning the transconductance, which means adjusting the gate voltage of transistor M17 in the proposed OTA, to compensate for the process and the temperature variation. By using the result form Eq. (23), the noise of the biquad cell is the summation of each transconductor cell referred to the input nodes. By setting the pole-zero position of each biquad section, the gm versus loading capacitance should be selected by considering power versus noise optimization. Shown in Table 1, the transconductance is chosen at first for our noise

Table 1 Parameters of each biquadratic section

	Q	Gm1 (ms)	C (pF)	Gm2 (ms)
Biquad 1	0.5573	2.95	1.95	5.9
Biquad 2	1.0652	2.95	0.8	2.95

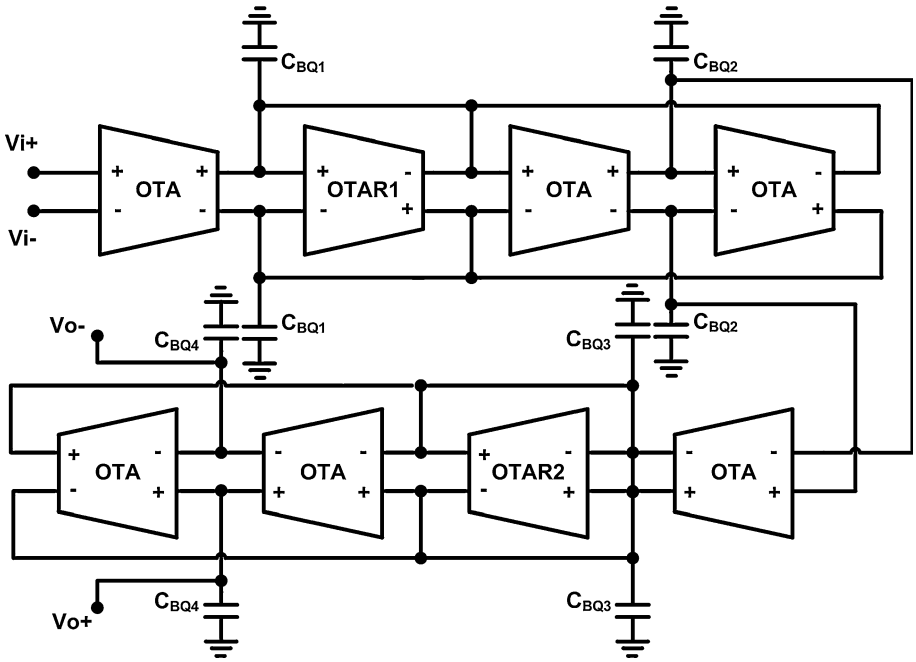

Fig. 3 Implementation of the 4th-order filter

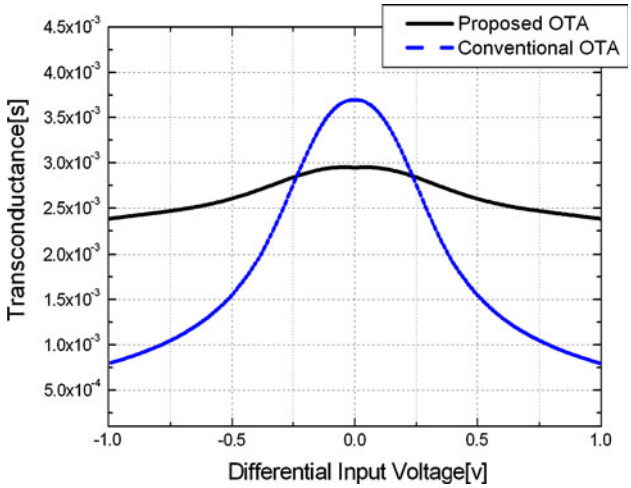

Fig. 4 Simulated transconductance of the conventional and proposed circuits with the relationship to input differential voltage

requirement, and then the loading capacitor is selected from the desired pole-zero frequency.

An output buffer is required to measure the entire filter response, and thus an extra OTA is added

5 Results

Figure 4 shows the simulated transconductance of the OTA at different input signals. By giving the same degeneration resistor, the dotted line shows the transconductance of the conventional source degeneration and the solid line shows the proposed circuit. We can find that the proposed circuit has more flatness performance of the transconductance, which means the linearity of the proposed circuit is indeed improved. The difference between the conventional and proposed circuits comes from the additional transistors M5 to M8 shown in Fig. 2. Also, equal branch current is used to achieve 3mS transconductance for comparison. The size for these additional transistors is W/L = 46/0.4 u. The input common-mode voltage is set to 1 V under the 1.8 V supply. In the simulation, the proposed circuit has more than 10 dB improvement of HD3 than the conventional source degeneration circuit by giving a 200 MHz input signal.

The OTA and the filter were designed in the TSMC 0.18 μm CMOS process. The chip micrograph and layout view are shown in Fig. 5 with the active area less than 0.23 mm^2. The circuit operates at a 1.8 V supply with the power consumption of 32 mW. Figure 6 shows the measured frequency response of the proposed filter. The -3 dB cutoff frequency is 250 MHz, which meets our requirement. The degraded magnitude of the filter is owing to small output impedance loading after the final stage. The group delay is less than 5 ns at filter cutoff frequency. Figure 7 shows the HD3 performance of the filter. The performance of about −40 dB could be obtained by giving an 80 MHz 0.4 Vpp input signal. Compared with the calculation results from Eq. (21), the −43 dB performance is obtained. The 3 dB difference between the calculation and measurement is from the high frequency non-ideal effect by parasitic capacitance. When a two-tone test is applied to the filter cut-off frequency, 37 dB IM3 is obtained.

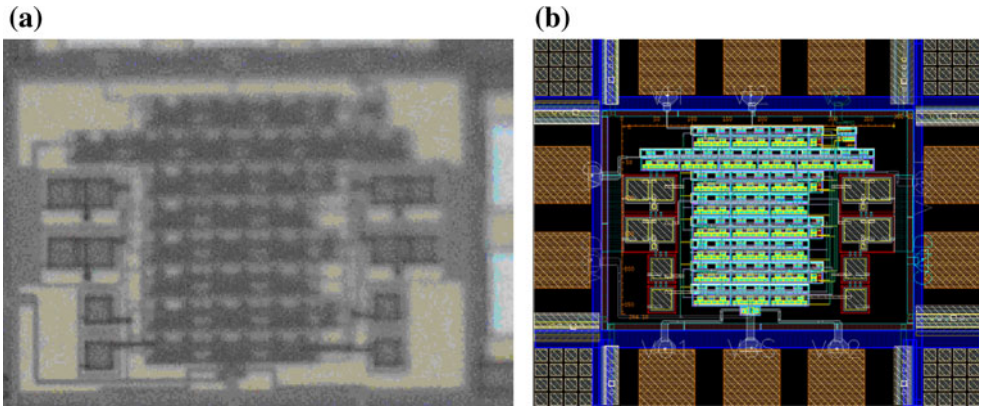

Fig. 5 **a** Chip micrograph and **b** Layout view

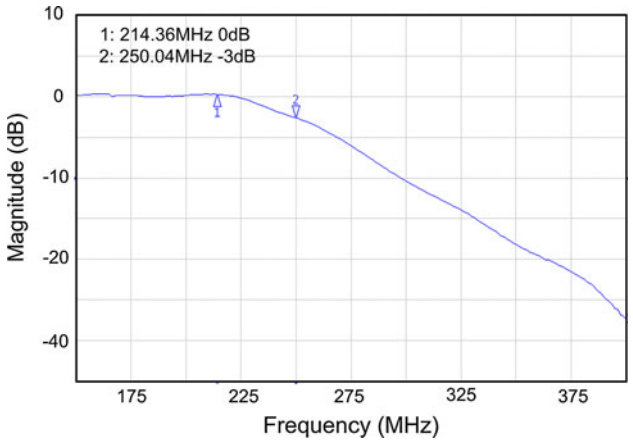

Fig. 6 Measured frequency response of the proposed filter

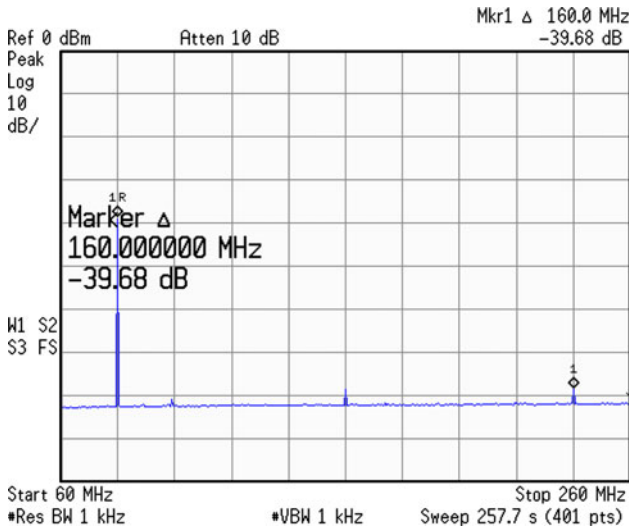

Fig. 7 Measured HD3 of the proposed filter

The measured common-mode rejection ratio (CMRR) is 33 dB at low frequency, and the integrated output in-band noise is 256 μVrms, indicating a SNR of 55 dB at −40 dB THD. From the measured noise, we can derive the loop transfer function from the internal nodes to the input, and find that the noise is approximately equal to the $(8)^{1/2}$ times transconductor noise within the band of interest. Therefore, the input-referred noise of each transconductor is about 90.5 uV from the measurement. We should note that in Eq. (24), an 80 uV performance is calculated. The larger noise obtained in measurement is owing to the addition of output buffer circuits. Table 2 shows the performance summary of the circuit. A FOM [4] performance is also reported for this work.

Table 2 Performance summary of the filter

Reference	JSSC 2003 [11]	TCAS-I 2006 [12]	This work
Technology	0.5 μm CMOS	0.35 μm CMOS	0.18 μm CMOS
Supply voltage (V)	3.3	3.3	1.8
Filter order	4	4	4
−3 dB frequency (MHz)	100	550	250
Linearity	−40 dB IM3@ 100 MHz 350 mV_{pp}	−40 dB IM3@ 500 MHz 283 mV_{pp}	−40 dB HD3@ 240 MHz 400 mV_{pp}
Noise (nV/sqrt(Hz))	70	42.6	16.2
Power consumption (mW)	86	140	32
FOM (fJ)	1	0.86	0.2

6 Conclusions

In this paper, a conventional source degeneration circuit is described and its major problem at high speed operation is also discussed. Then, a modified source degeneration circuit is proposed to solve the problem. This OTA circuit utilizes the negative current feedback approach to improve linearity. In addition, this paper also describes the structure of the 4th-order Gm-C low-pass filter. The measured -3 dB cutoff frequency of the filter is about 250 MHz and we can conclude that the filter operate well at the required specification.

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