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Inhibition of bird's beak in LOCOS by new buffer N_2O oxide

T.S. Chao, J.Y. Cheng and T.F. Lei

Indexing terms: Silicon, Oxidation

In the Letter new N_2O buffer oxide was used to replace the conventional dry oxide for LOCOS isolation. This new structure can result in a shorter bird's beak than the conventional structure without adding extra steps and inducing the defect in silicon substrate.

Introduction: Local oxidation of silicon (LOCOS) has been used as the workhorse isolation technology for MOS devices over the past 20 years [1]. The initial idea is to use nitride as a mask for oxidation. A buffer oxide is used to cushion the transition of stress between the silicon substrate and the subsequently deposited nitride. The edge force from nitride to silicon substrate decreases as the thickness of the buffer oxide increases. Large stress from nitride results in the formation of dislocation under the edge during a later high-temperature oxidation process. The minimum buffer oxide thickness that can be used to avoid the formation of dislocation should be at least one-third the thickness of the nitride layer [2]. Oxidising species can diffuse laterally and oxidise the silicon under the edge of the nitride film, causing a so-called 'bird's beak'. Conventionally, bird's beak encroachment limits the scaling of channel widths to around 1.2 – 1.5µm. Many methods have been proposed to reduce the effect of bird's beak, such as sealed interface local oxidation (SILO) [3], nitrogen implantation for local oxidation (NILO) [4], poly-buffered LOCOS [5] and fully recessed oxide LOCOS [6]. The proposal of these methods is to achieve sealing of the silicon surface and maintain a minimum stress at the edge. As for sealing the silicon surface, instead of using nitride directly to seal the silicon surface, nitrogen implantation is used to inhibit the oxidation in the NILO method. However, NILO needs a high dose of N_2^+. In this Letter N_2O oxide is used as the new buffer oxide, replacing the conventional dry oxide buffer oxide. The advantage of this structure is that N_2O oxide has a native N atom (4atm.%), which piles up at the SiO_2/Si interface during the oxidation process. This nitrogen layer has been proved to retard the oxidation of oxygen species. Hence this method is simple without additional step-like high-dose N implantation in NILO, or nitride film in SILO.

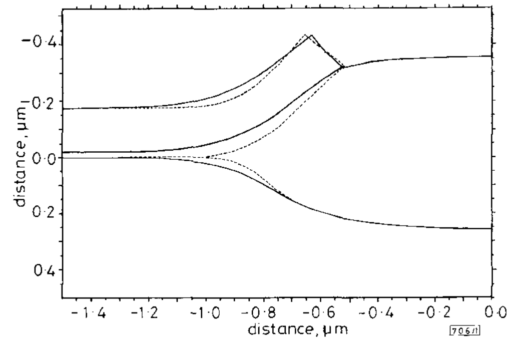

Fig. 1 *Cross-section of LOCOS simulated by SUPRENUM 4 of conventional O_2 buffer oxide, and new N_2O buffer oxide*

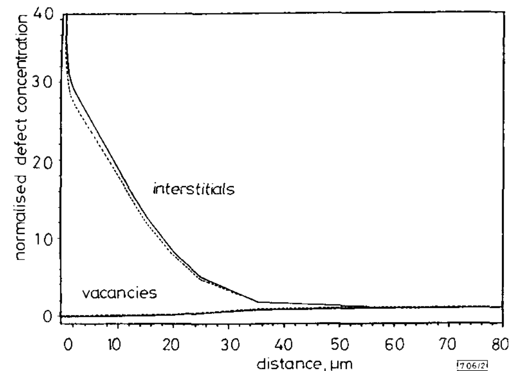

Fig. 2 *Normalised defect concentration, vacancies and intersitial, of O_2 oxide and N_2O oxide*

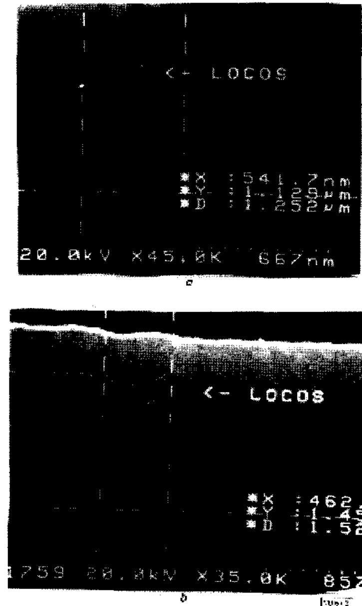

Fig. 3 *SEM photographs of O_2 and N_2O sample after LOCOS processes*

a O_2 sample
b N_2O sample

Simulation and result: LOCOS was simulated in SUPRENUM 4. The structure of N_2O oxide was implemented as a two-layer structure [7]. The top layer is pure oxide. The bottom layer on the sili-

con substrate is the oxynitride (20Å). This is because, during the N_2O oxidation, nitrogen only piles up at the SiO_2/Si interface. This layer had been characterised as an oxynitride film with a refractive index $N = 1.77$ and thickness around 20Å. Fig. 1 shows the result of LOCOS with a buffer of O_2/N_2O oxide. For the O_2 sample, the simulated structure is Si_3N_4 (1500Å)/SiO_2 (200Å)/Si. For the N_2O sample, the structure is Si_3N_4 (1500Å)/ SiO_2 (180Å)/oxynitride (20 Å)/Si. The samples were oxidised at 980°C for 140min. Clearly, the N_2O sample exhibits a shorter bird's beak (4800Å) than conventional O_2 (6400Å). The vacancies and interstitial under the field oxide were also simulated. Fig. 2 shows the normal defect concentration of vacancies and interstitial for N_2O sample and O_2 sample. There is no difference for vacancies and little increase in interstitial for the N_2O sample. In the experiment, 6 in, *p*-type (100), 15–25Ωcm wafers were used. After RCA cleaning processes, samples were oxidised in N_2O and O_2/N_2 (1:6) ambients to grow 100Å oxide at 900°C for 100min. Samples were then put into an LPCVD system to deposit 1200Å Si_3N_4 film. Active regions were defined and etched by an Si_3N_4 etcher. Wet oxidation was conducted at 980°C for 80min. The bird's beak of the sample was characterised by SEM. Fig. 3*a* and *b* show the SEM results. In Fig. 3*a* the conventional O_2 oxidising encroaches significantly into the SiO_2/Si interface, while in Fig. 3*b*, in the N_2O sample, the encroachment is retarded. The length difference from the flat on the field oxide to the bird's beak for these two samples is 800Å.

Conclusion: The N_2O oxide used as the new buffer oxide for LOCOS has been investigated. From the simulation, this new structure causes no additional effect on vacancies and interstitial, and reduces the length of the bird's beak simultaneously. The new structure is simple, just replacing O_2 by the N_2O, and could be a candidate for future isolation technology.

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Low-frequency noise of selectively dry-etch gate-recessed GaAs MESFETs

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Indexing terms: MESFETs, Reactive ion etching, Semiconductor device noise

The authors report the input referred low-frequency noise (2–100 kHz) spectra of 0.2µm-gate-length GaAs MESFETs which were gate-recess-etched using a selective Freon 12 based dry-etching process. For comparison, the noise spectra of nonselective wet-chemical, ammonia-based gate-recess-etched devices are also presented. Little change in low-frequency noise performance is observed for devices dry-etched for 30–50s, demonstrating the latitude of the dry-etch process. Additionally, the input referred noise of the wet-etched devices was greater than that of 30, 40 and 50s dry-etched devices, suggesting that the dry-etching process may passivate traps contributing to the low-frequency noise component of the MESFETs.

Introduction: One of the yield-limiting processes in short-gate-length (< 0.25µm) MESFET- or HEMT-based monolithic microwave integrated circuits is device-to-device reproducibility of the gate-recess etch depth. This has resulted in considerable research into selective gate-recess etching processes where highly reproducible gate-recess depths can be achieved by selective etching of the epilayers in the transistor material structure. A highly uniform Freon 12 based selective dry-etch gate-recess process with etch selectivity of 4000:1 between GaAs and AlGaAs has been successfully demonstrated in the fabrication of high-performance GaAs MESFETs [1]. The microwave gain and noise performance of these devices was comparable with state-of-the-art pseudomorphic HEMTs [2].

To date, little work has been reported on the low-frequency noise performance of dry-etched MESFETs and HEMTs, despite the fact that it is primarily determined by trapping mechanisms in the device channel, and so may be sensitive to damage introduced by the etching process. Transistor low-frequency noise performance is also a figure of merit in oscillator-based microwave circuits where the low-frequency noise component is converted into microwave phase noise by active device nonlinearities [3].

In this Letter the low-frequency noise performance of GaAs MESFETs gate-recessed using a Freon 12 process is presented and compared with nonselective wet-chemical-etched devices.

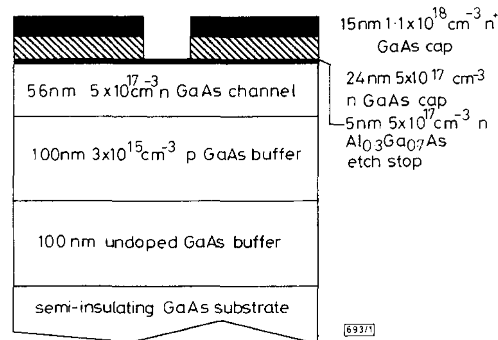

Fig. 1 *Material structure*

Device fabrication and measurement system: The material structure on which devices were fabricated is shown in Fig. 1. The structure was grown by molecular beam epitaxy on a (100) semi-insulating GaAs substrate. All levels of lithography used to fabricate the 60 µm-wide MESFETs of this study were written using a Leica Cambridge EPBG-5 Beamwriter. The 0.2µm footprint T-gate was defined using a trilayer resist system [4]. The selective dry-etched gate-recess was performed using a Freon 12 based chemistry to etch the GaAs cap layers (total thickness 39 nm), stopping on the 5nm $Al_{0.3}Ga_{0.7}As$ etch stop layer [1]. Four samples were dry-etched