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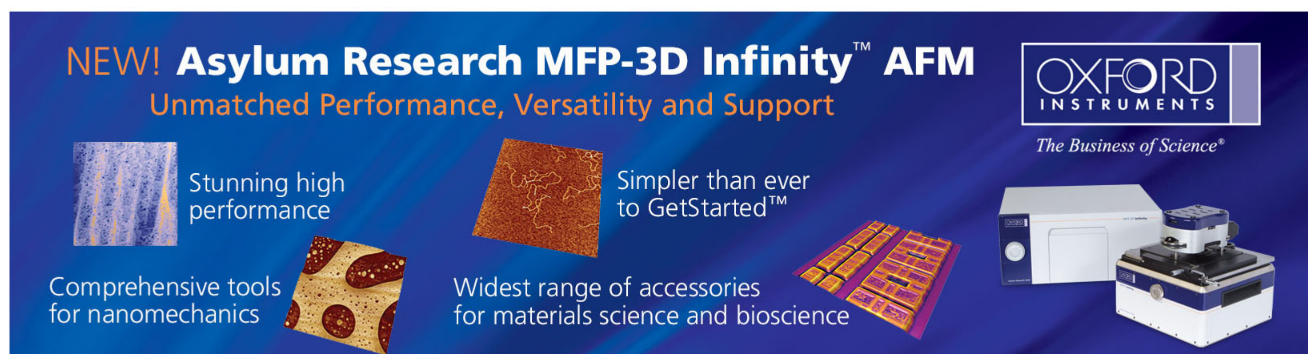

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Abnormal interface state generation under positive bias stress in TiN/HfO_2 p-channel metal-oxide-semiconductor field effect transistors

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This Letter studies positive bias stress-induced abnormal interface state on TiN/HfO_2 p-channel metal-oxide-semiconductor field effect transistors. It can be found that the degradation is associated with electron trapping, resulting in V_{th} shift but without subthreshold slope degradation. However, charge pumping current (I_{CP}) shows a significant degradation after stress. Accordingly, the impact ionization-induced N_{it} located HfO_2/SiO_2 is proposed to demonstrate the I_{CP} degradation. The AC stress with several frequencies is used to evidence the occurrence of impact ionization. Further, the device with additional pre-existing N_{it} located SiO_2/Si has insignificant degradation due to reduction in stress electric field. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4752456]

The physical limitation of the silicon dioxide (SiO_2) as gate insulator has achieved the point where its thickness is approaching to a few atomic layers thick.[1,2] Below the physical thickness 12 Å, the significant gate leakage current results in a volume active power consumption, leading a worse reliability of metal-oxide semiconductor field effect transistors (MOSFETs). To avoid this serious issue, high-k dielectrics have been introduced as hafnium (Hf)-base, zirconium, aluminum oxides[3–6] and heavily investigated as a replacement for conventional SiO_2 gate insulator. However, metal gate/high-k stack has to face many critical issues such as defects in high-k material, which can lead to undesired transport through the dielectrics and trapping-induced instabilities such as negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), and time-depended dielectric breakdown (TDDB), and hot carrier injection (HCI) in metal gate/high-k devices to realize the influence of high-k dielectric characteristics on devices under electric stress.[7–13] However, for p-FETs, the behavior of off-state stress on gate/high-k devices has not yet been studied. Therefore, this Letter investigates the phenomenon for TiN/HfO_2 p-MOSFETs under positive bias stress (PBS). And we found that the stress-induced N_{it} is generated at interface between high-k layer and buffer oxide, instead of channel interface.

The TiN/HfO_2 p-MOSFETs were studied in this paper based on the high-performance 28-nm CMOS technology. Both devices were fabricated using a conventional self-aligned transistor flow through the gate first process. For the gate first process devices, 10 Å and 30 Å of high quality thermal oxide were, respectively, grown on a (100) Si substrate as buffer oxide layers. After standard cleaning procedures, 30 Å of HfO_2 films were sequentially deposited by atomic layer deposition. Next, 10 nm of TiN films were deposited by radio frequency physical vapor deposition, followed by poly-Si deposition as a low resistance gate electrode. The dopant profile is $\sim 10^{20}\,cm^{-3}$ and $\sim 10^{18}\,cm^{-3}$ for source/drain and channel, respectively, and activation were performed at 1025 °C. And the doping concentration of poly gate is $\sim 10^{20}\,cm^{-3}$. In this study, the dimensions of the selected devices were 10 μm and 1 μm in width and length, respectively. The device with buffer thickness of 10 Å was subjected to the positive gate voltage (V_G) condition with 2V+flatband voltage (V_{FB}). The stress was briefly interrupted to measure the drain current-gate voltage (I_D-V_G) and charge pumping current (I_{CP}). All experimental data were measured using an Agilent B1500/B1530A semiconductor parameter analyzer.

Figure 1 shows the PBS-induced drain current (I_D)-gate voltage (V_G) characteristic under semi-logarithmic scale of TiN/HfO_2 p-MOSFETs (device A). The stress condition V_G was selected 2 V, adding V_{FB} to be a correction term. As the result, the degradations on device during PBS show positive shift and decrease in threshold voltage (V_{th}) and drain current (I_D), respectively. The subthreshold slope (SS) is extracted by I_D ranges 10^{-7}A to 10^{-9} A. In addition, the I_D-V_G under semi-logarithmic scale shows a parallel shift at subthreshold region without stretch out, indicating invariant of SS after PBS. This is because the PBS-induced charge trapping is associated with amount of traps and stress electric field. As carriers could rely on tunneling or/and thermal emission to cross oxide barrier height, charge trapping behavior should occur and no damaging interface state at Si/SiO_2 ($N_{it,\ Si/SiO2}$), especially for ultra-thin buffer oxide.[10,11] Additionally, the C-V curve also shows the occurrence of electron trapping at high-k layer as shown in the inset of Figure 1. It can be seen that the capacitance of gate terminal to body terminal versus gate voltage (C_{GB}-V_G) curve exhibits a hysteresis window as V_G implements a dual-sweep (forward and reverse) before and

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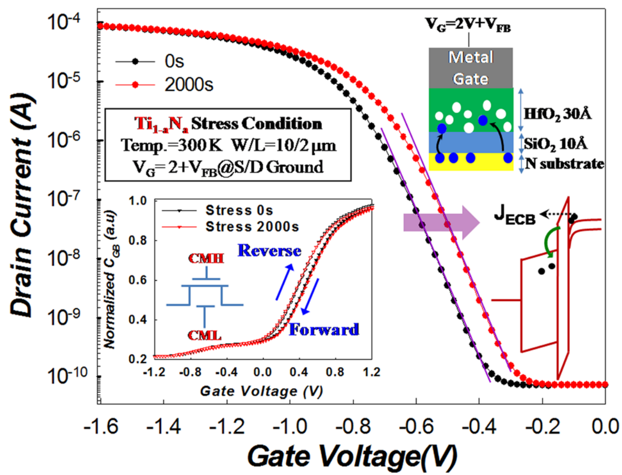

FIG. 1. I_D-V_G transfer characteristic curves of TiN/HfO_2 p-MOSFETs before and after PBS stress. The inset shows normalized C_{GB}-V_G curve before and after stress and corresponding energy band diagram for stress condition.

after PBS. According to experimental data, the window size seems to be invariant after PBS (red triangle). This behavior illustrates that stress condition did not result in additional bulk traps in high-k layer. However, charge pumping current (I_{CP}), which is another method to examine $N_{it,\ Si/SiO2}$ has an inconsistent result with SS. Figure 2 shows the I_{CP} shift for TiN/HfO_2 p-MOSFETs under PBS and the SS degradation is also shown for comparison. The gate pulse frequency (f) with 1 MHz is selected as I_{CP} was measured. It can be seen that the shift of I_{CP} is more significant than SS. According to the previous, I_{CP} measurement with high frequency (<1 MHz) is difficult to examine the deep defects in high-k bulk due to insufficient charging time. The measurement condition of I_{CP} with f = 1 MHz we selected is mainly bounded to detect interfacial defects, instead of deep bulk traps.[14,15] And then, C_{GB} has shown that there are not additional stress-induced deep defects in high-k layer as shown in the inset of Fig. 1. Accordingly, I_{CP} signal must reflect the defects located at somewhere. Based on those results, we would like to propose that interfacial defects could be generated under PBS located at HfO_2/SiO_2 interface ($N_{it,\ SiO2/HfO2}$). Due to the buffer SiO_2 layer is ~10 Å, the pumping carriers come from source and drain (S/D) have a probability to tunnel buffer oxide to approach HfO_2/SiO_2 interface as I_{CP} was measured. Therefore, $N_{it,\ SiO2/HfO2}$ could be detected by I_{CP} with 1 MHz. To illustrate by energy diagram, the electrons could tunnel from conduction band (ECB) into high-k layer, then gaining potential energy to impact interface of HfO_2/SiO_2, generating non-recovery broken bonds near that. According to continuity boundary conditions and the property of direct tunneling, we estimate the depth carriers could reach under stress voltage roughly as shown in the inset of Fig. 2. The result demonstrates that the stress condition can make carriers cross through ~14 Å for SiO_2 dielectric layer under direct tunneling mechanism, showing the consistency of assumption we mentioned. Since HfO_2/SiO_2 interface owns more incomplete or weak bonds between high-k and buffer oxide, the stress condition could induce more additional $N_{it,\ SiO2/HfO2}$, instead of $N_{it,\ Si/SiO2}$. In order to verify the impact-induced $N_{it,\ SiO2/HfO2}$ under PBS, we introduce AC voltage into experiment. Under AC stress, $N_{it,\ SiO2/HfO2}$ should be degraded seriously as well as the amount of $N_{it,\ SiO2/HfO2}$ could be increased as stress frequency increases. The stress condition was fixed $V_G = 2V + V_{FB}$ for frequency range of 1 kHz~1 MHz to assure the corresponding result. Figure 3 shows the SS and I_{CP} degradation for TiN/HfO_2 p-MOSFETs under PBS with different frequencies. Obviously, the I_{CP} degradation becomes more significant as frequency increases, but SS degradation seems to be invariant regardless of modulating frequencies.

This is because under AC stress, carrier could be accelerated and released repeatedly to enhance the probability of collision at HfO_2/SiO_2 interface, and the reduction of stress electric field due to interfacial ($N_{it,\ SiO2/HfO2}$) trapping is insignificant than that under DC stress. Figure 4 shows I_G measurement by single pulse with period width (PW) 1 μs (0.5 MHz). It can be found that the corresponding gate current forms a rectangular wave with 1.3 μA. To compare gate current with the DC measurement as shown in the inset of Fig. 4, it shows a consistent value at gate voltage = 1.6 V, proving that electrons can transport from substrate to gate

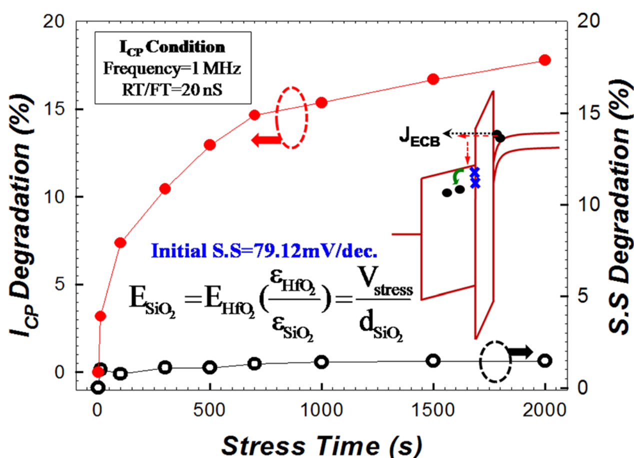

FIG. 2. The PBS-induced I_{CP} and SS degradation for TiN/HfO_2 p-MOSFETs. The inset shows the equation for partial voltage for SiO_2 and initial SS value.

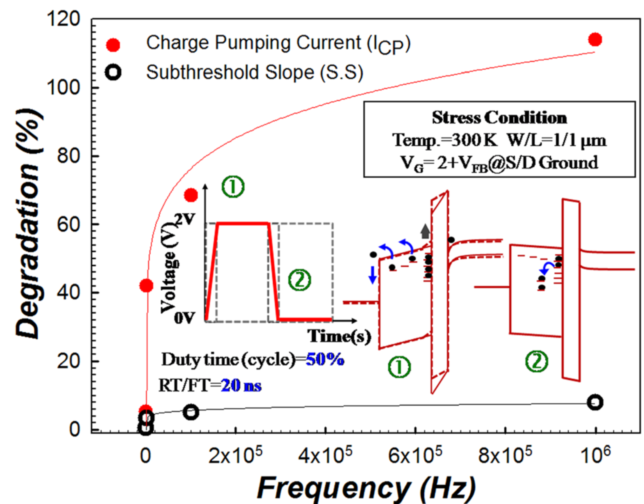

FIG. 3. The PBS-induced I_{CP} and SS degradation for TiN/HfO_2 p-MOSFETs were plotted as a function of AC stress frequency ranging of 0 Hz, 1 kHz, 100 kHz, and 1 MHz. The inset shows the corresponding energy band diagram for AC and DC stress condition.

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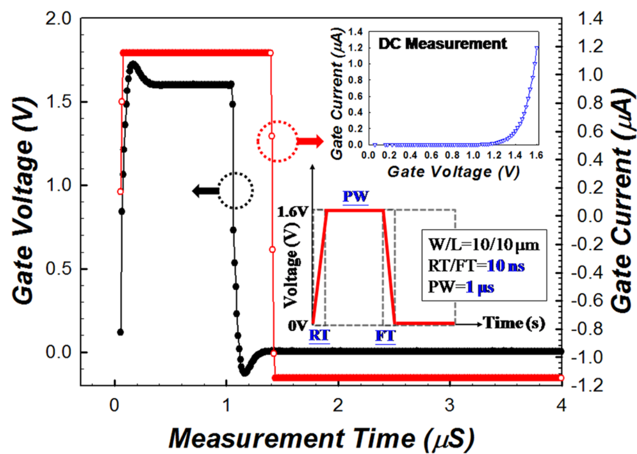

FIG. 4. I_G-V_G pulse characteristic curves of TiN/HfO_2 p-MOSFETs. The inset shows the pulse configuration and I_G-V_G characteristic curves under DC measurement.

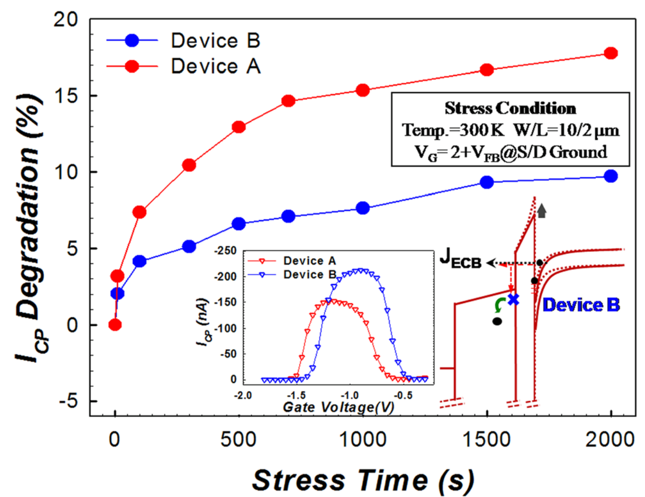

FIG. 5. The PBS-induced I_{CP} and SS degradation for TiN/HfO_2 p-MOSFETs with different SiO_2/Si N_{it} under PBS (devices A and B). The inset shows the corresponding energy band diagram for device B under stress and the I_{CP} curve versus V_G before stress with measurement condition f = 5 MHz.

under AC voltage, and without current decrease. Further, showing that impact ionization under AC stress is possible.

In detail, electrons can transport continuously from E_C to gate dielectric and result in electron trapping. After that, electron could be caught by $N_{it,\ SiO2/HfO2}$, influencing in the energy band near SiO_2 as shown in the peak voltage (+2V) in inset of Fig. 3. Due to transport continuously, interfacial electron trapping ($N_{it,\ SiO2/HfO2}$) could occur constantly, even though electric field makes electrons tends toward gate by Poole-Frenkel emission. However, there is a transform of trapping behavior from interfacial states to deep states for AC condition, since AC stress exhibits peak (+2V) and base voltage (0V). For peak voltage, the behavior on device is identical to DC condition. As application of stress voltage goes through base voltage, trapped electrons in $N_{it,\ SiO2/HfO2}$ have sufficient time to enter deep traps as shown in the inset of Fig. 3. During long time term, reduction of electric field for DC stress condition is more significant than that for AC.[10] Thus, significant degradation should be under AC stress. Additionally, due to possible conduction of electron, worse degradation occurs under high frequency, meaning more amount of pulse induces significant impact ionization. To combine those two causes, I_{CP} under AC stress shows more obvious degradation than that under DC. Besides, since the direct tunneling mechanism does not influence channel interface, thereby SS shows an insignificant degradation under AC PBS. Furthermore, we also compare the degradation mechanism of I_{CP} under PBS for TiN/HfO_2 p-MOSFETs with more pre-existing $N_{it,\ Si/SiO2}$ (device B) as shown in Figure 5. It could be seen that I_{CP} decay curve of device B is more insignificant than that of device A under PBS, indicating that device B has less pre-$N_{it,\ Si/SiO2}$. However, stress condition V_G is given a correction term to achieve identical stress field, therefore the result should be consistent. But the experimental data are not consistent with this assumption. According to that, the stress electric field for device B is lower than device A is suggested. Clearly to explain, device B has a field screen by pre-$N_{it,\ Si/SiO2}$ to decrease stress electric field. As electrons are accelerated toward gate by stress electric field, pre-$N_{it,\ Si/SiO2}$ could trap carriers randomly, reducing stress electric field as shown in the inset of Fig. 5. Because of that, it can results in insignificant impact ionization, also leading less $N_{it,\ SiO2/HfO2}$ in device B.

This Letter investigates the degradation of TiN/HfO_2 p-MOSFETs under off-state stress. Clearly, electron trapping behavior dominates the characteristic of device, including positive V_{th} shift, decrease in I_D but without SS. However, I_{CP} measurement shows an inconsistent result with SS, and we believe that the signal reflect the defect generation at HfO_2/SiO_2 due to impact ionization. According to simple estimation, carriers can result impact near HfO_2/SiO_2 interface. And we found that I_{CP} degradation increases as frequency of AC voltage increases. This is because increase probability of collision at HfO_2/SiO_2 interface, and then the behavior of electric field lowering is insignificant. Therefore, the degradation increases with frequency increases, supporting the model we proposed. Further, the influence of pre-existing $N_{it,\ SiO2/HfO2}$ under PBS was discussed. The pre-$N_{it,\ Si/SiO2}$ can screen the stress field to reduce degradations of device due to interfacial charge trapping.

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