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Silicon-Germanium Structure in Surrounding-Gate Strained Silicon Nanowire Field Effect Transistors

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Abstract. In this paper we numerically examine the electrical characteristics of surrounding-gate strained silicon nanowire field effect transistors (FETs) by changing the radius (R_{SiGe}) of silicon-germanium (SiGe) wire. Due to the higher electron mobility, the n-type FETs with strained silicon channel films do enhance driving capability (∼8% increment on the drain current) in comparison with the pure Si one. The leakage current and transfer characteristics, the threshold-voltage (V_t), the drain induced barrier height lowering (DIBL), and the gate capacitance (C_G) are estimated with respect to different gate length (L_G), gate bias (V_G), and R_{SiGe}. For short channel effects, such as V_t roll-off and DIBL, the surrounding-gate strained silicon nanowire FET sustains similar characteristics with the pure Si one.

Keywords: strained silicon, nanowire FET, surrounding-gate, drain induced barrier height lowering, threshold-voltage roll-off, gate capacitance, simulation

1. Introduction

Strained silicon (Si) field effect transistors (FETs) have recently been proposed [1–10]. Their driving capability is superior to that of the pure Si-based FETs. Compared with the pure Si-based FET, the strained FET has a slightly higher leakage current due to the silicon-germanium (SiGe) channel film has a lower bandgap. To suppress the leakage current, double-gate (DG) strained Si FETs have been proposed. They have better transport characteristics and improved short channel effects (SCEs) than that of single gate (SG) strained FETs [1–23]. On the other hand, pure Si-based surrounding-gate FET has the best channel controllability and lowest SCEs among different structures of FETs [11–23]. We believe that study on surrounding-gate strained Si FETs can quantitatively provide rich information for diverse applications of nanodevice.

In this paper, the surrounding-gate stained Si nanowire FETs are computationally explored. In terms of several electrical characteristics, we find that the surrounding-gate strained Si nanowire FETs exhibit higher on-state current and maintain almost the same off-state current and SCEs, compared with the surrounding-gate Si nanowire FETs. The radius (R_{SiGe}) of SiGe wire, shown in Fig. 1, does modify the electrical characteristics of surrounding-gate strained Si nanowire FET. However, the surrounding-gate strained

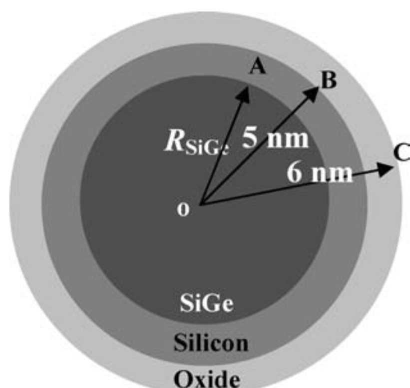

Figure 1. A cross-section view of the surrounding-gate strained Si nanowire FET. The oxide thickness (BC) is 1 nm and the layer radius (oB) of Si film and SiGe is 5 nm.

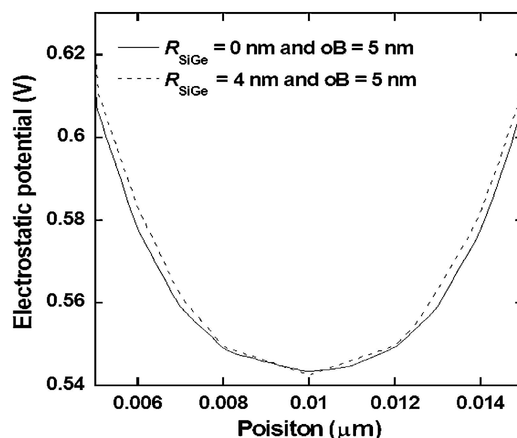

Figure 2. A cross-section view of the electrostatic potentials in both surrounding-gate pure ($R_{\mathrm{SiGe}} = 0$ nm) and strained ($R_{\mathrm{SiGe}} = 4$ nm) Si nanowire FETs, where the gate length $L_G = 5$ nm.

Si nanowire FET sustains the similar on/off current ratio, the threshold voltage roll-off, and SCEs, compared with the characteristics of pure Si one. This study is useful in optimal design of structure for the strained FETs.

The paper is organized as follows. Section 2 state the computational structure. Section 3 describes the simulation results. Section 4 draws conclusions.

2. Device Structure and Simulation

A cross-section view of the simulated surrounding-gate strained Si nanowire FET is shown in Fig. 1. The structure is with a SiGe nanowire covered by a layer of Si. The composition of $\mathrm{Si}_x\mathrm{Ge}_{1-x}$ of the n-type FET is fixed at $x = 0.8$ in our simulation. The dopant of channel and source/drain are 10^{18} and $5 \times 10^{19}\mathrm{cm}^{-3}$, respectively. Mid-gap gate material, TiN is used in the device. The oxide thickness (BC), shown in Fig. 1, is equal to 1 nm and the layer radius (oB) of Si and SiGe is equal to 5 nm. Full quantum mechanical models theoretically are the most accurate ways to study such ultrasmall nanodevices. However, this approach is computationally expensive in the simulation of two- and three-dimensional (2D/3D) devices [14–23]. Phenomenological quantum correction model, a calibrated 3D density-gradient drift-diffusion model, is adopted in this work [14–23]. This approach quantitatively predicts the main tendency of electrical characteristics of the examined devices. Formulation of mobility is an important factor for the strained Si devices [24–25], a strained-dependent mobility is implemented in our simulation.

3. Results and Discussion

Electrostatic potential distribution of the surrounding-gate nanowire FET with $V_{\mathrm{GS}} = 0.5$ V and $V_D = 0.05$ V are almost the same for the strained ($R_{\mathrm{SiGe}} = 4$ nm) and pure Si ($R_{\mathrm{SiGe}} = 0$ nm) samples due to the dielectric constant of both Si and SiGe films are very similar. Cutting from the center of nanowire FET, a cross-sectional plot of the computed potential distribution indicates that there is only slightly difference between them, shown in Fig. 2.

Figure 3 shows the $I_D - V_G$ curves of the surrounding gate strained Si FETs with different R_{SiGe}.

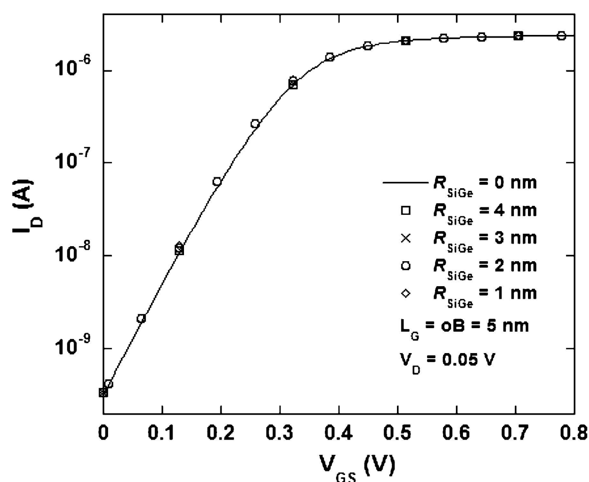

Figure 3. The computed $I_{\mathrm{D}} - V_{\mathrm{GS}}$ curves of the FET with different R_{SiGe}.

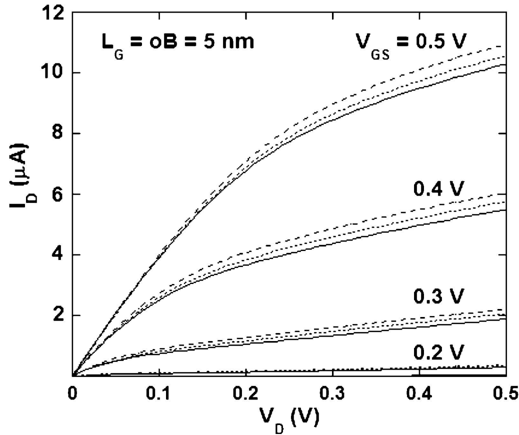

Figure 4. The computed $I_D - V_D$ curves of the FET with different R_{SiGe}.

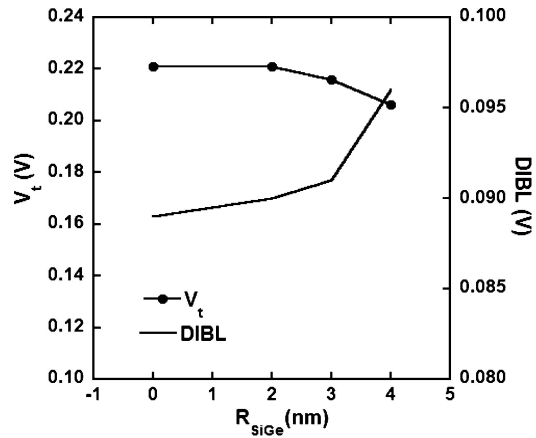

Figure 6. The V_t and DIBL versus R_{SiGe}, respectively.

Results confirm that the difference of V_t and the ratio of on/off current among different testing conditions are small. Strained Si structures do not have very significantly changes on the transfer characteristics for the surrounding-gate nanowire FETs devices. Band gap of SiGe is intrinsically smaller than that of pure Si, but the leakage current does not influenced. This consequence is caused from the fact that the surrounding-gate nanowire FET does have excellent channel controllability. Therefore, suppression of leakage current is enhanced from the band gap narrowing.

Shown in Fig. 4, the surrounding-gate strained Si nanowire FET with $R_{SiGe} = 2$ and 4 nm, respectively, has a higher drain current than that of the pure Si one (solid lines). The larger radius ($R_{SiGe} = 4$ nm) of SiGe implies the higher drain current (dash lines) due to a

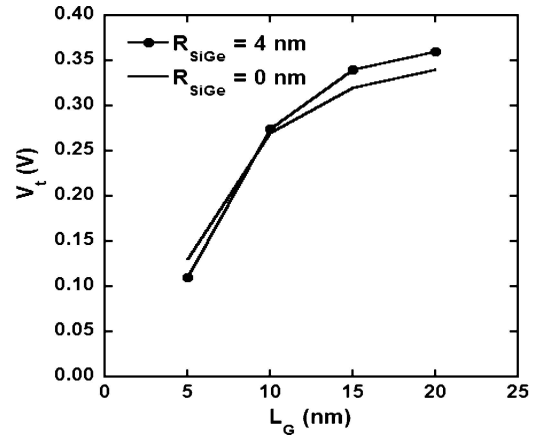

Figure 7. The V_t versus the L_G for the FET with $R_{SiGe} = 0$ and 4 nm.

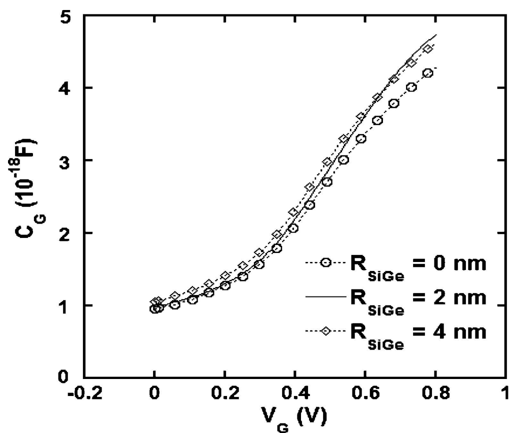

Figure 5. The C_G versus V_{GS} of the FET with different R_{SiGe}.

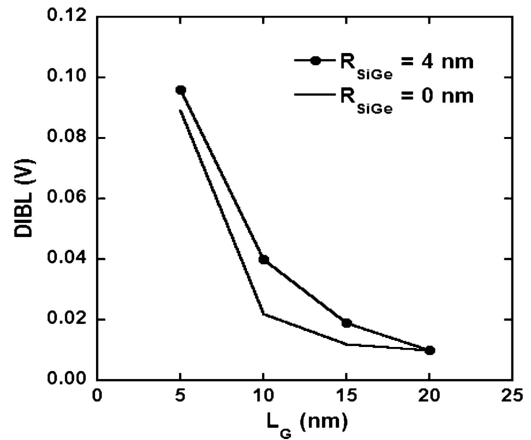

Figure 8. The DIBL versus the L_G for the FET with $R_{SiGe} = 0$ and 4 nm.

higher stress caused from the thinner Si film. We observe that the lower source/drain parasitic resistance caused from the SiGe layer plays another factor for the enhancement of the on-state current. Figure 5 shows the relation of C_G versus V_G. A higher gate to channel capacitance is obtained for the strained Si nanowire FETs.

Figure 6 shows the V_t and DIBL versus R_{SiGe}. It is found that R_{SiGe} only has slight influence on the threshold voltage and the DIBL effect. Similar results can be also found from the threshold voltage roll-off and DIBL effect versus the gate length, shown in Figs. 7 and 8 respectively.

4. Conclusions

We have theoretically investigated the effect of R_{SiGe} on the electrical characteristics of the surrounding-gate strained Si nanowire FET using a 3D device simulation. R_{SiGe} can change the driving current of the surrounding-gate strained Si nanowire FET. When R_{SiGe} is increased, the driving current is increased. However, it does not have significant changes on the transfer characteristics. The surrounding-gate strained Si nanowire FET has larger gate-to-channel capacitance and on-state current. The on/off current ratio, the threshold voltage roll-off, and the SCEs can be sustained similarly with the characteristics of pure Si one. $I_D - V_G$ characteristics relate to the transfer characteristics which dominate the switching capability, the leakage current, and the power consumption. $I_D - V_D$ characteristics have relations with the output characteristic and play the central role in the high frequency performance and application of analog circuits. Simulation results have shown that the surrounding-gate strained Si nanowire FET is attractive to application of nanodevices. We note that for more accurate estimation, effects of the random doping fluctuation should also be included [26–27]. We are currently working on device characteristic optimization with respect to various physical parameters including composition effect of $\mathrm{Si}_x\mathrm{Ge}_{1-x}$.

Acknowledgments

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References

1. B.H. Lee et al., "Performance enhancement on sub-70 nm strained silicon SOI MOSFETs on ultra-thin thermally mixed strained silicon/SiGe on insulator (TM-SGOI) substrate with raised S/D," *Tech. Dig. IEDM* 946 (2002).
2. H.M. Nayfeh et al., "Influence of high channel doping on the inversion layer electron mobility in strained silicon n-MOSFETs," *IEEE Elec. Dev. Lett.*, **24**, 248 (2003).
3. J. Welser et al., "NMOS and PMOS transistors fabricated in strained silicon/relaxed silicon-germanium structures," *Tech. Dig. IEDM* 1000 (1992).
4. M. Rashed et al., "Simulation of electron transport in strained silicon on relaxed $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ substrates," in *Proc. Biennial University/Government/Industry Microelec. Symp.* (1995) vol. 168.
5. J.R. Hwang et al., "Performance of 70 nm strained-silicon CMOS devices," *Dig. Tech. 2003 Symp. VLSI Tech.*, 103 (2003).
6. L. Huang et al., "Electron and hole mobility enhancement in strained SOI by wafer bonding," *IEEE Trans. Elec. Dev.*, **49**, 1566 (2002).
7. C. Fenouillet-Beranger et al., "Requirements for ultra-thin-film devices and new materials for the CMOS roadmap," *Solid-State Elec.*, **48**, 961 (2004).
8. M. Enciso Aguilar et al., "Strained Si HFETs for microwave applications: State-of-the-art and further approaches," *Solid-State Elec.*, **48**, 1443 (2004).
9. F.-L. Yang et al., "Strained FIP-SOI (finFET/FD/PD-SOI) for sub-65 nm CMOS scaling," in *Dig. Tech. 2003 Symp. VLSI Tech.* (2003) p. 137.
10. K. Rim et al., "Fabrication and analysis of deep submicron strained-Si n-MOSFET's," *IEEE Trans. Elec. Dev.*, **47**, 1406 (2000).
11. F.-L. Yang et al., "25 nm CMOS Omega FETs," *Tech. Dig. IEDM*, 255 (2002).
12. H. Wakabayashi et al., "Sub-10-nm planar-bulk-CMOS devices using lateral junction control," *Tech. Dig. IEDM* S20P7 (2003).
13. S.N. Balaban et al., "Quantum transport in a cylindrical sub-0.1 μm silicon-based MOSFET," *Solid-State Elec.*, **46**, 435 (2002).
14. R. Venugopal et al., "Simulating quantum transport in nanoscale transistors: Real versus mode-space approaches," *J. App. Phys.*, **92**, 3730 (2002).
15. J. Wang et al., "Does source-to-drain tunneling limit the ultimate scaling of MOSFETs?," *Tech. Dig. IEDM*, 707 (2002).
16. A. Svizhenko et al., "Role of scattering in nanotransistors," *IEEE Trans. Elec. Dev.*, **50**, 1459 (2003).
17. H. Kawaura et al., "Observation of source-to-drain direct tunneling current in 8 nm gate electrically variable shallow junction metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, **76**, 3810 (2000).
18. A. Schenk et al., "2D Analysis of source-to-drain tunneling in decananometer MOSFETs with the density-gradient model," in

Tech. Proc. Int. Conf. Modeling and Simulation of Microsystems 552 (2002).
19. A. Asenov et al., "The use of quantum potentials for confinement in semiconductor devices," in *Tech. Proc. Int. Conf. Modeling and Simulation of Microsystems* 490 (2002).
20. Y. Li et al., "A Practical implementation of parallel dynamic load balancing for adaptive computing in VLSI device simulation," *Engineering with Computers*, **18**, 124 (2002).
21. Y. Li et al., "A two-dimensional quantum transport simulation of nanoscale double-gate MOSFETs using parallel adaptive technique," *IEICE Trans. Information and Systems*, **E87-D**, 1751 (2004).
22. T.-W. Tang et al., "Discretization scheme for the density-gradient equation and effect of boundary conditions," *J. Comput. Elec.*, **1**, 389 (2002).
23. C.-S. Tang et al., "Simulation of electrical characteristics of surrounding- and omega-shaped-gate nanowire FinFETs," *Proc. IEEE Conf. Nanotech*. 281 (2004).
24. K. Matsuda, "Phonon scattering effects on temperature dependence of conductivity in strained silicon," *J. Comput. Elec.*, **1**, 425 (2002).
25. G. Kaiblinger-Grujin et al., "A universal low-field electron mobility model for semiconductor device simulation," in *Tech. Proc. Int. Conf. Modeling and Simulation of Microsystems* 70 (1998).
26. A.R. Brown et al., "Intrinsic fluctuations in sub 10-nm double-gate MOSFETs introduced by discreteness of charge and matter," *IEEE Trans. Nanotech.*, **1**, 195 (2002).
27. A. Asenov et al., "Quantum mechanical and transport aspects of resolving discrete charges in nano-CMOS device simulation," in *Proc. IEEE Conf. Nanotech*. 334 (2004).