Novel 2-Bit/Cell Wrapped-Select-Gate SONOS TFT Memory Using Source-Side Injection for NOR-Type Flash Array

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***Abstract*—This letter is the first to successfully demonstrate the 2-bit/cell wrapped-selected-gate (WSG) SONOS thin-film transistor (TFT) memory using source-side injection (SSI). Because of the higher programming efficiency of SSI, a memory window of approximately 3 V can be easily achieved in 10 μs and 30 ms for the program and erase modes, respectively. In addition, we performed an excellent 2-bit/cell distinguish margin for 3-V memory window in WSG-SONOS TFT memory. The optimal reliability of the endurance and data retention tests can be executed by adjusting the applied voltage appropriately.**

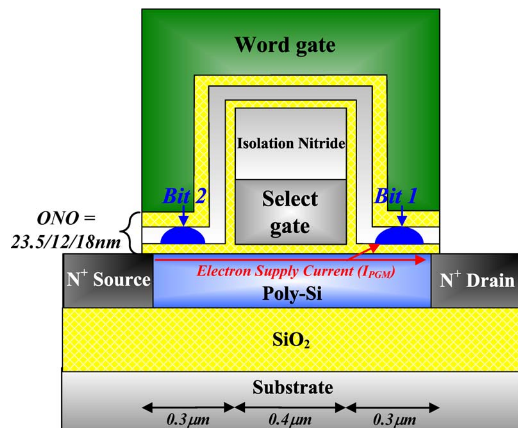
***Index Terms*—Source-side injection (SSI), thin-film transistor memory, two-bit/cell, wrapped-selected-gate (WSG)-SONOS.**

I. Introduction

THE advantage of polycrystalline silicon (poly-Si) thin-film transistors (TFTs) is that it can integrate additional functionality into system-on-glass (SOG) and system-on-chip (SOC) [1], including driver electronics, peripheral circuits, and memory devices. A poly-Si memory device with high performance on a multifunction system plays a vital role because embedded memory is used to assist the logic function and microcontroller. In addition, the 2-bit/cell application of SONOS TFT memory device is also a widely used method to effectively increase 2× density without increasing the device area [2]. This letter presents a TFT nonvolatile memory device using a wrapped-select-gate (WSG) structure to accomplish the 2-bit/cell with high performance requirements of the embedded memory device. This letter is also the first to verify that source-side injection (SSI) can be achieved in a WSG-SONOS TFT memory device [3].

II. Experimental

Fig. 1 shows the cross section of WSG-SONOS TFT memory with 2-bit/cell operation. It shows that the WSG gate is wrapped around isolated nitride and oxide to achieve a physically separated 2-bit and SSI program method in the proposed device. First, the device was fabricated on a silicon wafer with 5500-Å wet oxide, which is used to simulate glass substrate. Subsequently, a 500-Å amorphous Si (a-Si) film for the channel region was deposited at 500 °C by low-pressure chemical vapor deposition. After patterning, the deposited a-Si films were crystallized by solid-phase crystallization at 600 °C for 24 h. To form the embedded assistant gate, we deposited 180-Å TEOS oxide, 1000-Å *in situ* N^+ poly-Si layer, and 1000-Å isolated nitride, which is used to isolate select the gate and word gate. After WSG patterning, the thin-film thickness of the tunnel oxide, nitride trapping layer, and blocking oxide (ONO) stacks was deposited by horizontal furnace with 180, 120, and 235 Å, respectively. Followed by the 2000-Å word gate poly-Si deposition and pattern, the gate and source/drain regions were formed by the self-alignment implant technique. After source/drain activation, passivation oxide and back-end processes were performed. The WSG-SONOS TFT memory channel length and width were 1 and 10 μm, respectively. The length of the WSG was 0.4 μm. The threshold voltage of the device was defined by the constant current method (10^{-7} A) in the reverse read mode.



WSG-SONOS TFT Memory (2 Bit/Cell)						
Bit 1 operation	Mode	V_{WL}	V_D	V_S	V_{SG}
Program	SSI	18V	8V	0V	0.6V
Erase	BTBTHH	-8V	18V	0V	0V
Read	Reverse	0~8V	0V	6V	4V

Fig. 1. Cross section with SSI operation scheme under 2-bit/cell mode of WSG-SONOS TFT memory.

Manuscript received February 12, 2012; accepted March 19, 2012. Date of publication May 3, 2012; date of current version May 18, 2012. This work was supported in part by the National Science Council of Taiwan under Contract NSC-95-2221-E-009-272 and in part by MOE-ATU. The review of this letter was arranged by Editor M. Jurczak.

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Digital Object Identifier 10.1109/LED.2012.2192090

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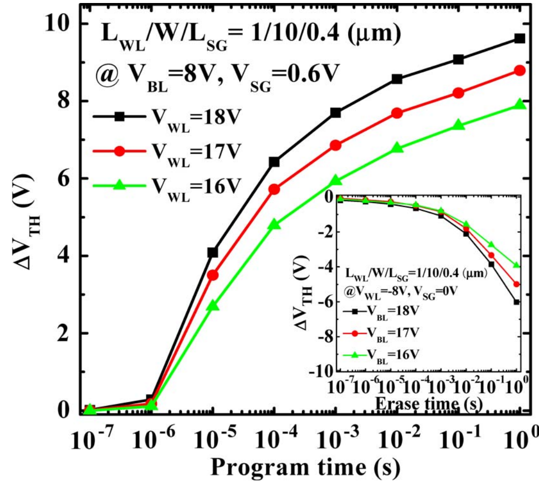


Fig. 2. High program speed of 2-bit/cell WSG-SONOS TFT memory in SSI mode. The inset figure shows erase speed. In our proposed method, V_{TH} of WSG-SONOS TFT memory is extracted by the constant current method (0.1 μA) with reverse read mode.

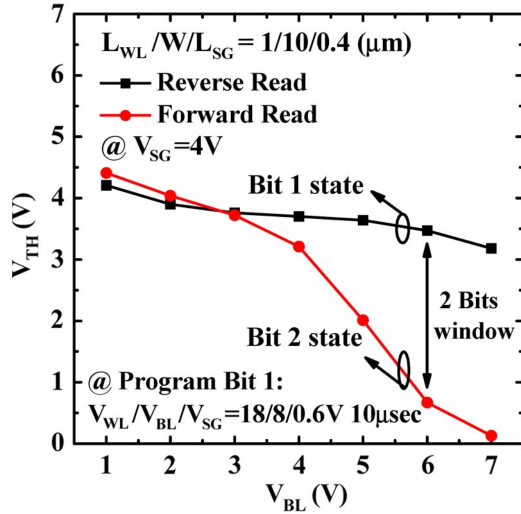


Fig. 3. SSI operation of 2-bit/cell characteristics of WSG-SONOS TFT memory under forward read and reverse read, respectively.

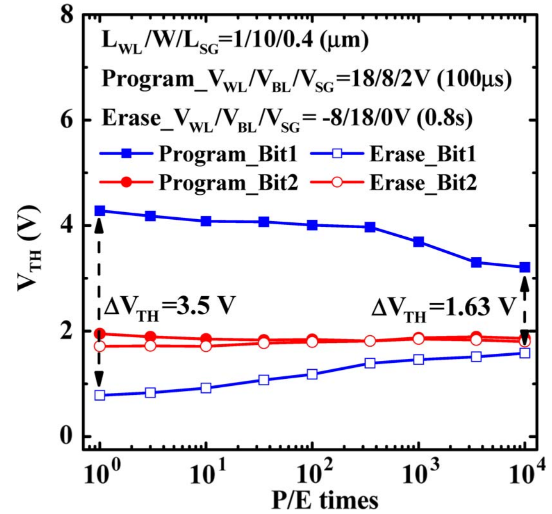
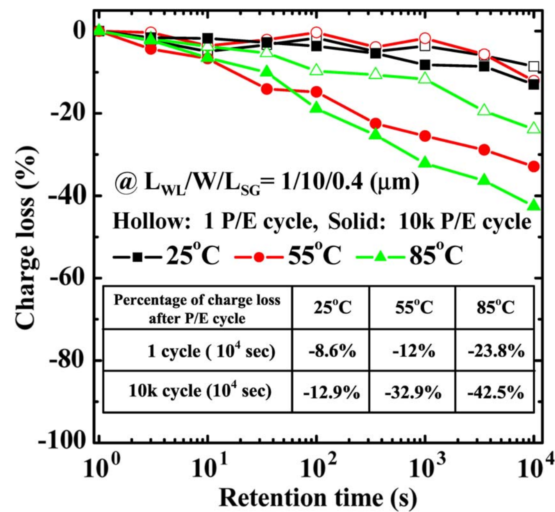


Fig. 4. Endurance characteristics with 2-bit/cell operation of WSG-SONOS TFT memory, including bit 1 and bit 2, and cycling up to $10^4\times$. The memory window of bit 1 can still maintain at 1.6 V even after 10^4 cycling stress, almost no variation at bit 2.



Percentage of charge loss after P/E cycle	25°C	55°C	85°C
1 cycle (10^4 sec)	-8.6%	-12%	-23.8%
10k cycle (10^4 sec)	-12.9%	-32.9%	-42.5%

Fig. 5. Data retention characteristics with SSI operation under different baking temperatures from 25 °C to 85 °C, respectively. The cells are uncycled and 10^4 cycled, respectively.

III. Results and Discussions

SSI was used to accomplish TFT 2-bit/cell operation in the program mode. The programming characteristic of the WSG-SONOS TFT memory is shown in Fig. 2. A $\Delta V_{\mathrm{TH}} = 3$ V can be achieved by $V_{\mathrm{WL}} = 18$ V, $V_{\mathrm{BL}} = 8$ V, and $V_{\mathrm{SG}} = 0.6$ V in 10 μs. In addition, the higher word gate voltage can also improve programming speed because of its higher electric field in the neutral gap region [4]. It indicates that the charge density of the inversion layer may be formed higher to pass V_{BL} to stride across the neutral region easily. The inset figure also shows the erasing characteristic dependence on V_{BL}. We used band-to-band-tunneling hot holes to recombine the electrons stored in the nitride trapping layer. $\Delta V_{\mathrm{TH}} = 3$ V can be also easily achieved by applying $V_{\mathrm{WL}} = -8$ V, $V_{\mathrm{BL}} = 18$ V, and $V_{\mathrm{SG}} = 0$ V in 30 ms.

Fig. 3 shows the 2-bit/cell operation characteristics with a different V_{BL}. The reverse read was widely used in 2-bit/cell operation to electrically separate the 2 bit. The charge screen effect can be gradually increased in conjunction with the bit-line voltage because of reverse bias application on p-n junction (substrate to source/drain). The result indicates that our WSG-SONOS TFT accomplished 2-bit/cell operation in 10 μs with 3-V difference memory windows.

Fig. 4 shows the endurance characteristics up to $10^4\times$, including bit 1 and bit 2. The erase state of bit 1 increased with repeated cycling up to $10^4\times$, indicating incomplete erasure [5], or more interfacial state generation in the bottom oxide [6]. Conversely, the program state of bit 1 decreased while increasing the P/E cycling test. The memory window maintained more than 1.6 V even after 10^4 cycles. In addition, the program and erase states of bit 2 exhibited almost no variation even after 10^4 cycling tests of bit 1. This verified that our WSG-SONOS TFT structure exhibited excellent electrical characteristics to separate two physical bits.

Fig. 5 shows the data retention characteristics after 10^4 s with programming state after 10^4 P/E cycles at 25 °C, 55 °C, and 85 °C baking temperatures. The charge loss behavior of the

TABLE I
COMPARISON TABLE OF ADVANCED TFT TECHNOLOGIES INCLUDES TFT AND BULK WSG-SONOS MEMORY DEVICE

TFT Structure	Program mode	Erase mode	Memory window	Charge Lost	Cycle Test
SOHOS Memory Ref. [8]	V_G=12V V_D=12V 1ms	V_G=-10V V_D=10V 10ms	3V 2 bit/cell	43% @ 85°C	~1.87V @10^4 cycles
Nanowire Memory Ref. [9]	V_G=18V 1ms	V_G=-18V 1s	3.5V 1 bit/cell	31.25% @ 85°C	~1.5V @10^6 cycles
SLS Memory Ref. [10]	V_G=18V V_D=12V 10ms	V_G=-8V V_D=20V 10ms	2.22V 1 bit/cell	N/A	N/A
WSG-SONOS (This Paper)	V_G=18V V_D=8V 100μs	V_G=-8V V_D=18V 0.8s	3.5V 2 bit/cell	42.5% @ 85°C	~1.6V @10^4 cycles
Bulk WSG-SONOS Ref. [11]	V_G=9-11V V_D=4V 10μs	V_G=-4V V_D=6V 5ms	1-3V 4 bit/cell	3% @ 85°C	1-3V @10^4 cycles

storage layer of WSG-SONOS TFT was considerable after 10^4 cycling test with 85 °C baking temperature. The higher baking temperature can assist the electrons to overcome the activation energy to discharge from the nitride trapping layer [7]. The interface state and tunneling oxide traps can also help discharge the electrons by the trap-assist tunneling mechanism, particularly for the devices after 10^4 P/E cycles stress [6]. The inset table in Fig. 5 shows the percentage of charge loss with various baking temperatures under unity P/E cycle and 10^4 P/E cycles after 10^4 s. It indicates that the quality of tunneling/blocking oxide plays a vital role in reliability issues of the WSG-SONOS TFT memory device for providing optimal stress immunity. The reliability of the WSG-SONOS TFT memory device can be improved once the strength of the tunneling/blocking oxide or embedded silicon dots are effectively increased in the nitride trapping layer. Table I shows the comparison to the other advanced TFT memory technologies, i.e., bulk and TFT WSG-SONOS memory devices [8]–[11]. It verifies that this WSG-SONOS TFT memory with good electrical characteristic has a high potential for embedded memory application on SOG.

IV. CONCLUSION

We have first demonstrated a 2-bit/cell operation WSG-SONOS TFT memory device using SSI and band-to-band-tunnel hot-hole erasing. The fast program/erase speed can be achieved in 10 μs/30 ms for a memory window that is equal to 3 V. Moreover, the memory window can maintain more than 1.6 V even after 10^4 P/E endurance tests. In addition, the percentage of charge loss was lower than 13% even after 10^4 s with 10^4 P/E endurance tests at 25 °C. Consequently, the WSG-SONOS TFT memory device is a potential candidate for future SOG or SOC systems because of its excellent performance and reliability.

ACKNOWLEDGMENT

The authors would like to thank the National Nano Device Laboratories for procedural support, as well as the Nano Facility Center of National Chiao Tung University.

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