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Temperature dependence on the contact size of GeSbTe films for phase change memories

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Abstract In this study, a three-dimensional electro-thermal time-domain simulation is developed for dynamic thermal analysis of Phase change memories (PCMs). The geometry effects of the GeSbTe (GST) materials and the TiN heater are explored through a series of numerical examinations. It is found that the contact size of the GST significantly alters the maximum temperature of the PCMs, compared with the height of the GST films. The heater's aspect ratio also dominates the maximum temperature of the GST material, and the effect of the heater's thickness on the temperature is more evident than its height. One conformal bi-layer GST structure with different electric and thermal conductivities on the GST layers is examined for different applied currents to extract the curve of resistances versus applied currents.

Keywords Phase change memories · GeSbTe material · Geometry effects · Temperature · Numerical simulation

1 Introduction

Phase change memories (PCMs) [1–4] are promising in solid-state memory technologies; particularly in substitution for static random access memory and flash memory. PCM stores data by a thermal-induced phase transition between conductive polycrystalline (set) and resistive amorphous (reset) states, in thin film of chalcogenide materials, such as GeSbTe (GST) alloy. In memory operation, cell read out is performed at low bias. Programming requires instead a relatively large current, to heat the GST alloy, which is leading to a local phase change. Determination of the maximum temperature of the GST material is crucial in the PCM technology.

In this study, a three-dimensional (3D) electro-thermal time-domain simulation is conducted for dynamic thermal analysis of PCMs. The contact size of the GST significantly alters the maximum temperature of the PCM, compared with the height of the GST films. For the effects of heater's aspect ratio, it is found that the effect of the heater's thickness on the temperature is more evident than its height. The effect of doping-dependent electrical conductivity of the GST in crystalline state on the temperature profile of the PCM cell is also discussed [5, 6]. One conformal bi-layer GST structure with different electric and thermal conductivities on the GST layers is examined for different applied currents to extract the curve of resistances versus applied currents. This paper is organized as follows. In Sect. 2, we state the model to be solved, where the simulation procedure is included. In Sect. 3, we show the results and discussion. Finally, we draw the conclusions and suggest future work.

2 The electro-thermal simulation model

The temperature profile of the GST is estimated by the time-evolutionary electro-thermal simulation [2, 3]. The computational model consists of a set of coupled Laplace and heat diffusion equations

$$\nabla(\sigma \cdot \nabla\phi) = 0, \quad (1)$$

$$\rho C_p \frac{\partial T}{\partial t} - K \cdot \nabla^2 T = \sigma |E|^2, \quad (2)$$

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where σ is the electrical conductivity, ϕ is the electrical potential, and ρ is the density. K and C_p correspond to the thermal conductivity and the specific heat, respectively. Incorporating proper initial and boundary conditions, finite element solution of these partial differential equations determines the potential and resulting temperature throughout the storage medium. The adopted physical parameters are summarized in Table 1 [1].

Figure 1 illustrates the computational flowchart to solve the coupled electro-thermal model. First the explored structures are established for the 3D simulation, and apply the finite element method to do the domain descretization [7, 8]. Then the Laplace equation is solved for the potential $\phi(i)$ at the time-step i. In the next step, the calculated potential distribution is used in the heat diffusion equation to solve the temperature distribution of the structure. After that, go back to solve the Laplace equation for next $(i+1)$ time step. If the final time step is achieved, the results will be output.

Table 1 A list of the thermal and electrical parameters in the thermal simulation of phase change memory

Material	Electric conductivity (1/Ωm)	Thermal conductivity (W/Km)	Specific heat (J/Km3)
GST (crystalline)	FCC: 2770 HCP: 1e5	FCC: 0.5 HCP: 1.2	1.25e6
GST (amorphous)	3	0.2	1.25e6
TiN heater	112000	2.47	0.7e6
Oxide	–	1.4	3.1e6

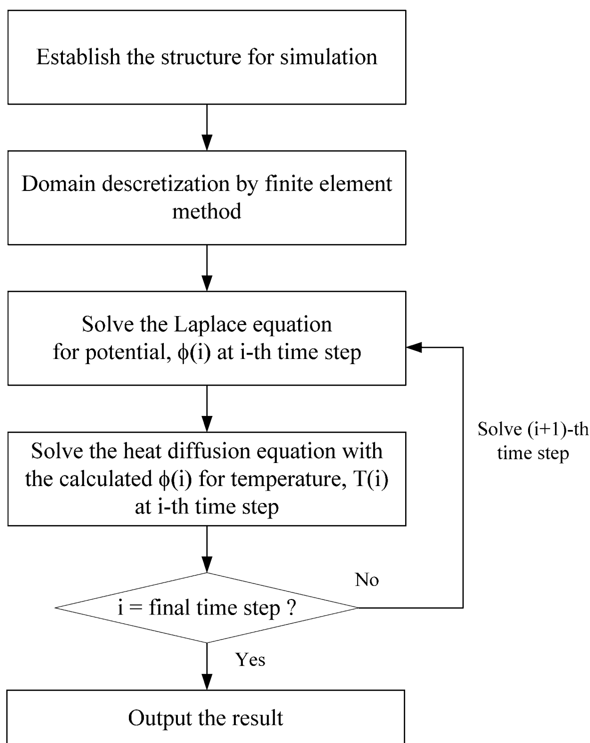

Fig. 1 A flowchart for solving the coupled Electro-Thermal Model

3 Results and discussion

Figure 2 is the structure of the explored PCM cell. Two different structures are examined in this work. The GST alloy is contacted with a TiN heater, and it has two GST layers for both structures, as shown in Fig. 2. In the first structure, as shown in Fig. 2(a), all GST layers use the setting of FCC phase. We examined the geometry effects of the GST and heater by the first PCM structure. The second structure in the Fig. 2(b) is a conformal bi-layer GST structure with a HCP phase in the top GST layer and a FCC phase in the bottom GST layer [9, 10]. The FCC and HCP are two different phases [9] with different electric and thermal conductivities for the GST materials. The second structure is used to simulate the curves of resistance versus applied currents (R-I curves). Based on the simulated R-I curves, we can accurately extract the applied current to reset the PCMs.

The simulation assumes that the PCM cell was in crystalline state and the constant current of 100 µA was applied between the top contact (CT2) and substrate contact (CT1) to heat the cell. Figure 3 shows the temperature profile of the cells with contact size between the two GST layers after a 50 ns pulse. Enlarging the contact size between the top and bottom GST films, shown in Fig. 3, the maximum temperature decreases when the contact size is increased from 20 nm to 40 nm. Figure 4 shows the temperature profiles for different GST's electrical conductivity, $\sigma = 1e3$ and 1e5 (1/Ωm). With the same constant current pulse, the high GST's electrical conductivity reduces the maximum temperature. It implies that a larger applied current is required to heat the GST for the higher electrical conductivity. Table 2 summarizes maximum temperature of the cell with respect to different GST geometry and electrical conductivity. We notice that

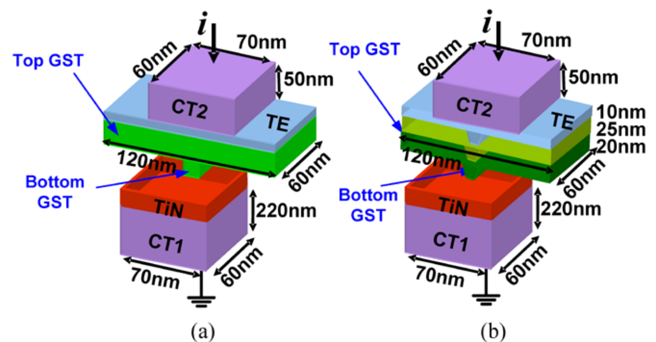

Fig. 2 A three-dimensional plot of the explored phase change memory cell. Effect of GST films' size on the temperature variation is studied. Two different structures are studied in this work, and the structure in (**b**) is a conformal bi-layer GST structure

the effect of the GST's contact size on the maximum temperature is larger than the effect of the GST's height (about 200 K variation). Figure 5 shows the maximum temperature versus time with different heater height and thickness. We can find that increase of the heater thickness and decrease of its height lead to a lower temperature. The effect of the heater's thickness on the maximum temperature is larger than the effect of the heater's height. In our 3D simulation, when increasing 10 nm for the heater thickness, the maximum temperature of GST is reduced from 1719 K to 1263 K. The maximum temperature difference is around 456 K. However, when we increase the heater's height from 50 nm to 60 nm, the difference of the maximum temperature is around 20 K only due to the heater's thickness decides the contact area to GST, which directly affects the heat diffusion from GST material to the heater.

Table 3 summarizes the maximum temperature and the corresponding potential for different applied currents. This examination is performed on the structure shown in the Fig. 2(b), and Fig. 6 shows the simulated resistances for different applied currents. Simulation results show the ratio of reset to set state resistance is ≈800. The set and reset resistances are about 12 k and 10 MΩ, respectively. From the R-I curve in Fig. 6, we need to apply current larger than 150 μA to entirely reset the PCMs to the amorphous statues.

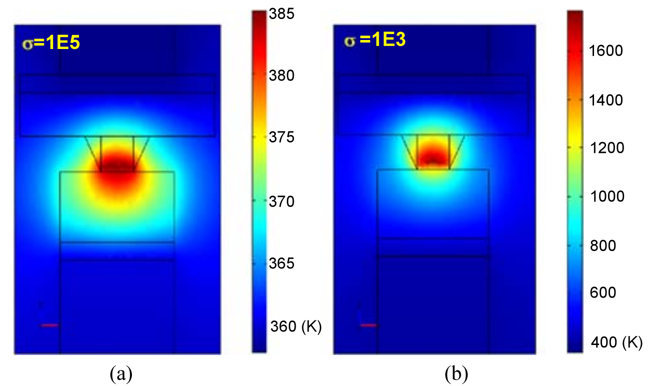

Fig. 4 Cross-sectional temperature profile of the cell after the 100 μA, 50 ns pulse, where the GST's electrical conductivities are (**a**) 1e5 and (**b**) 1e3 (1/Ωm), respectively. A 2-order magnitude variation on the GST's electrical conductivity results in 5-times temperature deviation

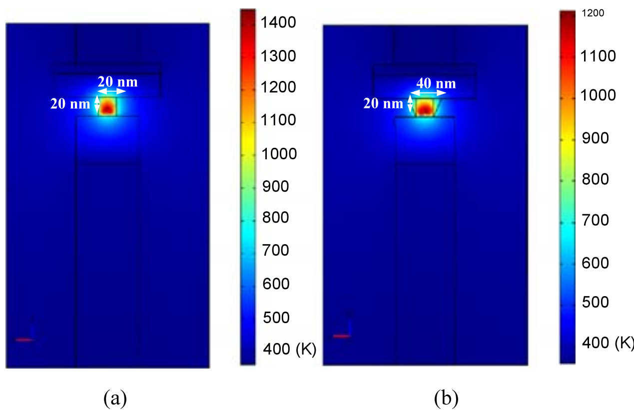

Fig. 3 Cross-sectional temperature profile of the explored cell after the 100 μA, 50 ns pulse. The contact size between the two GST layers are (**a**) 20 nm and (**b**) 40 nm

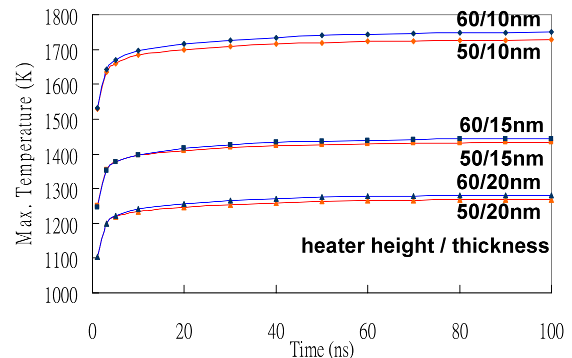

Fig. 5 The maximum temperature versus time with different heater's height and thickness

Table 2 A summarized maximum temperature of the cell with respect to different GST geometry and electrical conductivity

σ (1/Ωm)	2770						1e3	2e3	1e4	1e5
Heater height (nm)	50		50		50		50			
Heater thickness (nm)	10		10		10		10			
Top GST height (nm)	25		25		25	50	25			
Bottom GST height (nm)	20	40	20	40	40		20			
GST contact size (nm)	20		40		20		40			
Max. Temperature (K)	1448	1514	1214	1340	1514	1530	1767	1068	510	385

Table 3 A list of the maximum temperature and the corresponding potential for different applied current with the explored structure, as shown in Fig. 2(b)

Applied current (50 ns)	Max. temperature (K)	Potential (V)
50 (μA)	601	0.601
75 (μA)	905	0.902
100 (μA)	1330	1.203
150 (μA)	2546	1.804
200 (μA)	4248	2.405

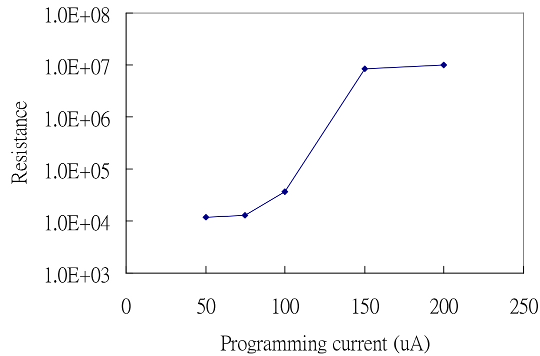

Fig. 6 The calculated resistances versus different applied currents Simulation results show the ratio of reset to set state resistance is ≈800. The set and reset resistances are about 12 k and 10 MΩ, respectively

4 Conclusions

In this work, a thermal analysis for phase change memory has been implemented by performing a 3D electro-thermal coupled simulation. As summarized in Table 2, our preliminary estimation shows that the GST film's geometry and electrical conductivity can modify the distribution of temperature and alter the maximum temperature of GST material. The heater's geometry aspect ratio also modifies the distribution of temperature and, the effect of the heater's thickness is more significant then its height. One conformal bi-layer GST structure is explored to simulate the curve of resistances versus different applied currents. Simulation results show the ratio of reset to set state resistance is ≈800, and we need to apply one current larger than 150 μA for completely transfer the PCMs from the crystalline status to amorphous status.

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