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# A novel technique to fabricate 28 nm p-MOSFETs possessing gate oxide integrity on an embedded SiGe channel without silicon surface passivation

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**Abstract**

A novel technique to create a suspending stacked gate oxide and subsequently to fill in an embedded SiGe channel (ESC) between the gate oxide and the underlying silicon substrate is proposed for the first time to fabricate 28 nm p-metal–oxide–semiconductor field-effect transistors (p-MOSFET). Without Si surface passivation on the ESC, such an ESC structure could achieve a p-FET transconductance ($G_m$) gain of 26% higher and a better $I_{on}$–$I_{off}$ performance gain of 8% than that of conventional strained Si p-FETs with the source/drain (S/D) SiGe. Better S/D resistance ($R_{sd}$) in the resistance versus gate length plot and improved swing slope of the $I_d$–$V_{gs}$ plot indicates higher mobility in the ESC devices. Moreover, the off-state gate current of the ESC structure is also comparable to the conventional ones. From the x-ray photoelectron spectrum analysis, only the Si–O bonding, and no Ge–O bonding at the SiGe/$SiO_2$ interface could account for this superior gate oxide integrity for the ESC and strained Si structure. Therefore, such a novel technique with an ESC structure is very promising for the 28 nm p-MOSFET devices era.

(Some figures may appear in colour only in the online journal)

## 1. Introduction

The last few years have seen the Si/SiGe material system widely integrated into CMOS technology. The 4.2% lattice mismatch between Si and Ge can be used to obtain the strained layer, where electron (in Si under tension) and hole (in SiGe under compression) transport is improved. Epitaxial SiGe in the source/drain (S/D) region for p-field-effect transistor (p-FET) drive current enhancement has been pursued aggressively in scaled CMOS technologies [1, 2]. However, the size of the strained SiGe at source/drain used for p-FET performance improvement is getting reduced because the volume left for this S/D SiGe stressor is getting smaller and smaller for the advanced technology node. Inevitably mobility degradation with gate length scaling has been reported. Widening the S/D volume to shorten the proximity of the S/D SiGe to the gate stack is attracting attention to increase the channel stress for device performance enhancement [3, 4]. However, extension of S/D SiGe to the gate stack also faced limitations in scaled CMOS technologies. Another approach to channel strain engineering is a SiGe channel, which was considered as a promising candidate in nano-p-metal–oxide–semiconductor field-effect transistors (p-MOSFETs) for performance boost-up [5–7]. However, an inevitable epitaxial Si cap layer to provide gate oxide integrity and subsequent thermal budget control to avoid onset of threading dislocations from SiGe layer become the major barriers of technology implementation [8–13]. In this work, we demonstrate a novel embedded SiGe channel (ESC) structure composed of strained SiGe channels without extra Si surface

 

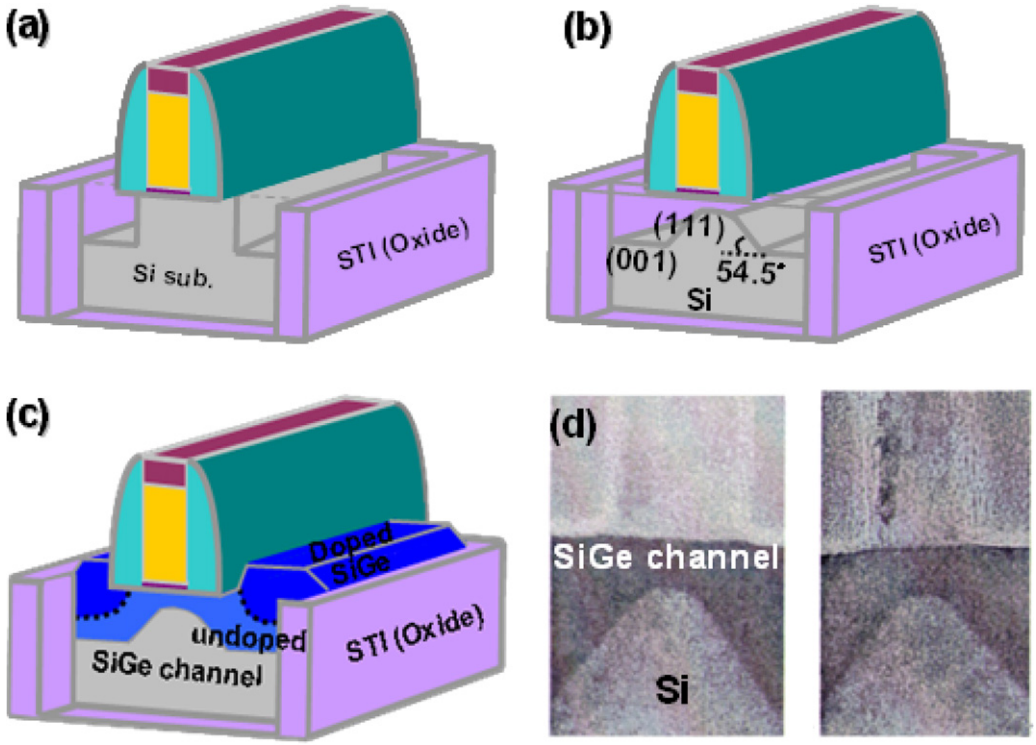


**Figure 1.** A novel technique of etching and deposition process sequence to create a suspending gate stack and to fill the ESC; the TEM picture shows the ESC structure.

passivation to show potentially superior hole mobility and superior gate oxide integrity. It is believed that the ESC structure is a very promising candidate in the nanodevice era with the beautiful essence of low cost and standard p-MOSFET process compatibility.

## 2. Device design and fabrication

A series of p-FETs with shallow trench isolation (STI) and arsenic well implantation to control $V_t$ in the ESC devices, which has a smaller energy gap ($E_g$) than the Si substrate were fabricated on 300 mm [1 1 0]/(0 0 1) Si wafers. After this process, 1.5 nm thick SiON with 10–15% of nitrogen concentration was formed by a rapid thermal process (RTP) and decoupling plasma nitridation (DPN). 30 nm gate length and 15 nm nitride spacer critical dimension (CD) were achieved. A conventional reactive ion etching (RIE) process, named dry etch-1 (figure 1(*a*)), created a recessed region of 60 nm in depth. Subsequently, the samples were put into a reduced pressure chemical vapour deposition (RPCVD) chamber at 700 °C for the novel technique of dry etch, named dry etch-2, which is an *in situ* etch process of $Cl_2$ or HCl gas to etch away silicon along the (1 1 1) plane with 54.5° to create a suspending gate stack (figure 1(*b*)). By the well-designed depth of dry etch-1 of over 50 nm and the crystalline characteristic of dry etch-2, we can perform calculations involving trigonometric functions to obtain a suspending gate stack. An undoped SiGe epitaxial layer (Ge ∼ 40 at%) to fill up the channel and a doped SiGe layer to fill up S/D were deposited at 700 °C without the necessity of a thin Si surface passivation layer in the same RPCVD chamber. The epitaxial SiGe layer was conjointly formed in compressive mode at the channel as well as the lightly doped drain (LDD) and S/D regions (figure 1(*c*)). The arsenic (As) pocket implantation and S/D implantation as well as a spike rapid thermal anneal (RTA) were conducted after the ESC formation. Subsequent processes were carried out to fabricate the 28 nm p-MOSFETs. The transmission electron microscopy (TEM) images of the almost dislocation-free ESC show a good crystalline ESC between the gate oxide and the underlying Si substrate, as shown in figure 1(*d*). The ESC devices are compared with the reference Si p-FETs with S/D strained SiGe.

Figure 2(*a*) shows the design of our ESC by defining the various depths of dry etch-1, $Y$, at 30 nm gate length and 15 nm nitride spacer CD, and then obtaining the corresponding SiGe channel depth, $Z$, which is calculated by the trigonometric functions of the lattice plane (1 1 1) with 54.5° between (0 0 1) planes. Figure 2(*b*) illustrates the profile of the ESC and S/D SiGe region. After *in situ* dry etch-2 to obtain a suspending gate stack, the undoped SiGe channel region was deposited first to form the SiGe channel. The SiGe channel results in a higher hole mobility than the Si channel device. The highly doped SiGe was subsequently deposited in the S/D region and it can lead to a lower S/D resistance and a better device performance. The optimized well implantation and the subsequent LDD and pocket implantation were performed to adjust the $V_t$ in the SiGe channel ECS device.

## 3. Device result

Figures 3 and 4 show the $V_t$ roll-off and $G_m$ improvement on the ESC p-FETs and conventional strained Si p-FETs (S/D SiGe

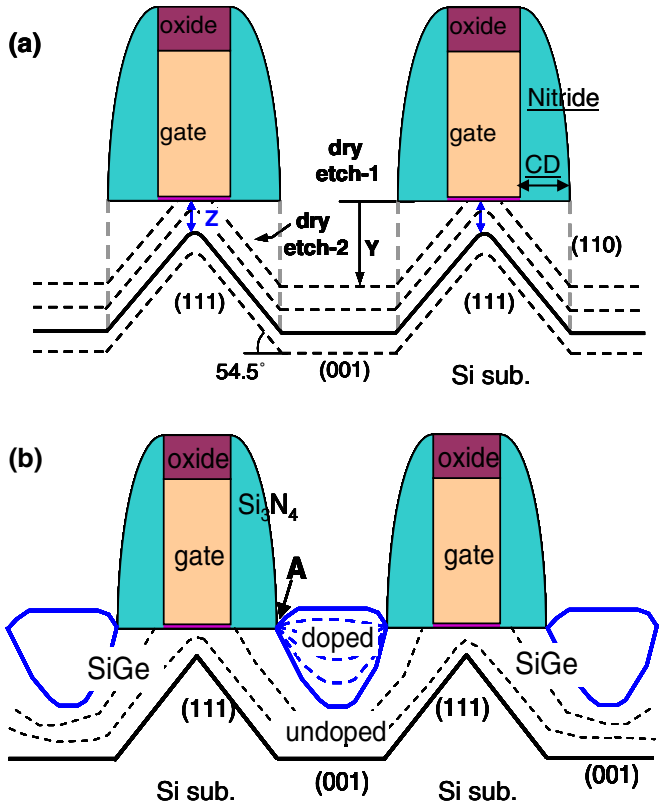


**Figure 2.** (*a*) illustrates the design of the ESC by defining the various depths of dry etch-1, $Y$, then obtaining the corresponding SiGe channel depth, $Z$; (*b*) shows the profile of the ESC and the S/D SiGe region.

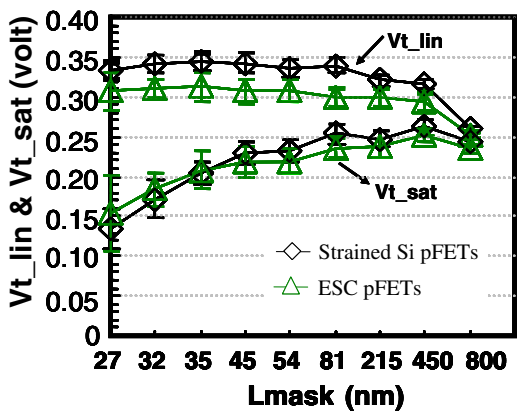


**Figure 3.** ESC device demonstrating $V_{th}$ slightly better than or comparable to that of the conventional strained Si p-FETs with the S/D SiGe devices.

p-FETs), respectively. It has been reported that boron out-diffusion from LDD regions causes the worse short channel control in the conventional strained Si p-FETs. The epitaxial SiGe layer of the ESC structure in the LDD region can retard the out-diffusion of boron and has a better short channel control. The optimized well implantation and As pocket implantation can contribute to the healthy $V_t$ roll-off behaviour and $V_t$ position for the application on current advanced transistors in figure 3. Due to the higher hole mobility in SiGe than in the Si channel, figure 4 demonstrates that the ESC p-FETs show 26%

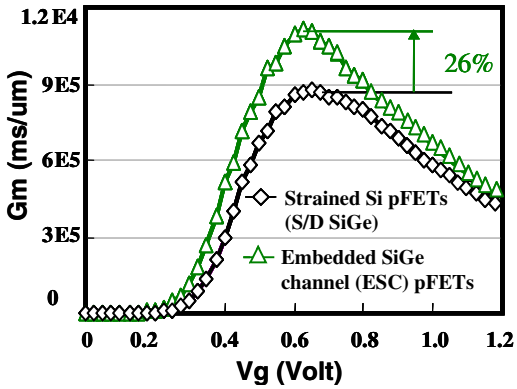


**Figure 4.** ESC device showing 26% p-FET $G_m$ gain higher than that of the conventional strained Si p-FETs with the S/D SiGe devices.

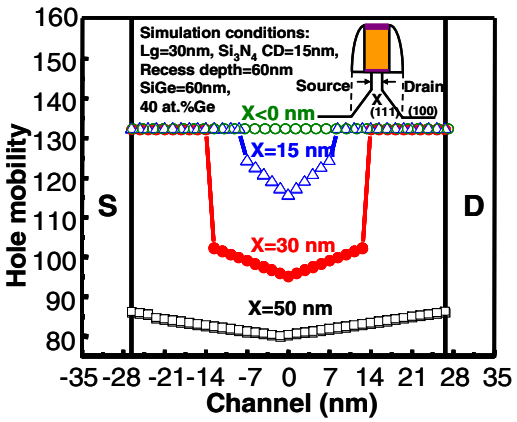


**Figure 5.** Simulation of the hole mobility of the ESC structure and the S/D SiGe structure. The epitaxial SiGe layer sharing more area of the Si channel shows higher channel Si stress induced mobility enhancement.

$G_m$ performance enhancement, higher than that of the strained Si p-FETs with S/D SiGe under a comparable threshold voltage ($V_{th}$). Higher hole mobility and $G_m$ improvement can lead to a better device performance in the strained SiGe channel of the ESC p-FETs than the strained Si p-FETs.

Figure 5 simulates the hole mobility in the ESC structure and the strained Si structure with the S/D SiGe. We calculate the hole mobility by the change in effective mass and carrier scattering with the stress treatment and different Ge concentrations in the SiGe channel. The stress distribution is simulated by ANSYS simulation tool first, and the SiGe effective mass, the change in scattering rate and the corresponding hole mobility with stress are calculated by the $6 \times 6$ k.p (Kroning–Penney) model. Both SiGe material in the channel and compressive stress in the channel benefit higher hole transport mobility. On the other hand, we can also observe that when the epitaxial SiGe layer shares more Si substrate region in the hole conduction channel, which means the proximity of the intra-recess spacing, $X$ becomes smaller, the hole mobility in the strained Si can be further enhanced. Hence, the average hole mobility in the device increases with decreasing Si region $X$. The hole mobility of the ESC structure is enhanced to the highest value as the epitaxial SiGe layer filled up the entire channel region. Based on the simulation,

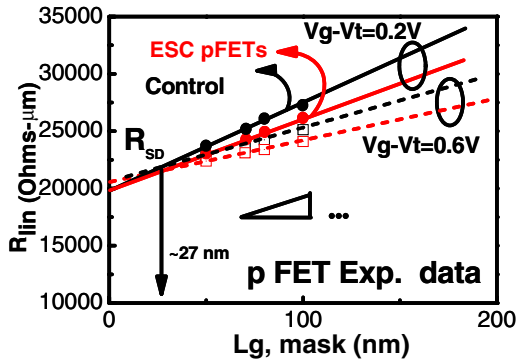


**Figure 6.** $R_{lin}$ as a function of gate length showing mobility enhancement for the ESC p-FET device.

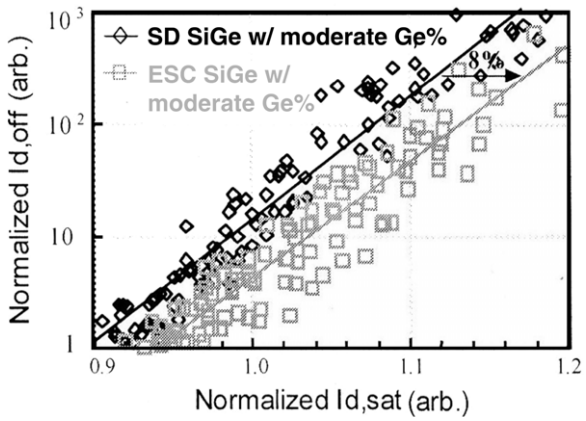


**Figure 7.** $I_{on}$–$I_{off}$ characteristic of p-FET devices showing a performance improvement gain of 8% for ESC wafers. No other strain element such as a compressive stressed nitride liner was used in either the control or the ESC devices.

the ESC structure has a hole mobility of about 56% higher than that of the S/D SiGe structure. However, only 26% $G_m$ gain enhancement is observed for ESC p-FET devices in our experiment. It is conjectured to the existence of the channel resistance and S/D contact resistance [14]. The superior p-FET performance of the ESC structure is considered as a highly potential candidate in the future nano-p-MOSFET node and FinFETs.

Figure 6 shows a clear difference in the slope between the control (strained Si device with S/D SiGe) and the ESC p-FET device in the $R_{lin}$ (resistance in the linear region of the $I$–$V$ curve) versus $L_g$, mask (gate length by mask) plot [15]. This obvious difference in slopes results from a 26% enhancement in transconductance gain by the higher carrier transport mobility for the ESC p-FETs than for the control wafer under the comparable effective gate length, $L_{g,eff}$, which was electrically extracted by the Terada method in the linear region of the current–voltage relationship [16].

In fact, the effect of this increased mobility can be seen in the $I_{on}$–$I_{off}$ characteristics shown in figure 7. In order to isolate the higher mobility effect of ESC alone, no other strain element such as a compressive stressed nitride liner was incorporated into either the control or the ESC p-FET devices. $V_t$ roll-off and overlap capacitance were well matched. At a fixed $I_{off}$ value, the drive current gain of the ESC p-FETs with moderate Ge content is ∼8% higher than that of the control devices.

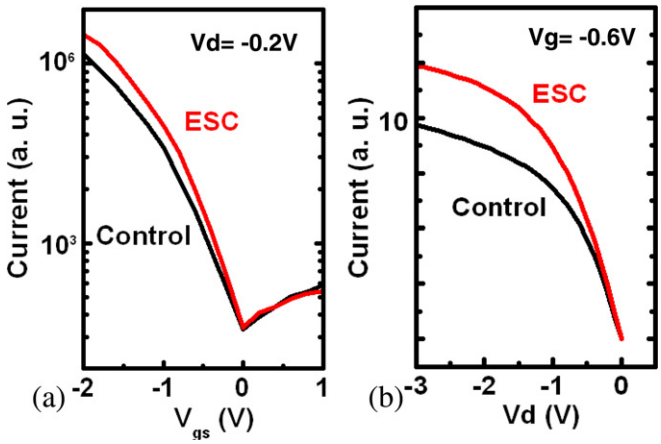


**Figure 8.** (*a*) $I_{ds}$–$V_{ds}$ and (*b*) $I_{ds}$–$V_{gs}$ characteristics of 28 nm $L_g$ p-FET with the control wafer and the ESC device.

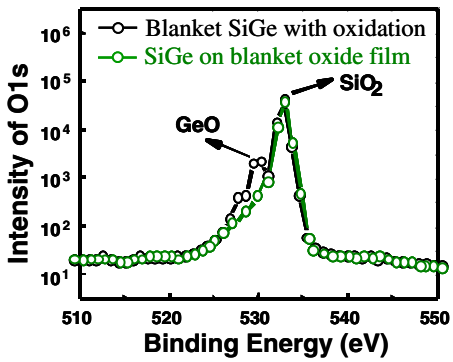


**Figure 9.** XPS analysis data; no Ge–O bonding is observed for the grown SiGe layer on the $SiO_2$, which means only Si–O bonding is observed in our ESC device.

As shown in figure 8(*a*), the $I_d$–$V_{gs}$ plot shows higher ion drive current for ESC devices than for the control of strained Si with S/D SiGe devices. On the other hand, SiGe channel devices, in general, would show a higher $I_{off}$ current than the strained Si devices due to the small band-gap in the SiGe material. Therefore, we use the additional arsenic well implant of about $2 \times 10^{12}\,cm^{-2}$ to suppress $I_{off}$ in our SiGe channel devices (ESC), the same as the control strained Si devices, and then make a clear device performance comparison. Figure 8(*b*) shows the $I_d$–$V_{ds}$ characteristics of the control and the ESC p-FET.

Figure 9 shows the x-ray photoelectron spectrum (XPS) analysis data and indicates that only Si–O bonding is observed in our ESC device. The fact that no Ge–O bonding is observed for the grown SiGe layer on $SiO_2$ reflects that the *in situ* etch does not damage with gate oxide $SiO_2$ at 700 °C and the epitaxially deposited SiGe does not react with the suspending stacked gate dielectric $SiO_2$ to form $GeO_x$ at the deposition temperature of 700 °C. The chemical equations for describing the formation of the ESC structure are expressed as follows:

$$2Cl_{2(g)} + Si_{(s)} \rightarrow SiCl_{4(g)} \qquad T = 700\,^{\circ}C \tag{1}$$

$$4HCl_{(g)} + Si_{(s)} \rightarrow SiCl_{4(g)} + 4H_{(g)} \qquad T = 700\,^{\circ}C \tag{2}$$

$$4HCl_{(g)} + SiO_{2(s)} \rightarrow SiCl_{4(g)} + 2H_{2(g)} + O_{2(g)} \qquad T > 1800\,^{\circ}C \tag{3}$$

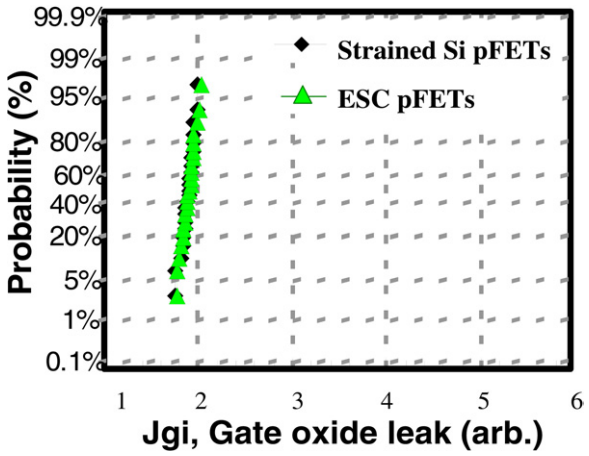


**Figure 10.** ESC device showing comparable gate oxide leakage performance with the strained Si p-FETs, because there is no $GeO_x$ composition during SiGe deposition according to the XPS analysis.

$$12HCl_{(g)} + Si_3N_{4(s)} \rightarrow 3SiCl_{4(g)} + 4NH_{3(g)} \quad T > 1800\,^{\circ}C \tag{4}$$

$$GeH_{4(g)} + SiO_{2(s)} \rightarrow SiH_{4(g)} + 2GeO_{2(s)} \quad T > 1800\,^{\circ}C. \tag{5}$$

In the literature, the conventional SiGe channel without Si surface passivation formed a gate dielectric with the interface composed of $GeO_x$/SiGe, which caused numerous interfacial defects and became one of the most crucial issues in the SiGe channel p-MOSFETs [17, 18]. Then, Si surface passivation is necessary to avoid $GeO_x$ formation, and a thin Si passivation layer of about 1 nm with good uniformity is very difficult for mass production. Therefore, this approach of the ESC structure can achieve the benefit of a SiGe channel without Si passivation to obtain a superior interface quality in addition to a higher channel mobility in SiGe.

Figure 10 compares the gate leakage current between the ESC device and the control strained Si devices with S/D SiGe. The comparable value between these two devices demonstrates that the insulator layer and the interface between $SiO_2$ and the semiconductor surface are good with only Si–O bonding observed in the ECS device. Due to the process design of the ESC, it cannot demonstrate a full SiGe channel for a large gate length ($L_g$), such as an MOS capacitor. Therefore, we cannot extract the interfacial defect (Dit) as an index to evaluate the integrity of the gate oxide, instead, we use the gate leakage current as an indicator for the integrity of the gate oxide of the ESC device.

## 4. Conclusion

A novel technique of creating an embedded SiGe channel (ESC) structure without Si surface passivation shows a p-FET $G_m$ gain of 26% higher than that of the conventional strained Si p-FETs with source/drain (S/D) SiGe for 28 nm p-MOSFETs. Better $R_{sd}$ and device gain of 8% in the $I_{on}$–$I_{off}$ plot and improved swing slope in the $I_d$–$V_{gs}$ characteristics all indicate enhanced hole mobility in the ESC p-FETs than the control wafer. According to the XPS analysis, the gate oxide leakage and the reliability of the constant voltage stress were also examined to recognize the superior SiGe/$SiO_2$ interface with Si–O bonding, and no Ge–O bonding. The novel etch process to create the ESC structure is considered as a very promising technique for 28 nm p-MOSFETs and future N/P SiGe channels in FinFETs.

## Acknowledgments

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