

Boosted Gain of the Differential Amplifier Using the Second Gate of the Dual-Gate a-IGZO TFTs

Y.-H. Tai, H.-L. Chiu, L.-S. Chou, and C.-H. Chang

Abstract—A dual-gate amorphous InGaZnO₄ (a-IGZO) thin-film transistor (TFT) has two gate electrodes. The primary gate electrode is at the bottom, and the other is on the top. The drain current of the TFT can be controlled by both the bottom and top gates. This phenomenon provides great flexibility for the circuit design. In this letter, we propose the differential amplifier circuit using the top gate of the dual-gate a-IGZO TFT as an input for positive feedback to boost the gain. It is experimentally verified that the gain of the differential amplifier circuit is increased three times larger than those without the feedback loop.

Index Terms—Differential amplifier circuit, dual-gate amorphous InGaZnO₄ (a-IGZO) thin-film transistor (TFT).

I. INTRODUCTION

AMORPHOUS InGaZnO₄ (a-IGZO) thin-film transistors (TFTs) have attracted much attention for their excellent characteristics, such as high mobility and uniform amorphous structure [1], [2]. They are suitable to use in a large high-resolution display. Compared with the single-gate a-IGZO TFTs, the dual-gate a-IGZO TFTs have the advantages of higher ON-current, better subthreshold swing, and higher electrical reliability [3]. Therefore, in addition to the usage in a display array, a-IGZO TFTs are also tried to search other applications.

A conventional TFT is a three-terminal device with the drain, gate, and source electrodes. Although the MOSFET has the fourth terminal of the body (or substrate), which can affect the drain current I_D of the transistor, it is either connected to the source terminal or commonly biased with other devices to avoid the body effect [4]. Hence, most circuits are designed to be built with three-terminal devices.

A dual-gate a-IGZO TFT also has the fourth terminal (top gate), which can be individually controlled. Taking advantage of the fact that the threshold voltage V_{th} of the dual-gate a-IGZO TFT can be shifted by the top gate of the TFT [5], [6], we are able to design the circuit with more flexibility. In fact,

Manuscript received August 31, 2012; revised September 21, 2012; accepted September 22, 2012. Date of publication November 15, 2012; date of current version November 22, 2012. This work was supported in part by the National Science Council of the Republic of China under Contract NSC100-2628-E-009-021-MY3 and in part by the Frontier Photonics Research Center of the Republic of China under Contract 100W959. The review of this letter was arranged by Editor W. T. Ng.

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Digital Object Identifier 10.1109/LED.2012.2220955

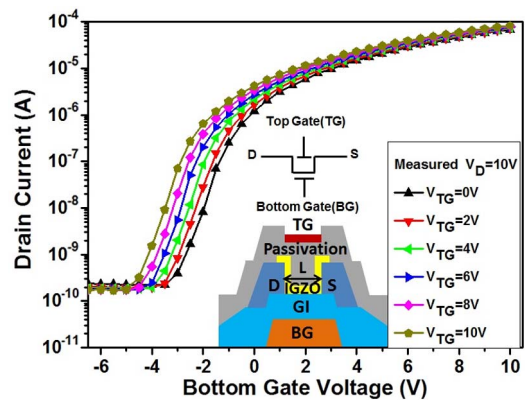


Fig. 1. Curves of drain current I_D versus bottom-gate voltage V_{BG} for the dual-gate a-IGZO TFT at different top-gate voltages V_{TG} .

some new circuits utilizing the dual-gate TFTs were proposed [3], [7]–[13].

In this letter, the benefit of using the second gate is demonstrated with a gain enhancement of the differential amplifier circuit based on the concept of using a positive feedback to the top gate of the dual-gate a-IGZO TFT. The improvement of the performance is experimentally verified.

II. DEVICE FABRICATION AND CHARACTERISTICS

The process flow of the a-IGZO TFTs is described as follows: First, the shaped Ti/Al/Ti gate electrodes were capped with the SiN_x gate dielectric, which was deposited by plasma-enhanced chemical vapor deposition. Then, going to the metal electrode process steps, another Ti/Al/Ti layer was formed by successive deposition with dc sputtering at room temperature. By patterning and dry etching these layers, we finish the source and drain gates. After that, the active layer of a 30-nm-thick a-IGZO film was deposited by dc magnetron sputtering using a target of In:Ga:Zn = 1:1:1. After the active layer was defined by etching, the device was capped with the passivation at 280 °C. Finally, ITO was patterned and shaped for the top-gate electrode.

Fig. 1 shows the curves of I_D versus bottom-gate voltage V_{BG} at the different top-gate voltages V_{TG} with the schematic cross section and circuit symbol of the device in the inset. These transfer curves exhibit parallel shifts at different V_{TG} values. Those phenomena are attributed to the attraction and expelling of free carriers in the active layer by the top gate, which is well explained in [6]. It provides a way of using the bottom gate of the dual-gate a-IGZO TFT as the primary gate while controlling

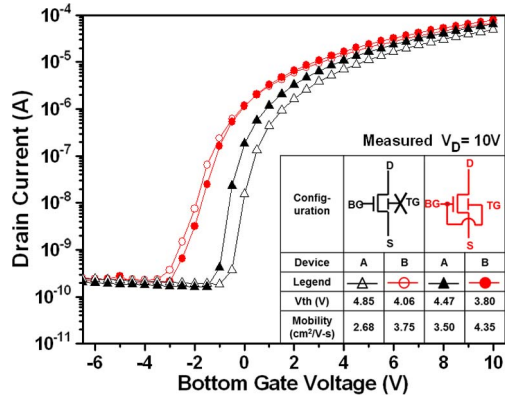


Fig. 2. Characteristics of the two transistors used in our experiments, i.e., T_A and T_B , under different top-gate conditions, namely, the top gate floating and the top gate shorted to the bottom gate.

the top gate independently. This gives us a way of using it to invent new circuits.

To make a differential amplifier, at least two TFTs are required. Fig. 2 shows the curves of I_D versus V_{BG} for two dual-gate a-IGZO TFTs, i.e., T_A and T_B , with their device parameters in the inset table. In general, a differential amplifier uses two identical TFTs as components. In this letter, two dual-gate a-IGZO TFTs with different electrical properties are used to demonstrate the effectiveness of the top-gate feedback. These devices are in the two configurations, namely, the top gate floating and the top gate shorted to the bottom gate. The TFTs are $100 \mu m$ in width, $10 \mu m$ in channel length, and $10 \mu m$ in top-gate length. It can be shown that the characteristic of the TFT with the top gate floating is worse than that with the top and bottom gates shorted [3]. These two TFTs are separately made on two substrates. The threshold voltage V_{th} difference between them is about 1 V.

III. EXPERIMENTAL RESULT AND DISCUSSION

A simple differential amplifier circuit is built by two TFTs (T_A and T_B), two resistors (R_A and R_B), and a constant current source I_S , as shown in Fig. 3. Fig. 4 shows the photograph of the measurement setup. The two TFTs are wire bonded to each other and the external resistors. The sources of T_A and T_B are connected together and biased by I_S of $0.7 \mu A$. The drains of T_A and T_B are connected to the positive supply V_{DD} of 10.5 V through the two resistors of $10 M\Omega$, respectively. The bottom gate of T_B is the applied sweeping voltage $V_{BG,B}$ from -2 to 2 V for the measurement, and the bottom gate voltage of T_A ($V_{BG,A}$) is biased at 1 V to compensate the input offset owing to the V_{th} difference.

The two transistors, i.e., T_A and T_B , are in the three configurations in the circuit. First, the top gates of T_A and T_B are floating, and thus, T_A and T_B can be considered as the conventional single-gate TFTs. Second, the top gates of T_A and T_B are shorted to their own bottom gates, respectively. They are similar to the conventional single-gate TFTs but with better performance. Third, the top gate of T_A is connected to the drain of T_B , and the top gate of T_B is connected to the drain of T_A . In the concept of designing the differential amplifier, when $V_{BG,B}$

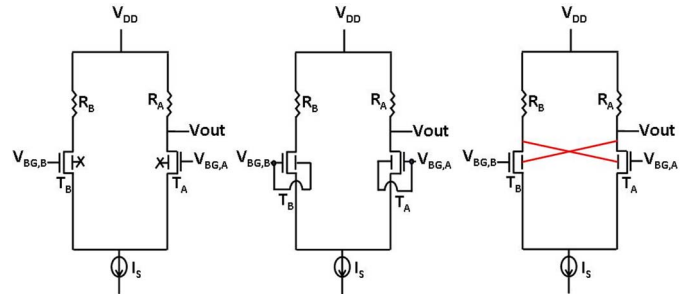


Fig. 3. Differential amplifier circuits in the configurations with (a) conventional TFTs, (b) TFTs of improved performance, and (c) positive feedback.

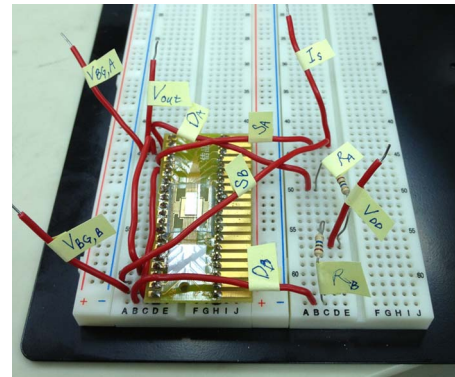


Fig. 4. Measurement setup.

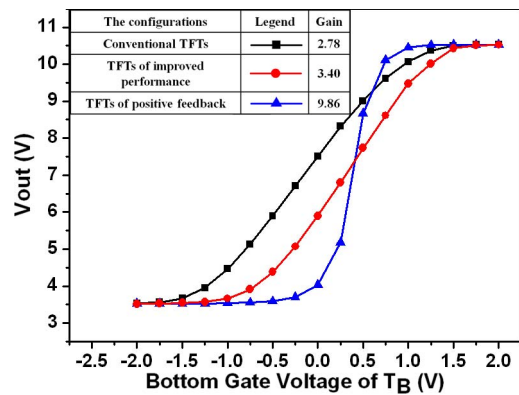


Fig. 5. Measurement result of the V_{out} variation versus different V at the different case of the dual-gate TFT.

gets higher, its drain voltage is lowered and fed to the top gate of T_A , which negatively shifts the V_{th} of T_A . In such way, the drain voltage of T_A is elevated to positively shift the V_{th} of T_B , which further increases the I_D of T_A under a bias of $V_{BG,A}$. Thus, a positive feedback in the circuit is established.

Fig. 5 shows the experimental results of V_{out} versus $V_{BG,B}$ for the three configurations. The steepness of the transfer curve near $V_{BG,B} = 0$ V reflects the differential gain of the amplifier. The slopes of $\Delta V_{out} / \Delta V_{BG,B}$ for the circuits in the three configurations are calculated and listed in the inset table in Fig. 5. Comparing the circuits in the first two configurations, the circuit that is made of a device with better performance has the higher gain. It is straightforward since the gain is proportional to the transconductance of the TFT, which can be increased by higher device mobility [4]. As for the last configuration, the

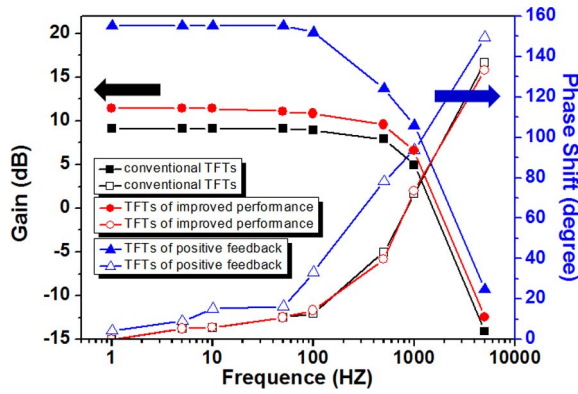


Fig. 6. Frequency and phase response of the circuits.

gain is boosted to more than three times. It is attributed to the positive feedback. A voltage change $\Delta V_{TG,A}$ at the top gate of T_A can be induced by the equation, i.e.,

$$\Delta V_{TG,A} = -\Delta I_{DS,B} \times R_B = -\Delta V_{BG,B} \times G_{m,B} \times R_B \quad (1)$$

where $\Delta V_{BG,B}$ is the voltage increase at $V_{BG,B}$, and $G_{m,B}$ is the transconductance of T_B with respect to the bottom gate. $\Delta V_{TG,A}$ then lowers the current of T_A and results in the increase in V_{out} by the equation, i.e.,

$$\Delta V_{out} = -\Delta I_{DS,A} \times R_A = -\Delta V_{TG,A} \times G_{mTop,A} \times R_A \quad (2)$$

where $G_{mTop,A}$ is the transconductance of T_A with respect to the top gate. V_{out} can further increase the drain current of T_B , push down the top gate voltage of T_A , and thus set up the positive feedback loop.

The frequency and phase response of the circuits are measured at the biasing points with respect to their highest gains. The gain of the proposed circuit keeps better than the other two, as shown in Fig. 6. The corner frequencies of the circuits are not high because they are limited by the large stray capacitance and resistance of the wire bonding package.

In this letter, the circuit is experimentally verified since there is yet no proper SPICE model in the commercial simulation tools for the dual-gate TFTs. Because a mutual interaction between the electric field generated by V_{TG} and V_{BG} is possible [3], the top and bottom gates of a dual-gate TFT can mutually affect the transconductance. This makes the device model for the circuit simulation more difficult to develop. To design more useful circuits of the dual-gate TFTs, we urge for the ability of simulation. Therewith, circuits of the dual-gate TFTs with the versatile usage of the top gates can be dynamically invented.

IV. CONCLUSION

The concept of positive feedback via the top gate of the dual-gate a-IGZO TFT has been successfully demonstrated in the simple circuit of the differential amplifier. The gain increases 3.5 times compared with that of the conventional single-gate a-IGZO TFTs. This concept can be possibly applied in other TFT circuits, which provides effective ways of designing the circuit with better performance.

REFERENCES

- [1] M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J.-S. Park, J. K. Jeong, Y.-G. Mo, and H. D. Kim, "High mobility bottom gate InGaZnO thin film transistors with SiO_x etch stopper," *Appl. Phys. Lett.*, vol. 90, no. 21, p. 212 114, May 2007.
- [2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductor," *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004.
- [3] G. Baek, K. Abe, A. Kuo, H. Kumomi, and J. Kanicki, "Electrical properties and stability of dual-gate coplanar homojunction DC sputtered amorphous indium–gallium–zinc-oxide thin-film transistors and its application to AM-OLEDs," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4344–4353, Dec. 2011.
- [4] A. S. Sedra and K. C. Smith, *Microelectronic Circuit*, 5th ed. New York: Oxford, 2004, pp. 258–259.
- [5] K.-S. Son, J.-S. Jung, K.-H. Lee, T.-S. Kim, J.-S. Park, K. C. Park, J.-Y. Kwon, B. Koo, and S.-Y. Lee, "Highly stable double-gate Ga–In–Zn–O thin-film transistor," *IEEE Electron Device Lett.*, vol. 31, no. 8, pp. 812–814, Aug. 2010.
- [6] N. D. Jankovic and V. Brajovic, " V_{th} compensated AMOLED pixel employing dual-gate TFT driver," *Electron. Lett.*, vol. 47, no. 7, pp. 456–457, Mar. 2011.
- [7] Y.-H. Tai, L.-S. Chou, H.-L. Chiu, and B.-C. Chen, "Three-transistor AMOLED pixel circuit with threshold voltage compensation function using dual-gate IGZO TFT," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 393–395, Mar. 2012.
- [8] M. J. Seok, M. H. Choi, M. Mativenga, D. Geng, D. Y. Kim, and J. Jang, "A full-swing a-IGZO TFT-based inverter with atop-gate-bias-induced depletion load," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1089–1091, Aug. 2011.
- [9] C. H. Park, K. H. Lee, M. S. Oh, K. Lee, S. Im, B. H. Lee, and M. M. Sung, "Dual gate ZnO-based thin-film transistors operating at 5 V: NOR gate application," *IEEE Electron Device Lett.*, vol. 30, no. 1, pp. 30–32, Jan. 2009.
- [10] M. H. Choi, M. J. Seok, M. Mativenga, D. Geng, D. H. Kang, and J. Jang, "A full-swing a-IGZO TFT-based inverter with a top gate-induced depletion load," in *Proc. Soc. Inf. Display Int. Symp. Tech. Dig.*, 2011, pp. 1144–1147.
- [11] H.-W. Zan, W.-T. Chen, C.-C. Yeh, H.-W. Hsueh, C.-C. Tsai, and H.-F. Meng, "Dual gate indium–gallium–zinc-oxide thin film transistor with an unisolated floating metal gate for threshold voltage modulation and mobility enhancement," *Appl. Phys. Lett.*, vol. 98, no. 15, p. 153 506, Apr. 2011.
- [12] Y.-H. Tai, H.-L. Chiu, and L.-S. Chou, "Active matrix touch sensor detecting time-constant change implemented by dual-gate IGZO TFTs," *Solid State Electron.*, vol. 72, pp. 67–72, Jun. 2012.
- [13] S.-M. Yoon, S. Yang, M.-K. Ryu, C.-W. Byun, S.-W. Jung, S.-H. K. Park, C.-S. Hwang, and K.-I. Cho, "Oxide semiconductor-based organic/inorganic hybrid dual-gate nonvolatile memory thin-film transistor," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 2135–2142, Jul. 2011.