Random Pulsewidth Matching Frequency Synthesizer With Sub-Sampling Charge Pump

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***Abstract*—This paper presents a fast locking phase-locked loop (FLPLL) system with reference-spur reduction techniques exploiting random pulsewidth matching and a sub-sampling charge pump. Through the randomization and average of the pulsewidth and the reduction of current mismatch, the frequency synthesizer can reduce the ripples on the control voltage of the voltage-controlled oscillator in order to reduce the reference spur at the output of the phase-locked loop. A random clock generator is used to perform a random selection control. The loop bandwidth of the system can be adjusted by the control voltage so as to reduce the locking time. To demonstrate the effectiveness of the proposed spur-reduction techniques, a 2.5 GHz to 2.7 GHz FLPLL was designed and fabricated using a TSMC 90-nm CMOS process. The proposed circuit can achieve a phase noise of −114 dBc/Hz at an offset frequency of 1 MHz and reference spurs below −74 dBc.**

***Index Terms*—CMOS analog integrated circuits, frequency synthesizer, low spur, phase-locked loops (PLLs), sub-sampling charge pump (SSCP).**

I. Introduction

LOCKING time, phase noise, and spurious-free dynamic range (SFDR) are very important perspectives in designing a frequency synthesizer. For SFDR, one of the major sources of noise is the switching noise from the charge pump at the reference frequency. The switching noise modulates the control voltage and hence the output frequency of the voltage-controlled oscillator (VCO). Two tones that reduce the system performance appears at the upper and lower sidebands around the carrier [1]. A clock with high spectral purity is required in many applications, such as in communication systems to up-convert and down-convert the wanted signals, and in analog-to-digital converts (ADCs) to accurately define the sampling moments.

Phase-locked loop (PLLs) are widely used to generate a high-accuracy clock on chip [2], [3]. For the conventional charge pump (CP), the mismatch between the CP up-current and down-current is the major noise source at the VCO output. The mismatch between the current sources in the CP generates the output-current ripple, which is then converted to ripple on the VCO control voltage by the low-pass filter (LPF), resulting in VCO spur. A narrow loop bandwidth can be used to suppress the ripple, thereby reducing the VCO spur level. However, the PLL needs more locking time and a larger LPF area, which is difficult to implement in the SOC design. As shown in Fig. 1, the main noise sources of spurious tones of an integer-N PLL are digital noise coupling and mismatch currents. The noise sources of the fractional-N PLL are tones in the sigma-delta modulator (fractional spur) and noise from the integer-N PLL. A large bandwidth can offer a fast locking time and reduce the on-chip filter area, but it also reduces the sensitivity of the VCO output. In order to alleviate the tradeoff between low spur and large bandwidth, design techniques of random pulsewidth matching (RPWM) and sub-sampling charge pump (SSCP) have been proposed in this paper.

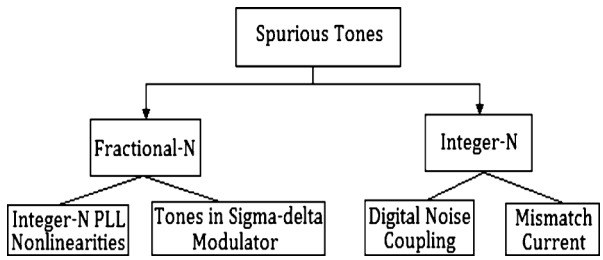

Fig. 1. Noise sources of spurious tones in PLL.

Several papers have been presented that focus on the CP designs to improve current source matching [4], [5] and linearization [6]. A charge-distribution mechanism on the control voltage of the voltage-controlled oscillator was used to suppress reference spur [7], and so was the technique using distributed PFDs and CPs [8]. The approach [8] involved the use of multiple small-current CPs equaling the total current value to enable the reduction of spikes on the control voltage. Pulse position modulation (PPM) was meant to select various delays in the reference and feedback clocks for distributed PFDs/CPs. However, the pulsewidth error between Up and Dn could not be resolved. Besides the use of a spur frequency-boost block [9], doubling the spur frequency and randomizing the charge redistribution time were also utilized to reduce the spurs [10]. In this paper, we propose RPWM to generate the matched CP pulsewidth, and randomize and average the ripples on the control voltage of the VCO. An SSCP is also utilized to reduce ripples on the control voltage in order to achieve a low spur level and relatively smooth spectrum. The frequency synthesizer exploits the RPWM and SSCP techniques to make the reference spur less than −74 dBc. The frequency synthesizer has achieved a phase noise of −114 dBc/Hz at an offset frequency of 1 MHz and reference spurs below −74 dBc at 25 MHz offset.

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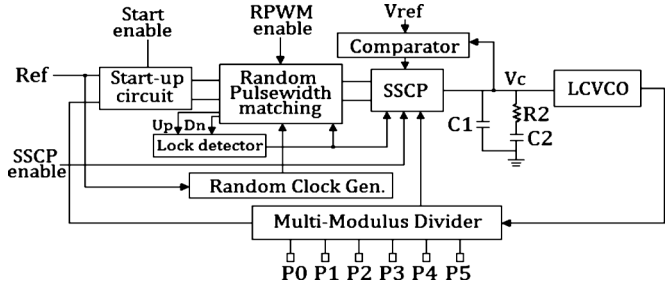

Fig. 2. Proposed fast-locking low-spur PLL.

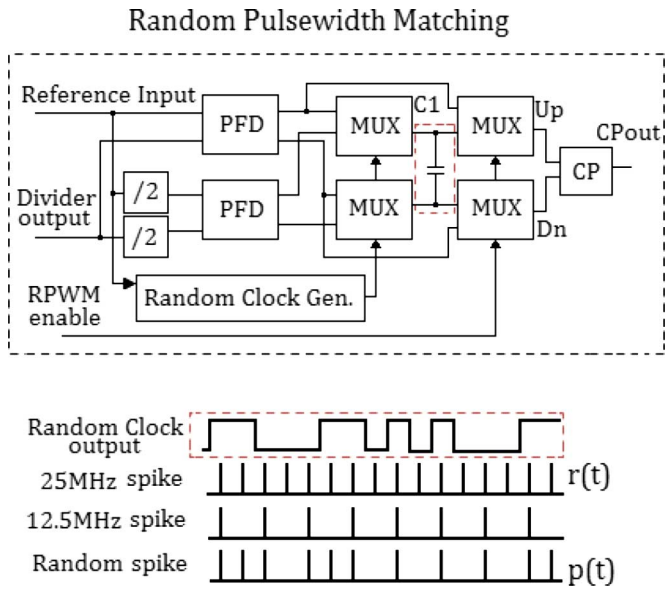

Fig. 3. Random Pulsewidth Matching (RPWM) architecture.

This paper is organized as follows. Section II discusses the RPWM and SSCP techniques. Section III describes the building blocks of the low-spur fast-locking PLL architecture. Section IV shows the experimental results and conclusions are presented in Section V.

II. Spur-Reduction Architectures

A. Random Pulsewidth Matching (RPWM)

The proposed fast-locking low-spur PLL is shown in Fig. 2, where RPWM and SSCP techniques are used to reduce the reference spur. A lock detector was designed into the system to indicate the locking status. The inputs of the lock detector are the two outputs (Up and Dn) of the conventional PFD, while the conventional PFD compares the phase of the feedback clock to the phase of the reference frequency. When the difference between the Up and Dn pulsewidths is less than 120 ps, the lock detector generates a "zero" signal to indicate that the PLL is locked. Fig. 3 shows the RPWM circuit, where new techniques are proposed for an integer-N frequency synthesizer. The conventional phase frequency detector (PFD) compares the phase of the divided-down VCO to the phase of the reference frequency (Ref) and generates two signals, $\mathrm{U_p}$ and $\mathrm{D_n}$ to control CP. It converts the phase error into the pulsewidth difference. The net $\mathrm{U_p}$ and $\mathrm{D_n}$ provided by the CP phase error should be zero when the PLL is phase locked. In the conventional case, there is usually a mismatch between the pulsewidths of $\mathrm{U_p}$ and $\mathrm{D_n}$, which is then converted to ripple on the VCO control voltage by the LPF. When our PLL is in the locked state, the proposed RPWM will enable a 6-bit random clock generator, which can randomize $\mathrm{U_p}$ and $\mathrm{D_n}$ to the CP. As illustrated in which can randomize $\mathrm{U_p}$ and $\mathrm{D_n}$ to the CP. As illustrated in Fig. 3, in the unlocked state, we choose a conventional Ref for tracking. In the locked state, we randomly choose Ref or Ref/2 frequency in PFD for phase comparison; therefore, the spur can be randomized, smoothed, and reduced. With a reference clock period of $\mathrm{T_{ref}}$, the traditional control voltage of the VCO, represented by r(t) as shown in Fig. 3, can be simplified as [10], [11]

$$r(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos\left(\frac{n \times 2\pi}{T_{ref}}\right) t \tag{1}$$

Considering the spur at the reference frequency, the corresponding term is

$$a_1 = \frac{1}{T_{ref}} \int_0^{Tref} r(t) \cos\left(\frac{2\pi}{T_{ref}} t\right) dt \tag{2}$$

p(t) is the new control voltage of the VCO after enabling RPWM; therefore, either the reference frequency or the reference frequency divided by 2 is randomly selected in PFD for phase comparison. p(t) is the random-disturbing waveform with a period of $\mathrm{mT_{ref}}$, where m is determined by the random bit length s, i.e., $\mathrm{m} = 2^{\mathrm{s}}$ for an s-bits random clock generator. $p(t)$ can be expressed as

$$p(t) = b_0 + \sum_{k=1}^{\infty} b_k \cos\left(\frac{k \times 2\pi}{mT_{ref}}\right) t \tag{3}$$

Considering the random spur at the reference frequency, the corresponding term is

$$b_m = \frac{1}{mT_{ref}} \int_0^{mTref} p(t) \cos\left(\frac{2\pi}{T_{ref}} t\right) dt \tag{4}$$

Because $p(\mathrm{t})$ can be expanded into m periodic pulses $S_1(t), S_2(t), \ldots, S_m(t)$ with mTref, each periodic pulse is the same, except for the different phase shifts. Therefore we can rewrite (4) as

$$b_m = \sum_{k=1}^{m} c_{m,k} = \sum_{k=1}^{m} \frac{1}{mT_{ref}} \int_0^{mTref} s_k(t) \cos\left(\frac{2\pi}{T_{ref}} t\right) dt \tag{5}$$

According to the (5), the spur at the reference frequency is reduced by a factor of 2 to the power of the random clock bit length, that is, we can average the spur power spectrum density to accomplish a low spur level and a smooth spectrum. The magnitude of the reference spur can be approximated by the pulsewidth difference $(\mathrm{U_p} - \mathrm{D_n} = \theta_{error})$ of the $\mathrm{U_p}$ and $\mathrm{D_n}$ signals. In our proposed RPWM circuit, as shown in Fig. 3, we add a capacitor C1 to average the $\mathrm{U_p}$ and $\mathrm{D_n}$ pulsewidths to control CP so as to accomplish optimal phase error to the ideal locked point. Without the RPWN circuit, we assume that the pulsewidth

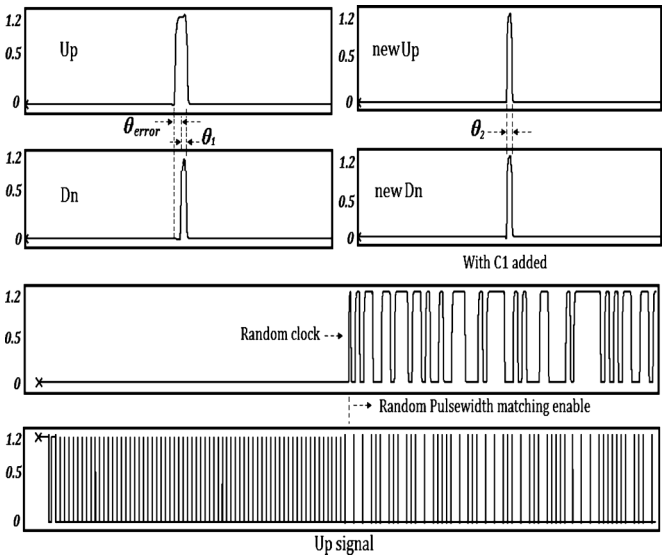

Fig. 4. RPWM timing diagram.

of $\mathrm{D_n}$ is $\theta 1$ and that the pulsewidth of $\mathrm{U_p}$ is $(\theta 1 + \theta_{error})$. C1 is designed as 2 pF; therefore, when the pulsewidth difference (θ_{error}) between Up and Dn is reduced to less than 75 ps under all process corners, the New Up and Dn pulsewidths will be the same to reduce the reference spurs. 75 ps was selected by setting the variation of the VCO output frequency less than 100 ppm with a 2.5 GHz output. A larger C1 enables the pulsewidths of New Up and Dn to equalize more quickly and achieve low spurs; however, this would certainly occupy more area.

When the RPWM is initially enabled, the pulsewidths of the New Up and Dn will not be equal. Capacitor C1 can average the Up and Dn pulsewidths to reduce pulsewidth error between them and the PLL loop still functions like a conventional PLL, except that capacitor C1 has expedited the locking process approaching the ideal locked point. With a decrease in the pulsewidth difference between Up and Dn to less than 75 ps, the New Up and Dn pulsewidths are equalized, which enables a low-spur PLL. With our proposed RPWM circuit, the pulsewidths of the new $\mathrm{U_p}$ and new $\mathrm{D_n}$ are the same and equal to $\theta 2 = \theta 1 + (\theta_{error}/2)$, as shown in Fig. 4. Fig. 4 shows the timing diagram of the RPWM, where the new random $\mathrm{U_p}$ and $\mathrm{D_n}$ signals are generated by a random clock and an average capacitor C1. The $\mathrm{V_{ripple}}$ is generated in the CP output of the locked PLL. The proposed RPWM can minimize the $\mathrm{V_{ripple}}$ because the pulsewidth of $\mathrm{U_p}$ is equal to that of $\mathrm{D_n}$; however, on the contrary, for a conventional PLL, the pulsewidth difference between $\mathrm{U_p}$ and $\mathrm{D_n}$ usually generates a large $\mathrm{V_{ripple}}$ on the control voltage.

$$Q = CV \Rightarrow V_{ripple} = \frac{I \cdot t}{C_{LPF}} = \frac{\left(I_{pump-U_p} \cdot t_{U_p}\right) - \left(I_{pump-D_n} \cdot t_{D_n}\right)}{C_{LPF}} \tag{6}$$

$$\frac{\left(I_{pump-U_p} \cdot (\theta_1 + \theta_{error}) - I_{pump-D_n} \cdot \theta_1\right)}{C_{LPF}} > \frac{\left(I_{pump-U_p} - I_{pump-D_n}\right) \cdot \theta_2}{C_{LPF}}. \tag{7}$$

From (6) and (7), the ripple on the control voltage $(\mathrm{V_{ripple}})$ is determined by the charge current of CP $(I_{pump-Up})$, the discharge current of CP $(I_{pump-Dn})$, the CP charge time (t_{Up}), and the CP discharge time (t_{Dn}). Reducing the mismatch between the charge and discharge currents $(I_{pump-Up}, I_{pump-Dn})$ and the pulsewidth difference between the $\mathrm{U_p}$ and $\mathrm{D_n}$ signals (t_{Up}, t_{Dn}) can minimize the reference spur. However, I_{pump} is restricted to the specified loop stability and the current mismatch and pulsewidth difference are difficult to prevent in a conventional integer-N PLL. Consequently, the presented RPWM randomizes the ripple to obtain a smooth spectrum, and averages the pulsewidth difference between $\mathrm{U_p}$ and $\mathrm{D_n}$ to reduce the ripple amplitude $(\mathrm{V_{ripple-conventional}} > \mathrm{V_{ripple-RPWM}})$ on the voltage control line so as to reduce the reference spur in the frequency domain.

When RPWM is enabled and New Up and Dn have equalized, like all of the PLLs in a locked state, except that there is no pulsewidth error between New Up and Dn, PFD appears to lose its effectiveness, but the detection function remains in operation. Once the pulsewidth difference between Up and Dn exceeds 75 ps, the PLL loop resumes operation because there is difference between New Up and Dn, and the PLL will move towards the ideal locked point once again. Furthermore, the lock detector continues detecting the locking status. Once the PLL is unlocked, the PLL switches back to the conventional mode by disabling RPWM and resuming the locking process.

B. Sub-Sampling Charge Pump (SSCP)

As shown in Fig. 5, an SSCP was designed to reduce current mismatch $(\mathrm{I_{Up}}, \mathrm{I_{Dn}})$ as well as locking time in the locked PLL. The concepts of fast locking in low-spur PLL have been discussed in the literature [12]–[14]. During the locking process of the PLL, when SSCP is not turned on, the MUX1 delivers Vbias1 to provide a tail current $\mathrm{I_B}(\mathrm{Vbias1} = \mathrm{V_{DD}})$. As shown in Fig. 2, the comparator will compare the control voltage of the VCO with a constant voltage $\mathrm{V_{ref}}$ to control the SSCP. If the Vc of the VCO is smaller than $\mathrm{V_{ref}}$, the MUX2 is enabled by the comparator output to provide an additional tail current $\mathrm{I_A}$ to expedite the locking process and reduce the locking time. As Vc continues to increase, when Vc becomes larger than $\mathrm{V_{ref}}$, the comparator will turn off the additional tail current $\mathrm{I_A}$, therefore reducing the tail current back to the original $\mathrm{I_B}$. The loop bandwidth of the FLPLL system can be adjusted by the control voltage. When the control voltage is less than $\mathrm{V_{ref}}$, a wider bandwidth can be obtained. When the control voltage becomes larger than $\mathrm{V_{ref}}$, the loop bandwidth becomes smaller.

In PLL design, conventionally there is usually a mismatch between $\mathrm{I_{Up}}$ and $\mathrm{I_{Dn}}$, that is, $\mathrm{I_{Up}} \neq \mathrm{I_{Dn}}$, which is then converted to spikes on the VCO control voltage, injecting noise to the VCO and reducing the performance of the frequency synthesizer. The proposed RPWM circuit averages the $\mathrm{U_p}$ and $\mathrm{D_n}$ pulsewidths, which results in $\mathrm{t_{Up}} = \mathrm{t_{Dn}}$. However, in the conventional CP, usually still exists $\mathrm{I_{Up}} \neq \mathrm{I_{Dn}}$. Therefore, an SSCP techniques is proposed to alleviate the mismatch between the charge current $\mathrm{I_{Up}}$ and the discharge current $\mathrm{I_{Dn}}$. At the locked

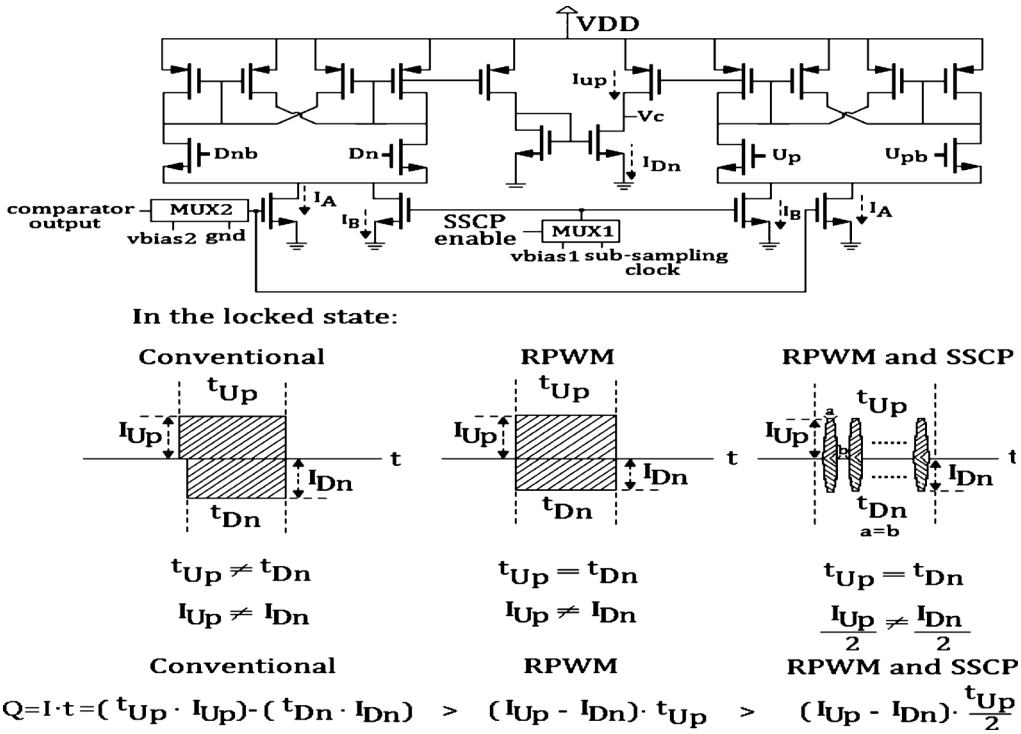

Fig. 5. Sub-sampling Charge Pump (SSCP)

state, after SSCP is enabled, the MUX1 will choose sub-sampling clock to sample the tail current $\mathrm{I_B}$. The period of the reference clock is 40 ns. However, the period of a sub-sampling clock is only 0.8 ns, where the very high speed sub-sampling clock samples the tail current $\mathrm{I_B}$ for 0.4 ns within each 0.8 ns. When the tail current of the SSCP is on, the PLL operates normally with the same amount of CP current, like the conventional PLL. With such a high speed sub-sampling clock, the charge current $\mathrm{I_{Up}}$ and the discharge current $\mathrm{I_{Dn}}$ in the time domain appear as a series of short-period trapezoidal waveforms with heights of $\mathrm{I_{Up}}$ and $\mathrm{I_{Dn}}$, respectively, instead of one rectangular waveform, as shown in Fig. 5. If the charge current $\mathrm{I_{Up}}$ and the discharge current $\mathrm{I_{Dn}}$ in the time domain were one rectangular waveform, the equivalent charge (the rectangular area) would be $\mathrm{Q = I \cdot t = (I_{Up} \cdot t_{Up})/1}$ and $\mathrm{(I_{Dn} \cdot t_{Dn})/1}$. When the charge current $\mathrm{I_{Up}}$ and the discharge current $\mathrm{I_{Dn}}$ in the time domain is a series of trapezoidal waveforms with $\mathrm{a = b}$, as shown in Fig. 5, the total area (equivalent charge) $\mathrm{Q = I \cdot t = (I_{Up} \cdot t_{Up})/2}$ and $\mathrm{(I_{Dn} \cdot t_{Dn})/2}$. Thus, if there is mismatch between $\mathrm{I_{Up}}$ and $\mathrm{I_{Dn}}$, the mismatch will be reduced to 1/2 by the proposed SSCP. To sum up, for a conventional CP it is given as

$$t_{Up} \neq t_{Dn}, \quad \mathrm{I}_{Up} \neq \mathrm{I}_{Dn} \tag{8}$$

for a RPWM CP it is given as

$$t_{Up} = t_{Dn}, \quad \mathrm{I}_{Up} \neq \mathrm{I}_{Dn} \tag{9}$$

and for RPWM and SSCP it is given as

$$t_{Up} = t_{Dn}, \quad \frac{1}{2}\mathrm{I}_{Up} \neq \frac{1}{2}\mathrm{I}_{Dn}. \tag{10}$$

Therefore, the $\mathrm{V_{ripple}}$ amplitude on the control voltage can be rewritten as

$$\begin{aligned} V_{ripple} &= \frac{\frac{1}{2}\left(I_{pump-U_p} \cdot \theta_2\right) - \frac{1}{2}\left(I_{pump-D_n} \cdot \theta_2\right)}{C_{LPF}} \\ &= \frac{\left(I_{U_p} - I_{D_n}\right) \cdot \theta_2}{2C_{LPF}}. \end{aligned} \tag{11}$$

The SSCP technique can effectively eliminate the current ripple spike. Combining RPWM and SSCP achieves more ripple suppression ($\mathrm{V_{ripple-conventional}} > \mathrm{V_{ripple-RPWM}} > \mathrm{V_{ripple-RPWM,SSCP}}$). In the locked VCO frequency of 2.5 GHz, the frequency of $\mathrm{I_{Up}}$ and $\mathrm{I_{Dn}}$, the sub-sampling frequency, is VCO/2.

Equation (11), which we know uses the sub-sampling technique, is equivalent to increasing $\mathrm{C_{LPF}}$ to get more suppression on the current spike of the locked state and obtain a smooth spectrum in the frequency domain. When RPWM is enabled, RPWM averages the pulsewidth and randomizes the $\mathrm{U_p}$ and $\mathrm{D_n}$ signals. The SSCP is enabled so as to accomplish a low current ripple. Another factor which also contributes to the CP current ripple is the charge sharing between the parasitic capacitances of the LPF, thereby using sub-sampling ($\mathrm{2C_{LPF}}$) to minimize the parasitic charge sharing of the LPF. The proposed RPWM and SSCP can randomize, average the pulsewidth, and reduce the amplitude of the ripples on the control voltage of the VCO. The sub-sampling technique ($\mathrm{2C_{LPF}}$) can effectively reduce the reference spur at the output of the locked PLL.

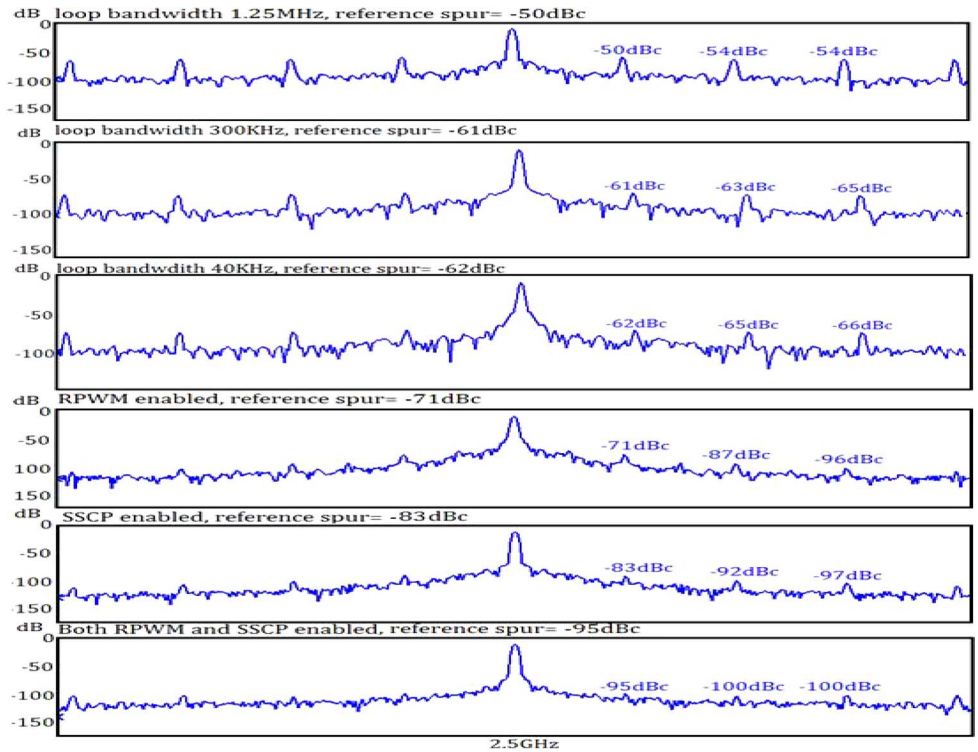

Fig. 6. Simulation of the spur reduction.

III. Synthesizer Design

A. Fast-Locking Low-Spur PLL

In this paper, as shown in Fig. 2, RPWM and SSCP are used to achieve the randomization, average, and reduction of the CP output ripple. During the operation of a conventional PLL mode, we employed a high loop-bandwidth-to-reference frequency ratio of 1/20 to achieve a fast locking PLL. After the PLL is locked, RPWM and SSCP are enabled to reduce the reference spur. When the spur reduction mechanisms were enabled, the effective loop bandwidth was decreased accordingly. A reduction in loop bandwidth effectively suppressed phase noise and the reference spur. However, using the proposed RPWM and SSCP, Up and Dn are randomized and averaged, and the charge current I_{Up} and the discharge current I_{Dn} in the time domain appear as a series of short-period trapezoidal waveforms, which reduces the reference spur even further. This can be verified by the simulation results shown in Fig. 6. Without a spur suppression mechanism, simulation results show a reference spur of -50 dBc. When the capacitance in the LPF is increased to reduce the loop bandwidth to 300 kHz, which is the measured loop bandwidth with only SSCP on, the reference spur becomes -61 dBc. When the loop bandwidth was further reduced to 40 kHz, which is the measured loop bandwidth with both RPWM and SSCP on, through increased capacitance, the reference spur was -62 dBc. However, when the spur suppression circuit for RPWM was enabled, the reference spur was -71 dBc. When the spur suppression circuit for SSCP was enabled, the reference spur was -83 dBc. When RPWM and SSCP were both enabled, the reference spur was -95 dBc. These simulation results are summarized in Table I.

TABLE I
Summary of Spur-Reduction Simulation

Loop bandwidth	Reference spur
Loop bandwidth 1.25MHz (Original PLL without spur reduction)	-50 dBc
Loop bandwidth 300kHz	-61 dBc
Loop bandwidth 40kHz	-62 dBc
RPWM enabled	-71 dBc
SSCP enabled	-83 dBc
RPWM and SSCP enabled	-95 dBc

Thus, despite a reduction in loop bandwidth, the reference spur could be effectively further reduced using the proposed techniques.

Moreover, with the proposed techniques, the loop bandwidth can been reduced without the need for a large capacitance area, providing a tremendous savings in chip area. The proposed techniques can be easily applied to other advanced processes.

B. Low-Pass Filter

The spur at the reference frequency is reduced by a factor of 2 to the power of the random clock bit length. In this proposed FLPLL, in the locked state, the frequency of the random clock is

$$\frac{25\ \text{MHz}}{2^6 - 1} = 396\ \text{KHz}. \tag{13}$$

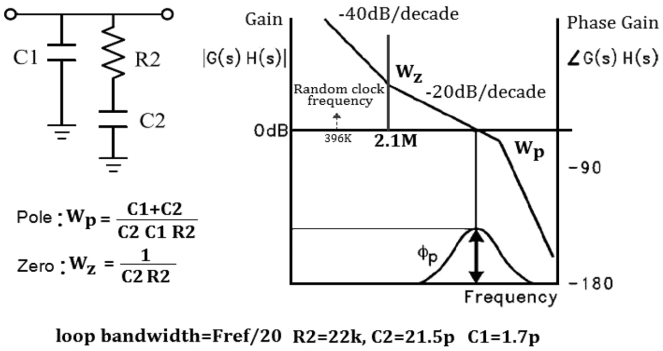

Fig. 7. Design of the loop filter.

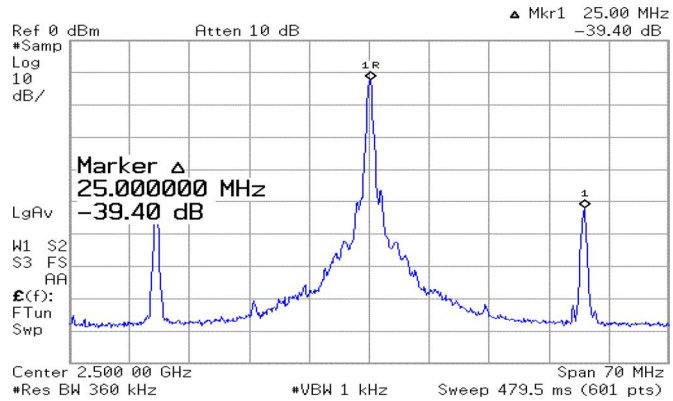

Fig. 8. Measured reference spurs at 2.5 GHz locked frequency.

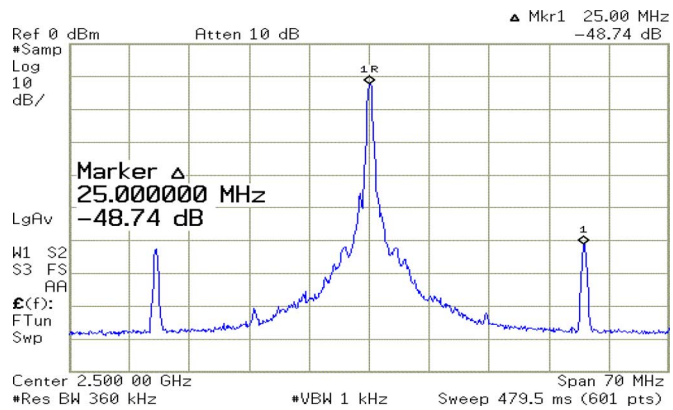

Fig. 9. Measured reference spurs at 2.5 GHz with RPWM on.

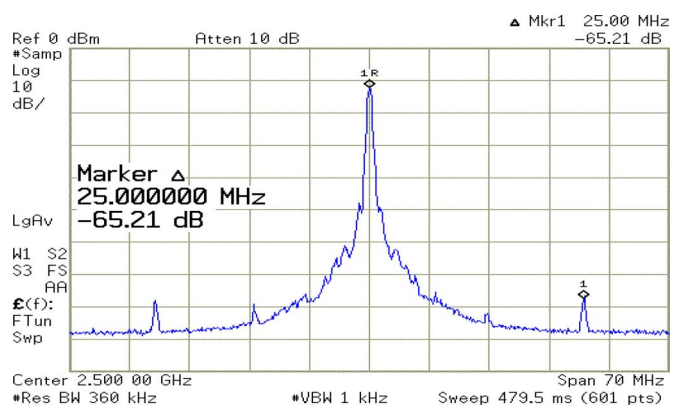

Fig. 10. Measured reference spurs at 2.5 GHz with SSCP on.

The LPF [15] was designed by using the open loop gain bandwidth and phase margin to determine the component values. As shown in Fig. 7, the phase margin will increase because of the zero and the system is stable at the unity-gain frequency. A third-order low-pass filter could be designed to attenuate the reference spur [16]; however, through the use of our proposed RPWM and SSCP techniques, the reference spur can be efficiently reduced while only a second-order LPF has been used. In other words, the proposed techniques include a second-order LPF, instead of a third-order LPF, which is adequate to provide a low-spur output clock.

C. Multi-Modulus Divider (MMD)

The choice of the divider architecture is essential for achieving low power dissipation and high design flexibility. One advantage of the MMD is that all the cells in the divider are identical, which can largely facilitate the layout work. The programmable divider can provide an output signal with a period of

$$T_{out} = (2^6 + p_5 \cdot 2^5 + p_4 \cdot 2^4 + p_3 \cdot 2^3 + p_2 \cdot 2^2 + p_1 \cdot 2^1 + p_0) \times T_{in}. \quad (14)$$

Equation (14) shows that the division ratios from 64 (if all CON $= 0$) to 127 (if all CON $= 1$) are achieved [17].

IV. Experimental Results

The circuit was fabricated using a TSMC 90-nm 1P9M CMOS process. The fast-locking low-spur frequency synthesizer has a tunable VCO ranging from 2.3 GHz to 2.76 GHz, and an output frequency range from 2.5 GHz to 2.7 GHz. The reference frequency is 25 MHz. The VCO gain is 380 MHz/V. Without a spur suppression mechanism, experimental results show measured reference spurs of -39 dBc and -36 dBc at 2.5 GHz and 2.6 GHz of the locked frequency by a 25 MHz frequency offset, respectively, as shown in Figs. 8 and 12. When the spur suppression circuit for RPWM is enabled, the measured reference spurs are -49 dBc and -43 dBc at 2.5 GHz and 2.6 GHz, respectively, as shown in Figs. 9 and 13. When the spur suppression circuit for SSCP is enabled, the measured reference spurs are -65 dBc and -64 dBc at 2.5 GHz and 2.6 GHz, respectively, as shown in Figs. 10 and 14. When RPWM and SSCP are both enabled, the measured reference spurs are -74 dBc and -70 dBc at 2.5 GHz and 2.6 GHz, respectively, as shown in Figs. 11 and 15. The phase noise was -107 dBc/Hz with a 40 kHz offset; with only RPWM on, the phase noise was -104 dBc/Hz with a 40 kHz offset; with only SSCP on, the phase noise was -102 dBc/Hz with a 40 kHz offset; with both RPWM and SSCP on, the phase noise was -102 dBc/Hz with a 40 kHz offset. These results are illustrated in Figs. 16, 17, 18 and 19, respectively. The proposed techniques increase phase noise slightly. Enabling the spur reduction mechanisms decreased the effective loop bandwidth. With the spur-reduction functions off, the measured loop bandwidth was 860 KHz. With RPWM on, the measured loop bandwidth was 600 KHz; with SSCP on, the measured loop bandwidth was 300 KHz; when both RPWM and SSCP were turned on, the measured loop bandwidth was 40 KHz.

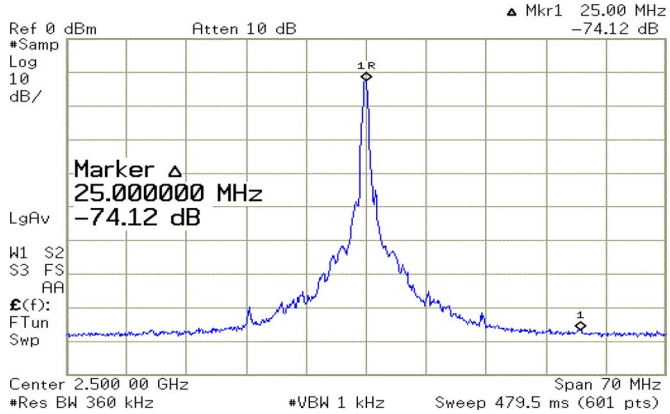

Fig. 11. Measured reference spurs at 2.5 GHz with both RPWM and SSCP on.

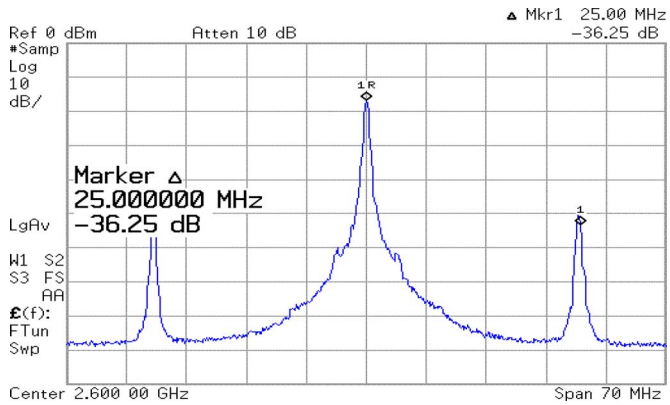

Fig. 12. Measured reference spurs at 2.6 GHz locked frequency.

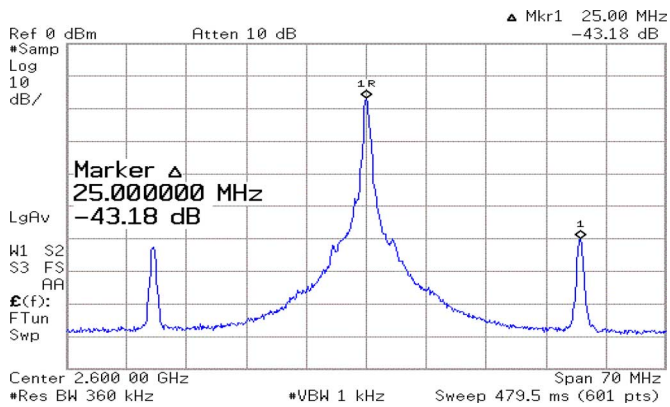

Fig. 13. Measured reference spurs at 2.6 GHz with RPWM on.

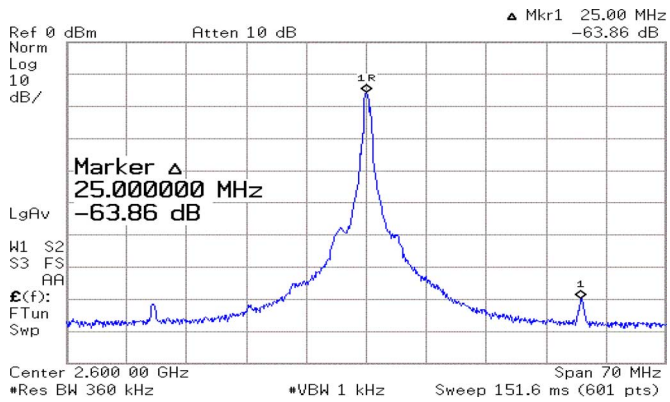

Fig. 14. Measured reference spurs at 2.6 GHz with SSCP on.

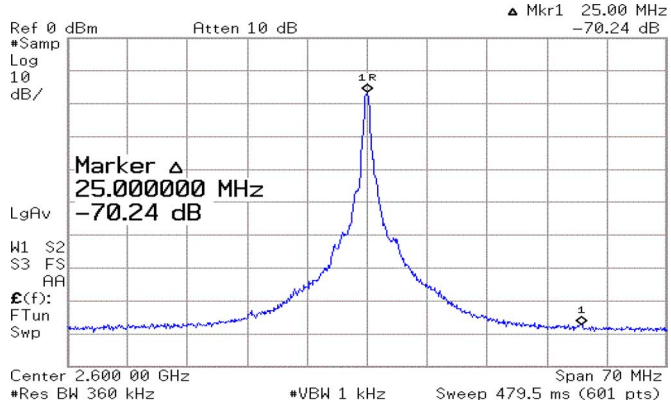

Fig. 15. Measured reference spurs at 2.6 GHz with both RPWM and SSCP on.

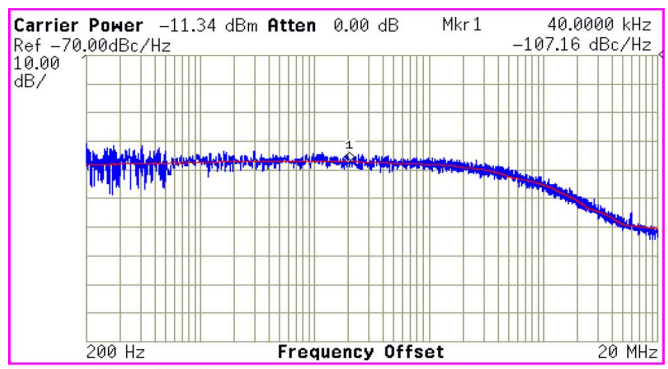

Fig. 16. Measured phase noise with 40 kHz offset at 2.5 GHz.

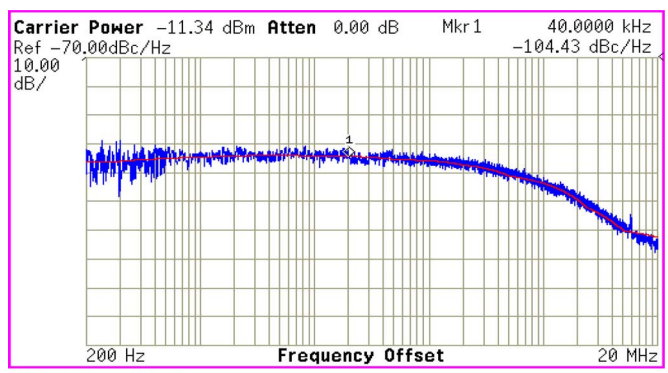

Fig. 17. Measured phase noise with 40 kHz offset at 2.5 GHz with RPWM on.

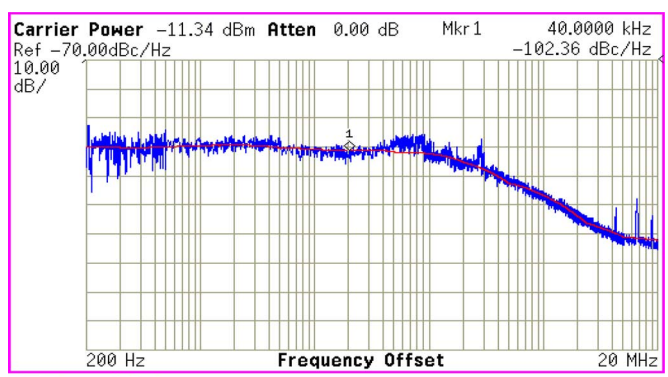

Fig. 18. Measured phase noise with 40 kHz offset at 2.5 GHz with SSCP on.

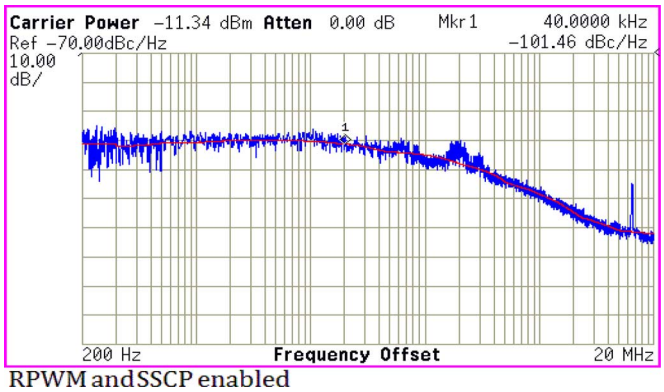

Fig. 19. Measured phase noise with 40 kHz offset at 2.5 GHz with both RPWM and SSCP on.

TABLE II
PHASE NOISE PERFORMANCE

Phase noise	Conventional PLL	RPWN enabled	SSCP enabled	RPWN and SSCP enabled
@40 kHz	-107 dBc/Hz	-104 dBc/Hz	-102 dBc/Hz	-102 dBc/Hz
@600 kHz	-110 dBc/Hz	-109 dBc/Hz	-108 dBc/Hz	-110 dBc/Hz
@1 MHz	-113 dBc/Hz	-111 dBc/Hz	-113 dBc/Hz	-114 dBc/Hz
Measured bandwidth	860 kHz	600 kHz	300 kHz	40 kHz

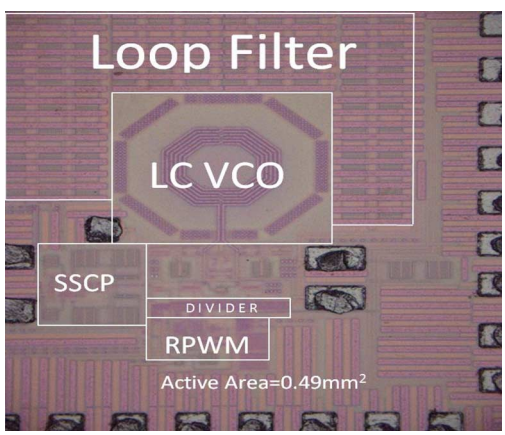

Fig. 20. Die micrograph.

With a reduction in the loop bandwidth, the phase noise can still be well suppressed. The phase noise performance under different conditions is summarized in Table II. The die micrograph is shown in Fig. 20. The area of the synthesizer is 0.49 mm^2, including the LPF.

The performance summary and comparisons are provided in Table III and Table IV, respectively. This work has lower reference spur levels by exploiting the RPWM and SSCP techniques

TABLE III
PERFORMANCE SUMMARY

Items	Performance
Technology	TSMC 90-nm 1P9M CMOS
Power Supply	1.2V
Reference Fre.	25MHz
LC VCO	2.3GHz-2.76GHz
Divider ratio	100
K_{vco}	380MHz/V
Spur level	−39 dBc
Spur level (RPWM on)	−49 dBc
Spur level (SSCP on)	−65 dBc
Spur level (RPWM and SSCP on)	−74 dBc
Spur reduction	35 dB
Phase noise @ 40 kHz (conventional)	−107 dBc/Hz
Phase noise @ 40 kHz (RPWM enabled)	−104 dBc/Hz
Phase noise @ 40 kHz (SSCP enabled)	−102 dBc/Hz
Phase noise @ 40 kHz (Both RPWM and SSCP enabled)	−102 dBc/Hz
Power consumption	12 mW

with the 2nd-order LPF frequency synthesizer. The reference spurs are lowered by about 35 dB (from −39 to −49 dBc for RPWM enabled, and from −49 to −74 dBc with both RPWM and SSCP on), which is still far below the simulated reduction of 45 dB (from −50 to −95 dBc with both RPWM and SSCP on). The noise floor increases by PCB coupling noise and power supply injection noise. As compared with other works, this work gets more suppression of reference spurs while the phase noise still maintains at a low level. The total power consumption of the proposed synthesizer is 12 mW.

V. CONCLUSIONS

The conventional charge pump-based high performance PLL has been facing increasing challenges imposed to scale with sub-micron VLSI technologies. The design tradeoffs among the PLL loop bandwidth, reference noise, VCO noise, and divider noise limit the usefulness of the integer-N PLL. In this paper, design techniques to reduce the PLL reference spurs and to achieve fast locking have been proposed. The low spur frequency synthesizer, which can randomize, average the pulsewidth, and reduce the amplitude of the ripples on the VCO control voltage in order to reduce the proposed. To demonstrate the effectiveness of the proposed reference spur at the output of the locked PLL, has been spur-reduction techniques, a 2.5 GHz–2.7 GHz

TABLE IV
PERFORMANCE COMPARISON WITH OTHER WORKS

	[1]	[9]	[14]	[18]	[19]	This work
Process	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.18um CMOS	90nm CMOS
Supply	1.8	1.8	1.8	1.8	1.8	1.2
Ref. freq.	12 MHz	1 MHz	20 MHz	55.25 MHz	50 MHz	25 MHz
Freq.(GHz)	2.4	4.8/2.4	2.2 – 2.6	2.21	3.6	2.5 – 2.7
F_{BW}/F_{ref}	1/12	N/A	1/74	N/A	1/50	1/20
Loop filter	N/A	2nd	N/A	N/A	N/A	2nd
Phase noise@(dBc/Hz)	-108@100kHz	-104/-110 @1 MHz	-105.5@1MHz	-126@200kHz	-93@100kHz	-102@40kHz
Ref. spur (dBc)	– 70	– 55	– 52	– 46	– 74	– 74
Power(mW)	39	18	22	7.6	110	12

FLPLL is designed and fabricated using a TSMC 90-nm CMOS process and has achieved a phase noise of -114 dBc/Hz at a 1 MHz offset frequency and reference spurs below -74 dBc. The proposed techniques can be easily applied to other advanced processes.

ACKNOWLEDGMENT

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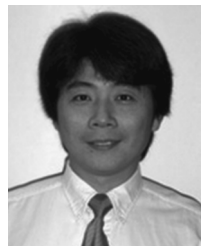

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