Resistor-Less Design of Power-Rail ESD Clamp Circuit in Nanoscale CMOS Technology

Chih-Ting Yeh, *Student Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—A resistor-less power-rail electrostatic discharge (ESD) clamp circuit realized with only thin-gate-oxide devices and with a silicon-controlled rectifier (SCR) as the main ESD clamp device has been proposed and verified in a 65-nm CMOS process. By skillfully utilizing the gate leakage current to realize the equivalent resistor in the ESD-transient detection circuit, the RC-based ESD detection mechanism can be achieved without using an actual resistor to significantly reduce the layout area in I/O cells. From the measured results, the new proposed power-rail ESD clamp circuit with an SCR width of 45 μm can achieve 5-kV human-body-model and 400-V machine-model ESD levels under the ESD stress event while consuming only a standby leakage current of 1.43 nA at room temperature under the normal circuit operating condition with 1-V bias.**

***Index Terms*—Electrostatic discharge (ESD), gate leakage, power-rail ESD clamp circuit, silicon-controlled rectifier (SCR).**

I. Introduction

In nanoscale CMOS technology, the gate oxide thickness has been scaled down to several nanometers. Such a thin gate oxide causes the gate tunneling issue more serious [1], [2]. The gate leakage current of a MOSFET is directly dependent on the poly-gate area and the gate oxide thickness, which has been investigated and modeled in the BSIM4 MOSFET model [3], [4]. For on-chip electrostatic discharge (ESD) protection, the ESD clamp device drawn in the layout style of a big field-effect transistor (BigFET) had demonstrated excellent ESD protection performance [5]–[10]. However, the ESD clamp device with BigFET layout style is not adequate for low power consumption anymore in the nanoscale CMOS technology because a BigFET of large device dimensions with thin gate oxides would lead to intolerable gate leakage current. Therefore, the ESD detection circuit has to be designed with consideration of the gate leakage issue. Recently, the low-leakage power-rail ESD clamp circuit in nanometer CMOS technologies has been revealed [11]–[13]. In [11], the gate current was utilized to bias the ESD detection circuit and to reduce the voltage drop across the MOS capacitors. In [12], an RC-based ESD detection circuit with a feedback control inverter was used to avoid the direct leakage path through the MOS capacitor. In [13], the ESD detection circuit consisted of an RC timer, inverters, and a feedback pMOS, which was used to lower the voltage drop across the RC timer and therefore reduce the gate leakage current of the MOS capacitor. However, those previous circuits with large layout areas were more complicated to implement the ESD detection circuits.

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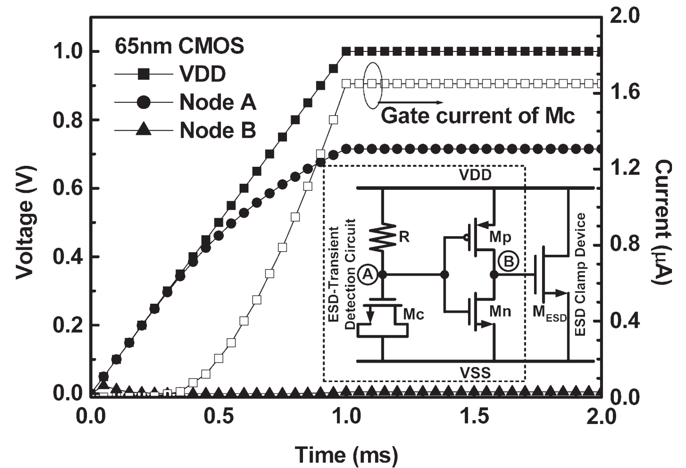

Fig. 1. Simulated voltages on the nodes of the traditional RC-based power-rail ESD clamp circuit [14] and the gate current flowing through the MOS capacitor Mc under the normal power-on condition with a rise time of 1 ms in a 65-nm CMOS process.

In this paper, a new resistor-less design of an ESD detection circuit realized with gate leakage current is proposed and successfully verified in a 65-nm 1-V CMOS technology. The proposed ESD detection circuit realized with only core devices can be accurately activated to generate the trigger current to the ESD clamp device. According to the experimentally measured results, the standby leakage current of the proposed power-rail ESD clamp circuit can be significantly reduced to a few nanoamperes under the normal circuit operating condition with 1-V bias.

II. Gate Leakage Current in the Conventional ESD Clamp Circuit

A. Traditional RC-Based Power-Rail ESD Clamp Circuit

The RC-based power-rail ESD clamp circuit was traditionally used to protect the core circuits [14], as shown in the inset of Fig. 1. Under the normal circuit operating condition, the MOS capacitor Mc with a large poly-gate area would

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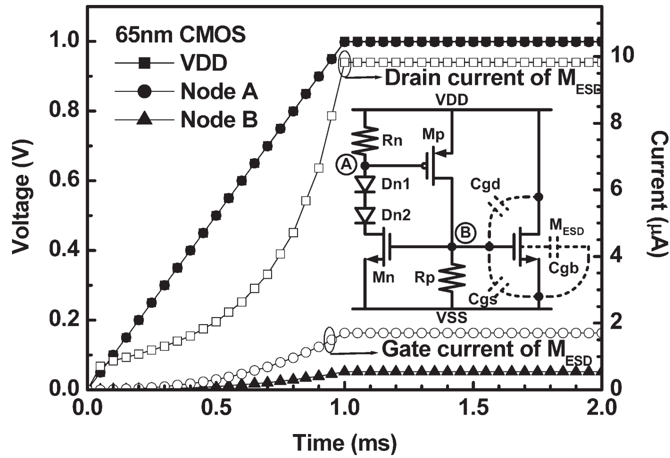


Fig. 2. Simulated voltages on the nodes of the capacitor-less power-rail ESD clamp circuit [15], the drain current, and the gate current flowing through the clamp device $\mathrm{M_{ESD}}$ under the normal power-on transition.

induce a large gate leakage current from node A to VSS in nanometer CMOS technology. A voltage drop across resistor R is generated, and therefore, the pMOS Mp cannot be completely turned off. The voltage of node B would be elevated to a level higher than VSS due to the non-turned-off pMOS Mp. Finally, the main ESD clamp device $(\mathrm{M_{ESD}})$ drawn with large device dimensions and operated in the subthreshold region will further generate a huge leakage current from VDD to VSS under the normal circuit operating condition.

The simulated voltages on the nodes of the traditional RC-based power-rail ESD clamp circuit and the gate current of the MOS capacitor Mc under the normal power-on condition with a rise time of 1 ms in a 65-nm CMOS process are shown in Fig. 1. The dimensions of R, Mc, Mp, Mn, and $\mathrm{M_{ESD}}$ are 165.3 kΩ, 64 μm/2 μm, 184 μm/60 nm, 36 μm/60 nm, and 2000 μm/0.1 μm, respectively. In Fig. 1, the gate leakage current of Mc is 1.65 μA and the voltage of node A is only 0.72 V when VDD is raised up to 1 V. Therefore, a leakage current path is generated from VDD through the inverter (Mp and Mn) to VSS. Consequently, the main ESD clamp device $\mathrm{M_{ESD}}$ operated in the subthreshold region will contribute another leakage current of 0.98 μA under the normal circuit operating condition.

B. Capacitor-Less Design of Power-Rail ESD Clamp Circuit

The capacitor-less design of the power-rail ESD clamp circuit was also proposed to protect the core circuits [15], as shown in the inset of Fig. 2. Under the normal circuit operating condition, the ESD clamp device $\mathrm{M_{ESD}}$ drawn with large device dimensions will induce a large gate current from the drain terminal to node B and a subthreshold channel current in $\mathrm{M_{ESD}}$ from the drain to the source in nanometer CMOS technology. The voltage drop across resistor Rp can be designed smaller to keep the nMOS Mn in the OFF state, and therefore, the pMOS Mp can be virtually turned off. Consequently, the ESD detection circuit can be almost turned off. However, the main ESD clamp device $\mathrm{M_{ESD}}$ drawn with large device dimensions always contributes a large standby leakage current under the normal circuit operating condition.

TABLE I
DEVICE DIMENSIONS OF THE CONVENTIONAL POWER-RAIL ESD CLAMP CIRCUITS

Device	Traditional RC-Based Power-Rail ESD Clamp Circuit	Capacitor-Less Design of Power-Rail ESD Clamp Circuit [15]
Capacitor (Mc)	64μm / 2μm (W/L)	none
Resistor (Ω)	R = 165.3k	Rn = 40k ; Rp = 20k
PMOS Transistor (Mp)	184μm / 60nm	24μm / 60nm
NMOS Transistor (Mn)	36μm / 60nm	12μm / 60nm
ESD Clamp NMOS Transistor ($\mathrm{M_{ESD}}$)	2000μm / 100nm	2000μm / 100nm
Diodes (Dn1 and Dn2)	none	0.057μm^2
Total Layout Area	82.5x60μm^2	58x60μm^2

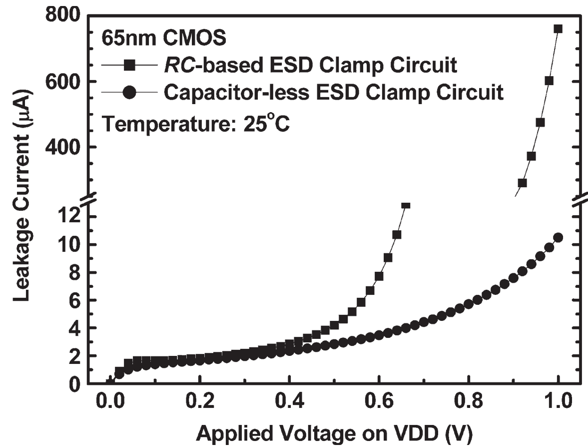


Fig. 3. Measured standby leakage currents of the traditional RC-based and the capacitor-less power-rail ESD clamp circuits.

The simulated voltages on the nodes of the capacitor-less power-rail ESD clamp circuit under the normal power-on condition with a rise time of 1 ms in a 65-nm 1-V CMOS process are shown in Fig. 2. The gate and drain currents of the ESD clamp device $\mathrm{M_{ESD}}$ are also shown in Fig. 2. The dimensions of Rp, Rn, Mp, Mn, and $\mathrm{M_{ESD}}$ are 20 kΩ, 40 kΩ, 24 μm/60 nm, 12 μm/60 nm, and 2000 μm/0.1 μm, respectively. The p$^+$-junction areas of diodes Dn1 and Dn2 are both 0.057 μm^2. In Fig. 2, the gate current of $\mathrm{M_{ESD}}$ is 1.70 μA and the voltage of node B is 0.05 V when VDD is raised up to 1 V. The voltage of node B is not enough to turn Mn on. Therefore, the voltage drop across Rn is only about 2 mV, and the ESD detection circuit can be almost turned off. However, there is still a leakage current path from VDD through the main ESD clamp device $\mathrm{M_{ESD}}$ to VSS. As shown in Fig. 2, the drain current of $\mathrm{M_{ESD}}$ is as large as 9.83 μA, which is the major source of the total standby leakage current.

The device dimensions and the total layout areas of the traditional RC-based and the capacitor-less power-rail ESD clamp circuits fabricated in a 65-nm CMOS process are listed in Table I. The measured standby leakage currents at room temperature are shown in Fig. 3. The applied voltage on VDD is from 0 to 1 V with a voltage step of 20 mV. When VDD is 1 V, the measured standby leakage currents of the RC-based and capacitor-less power-rail ESD clamp circuits are 760.42 and 10.48 μA, respectively. The standby leakage currents of the traditional RC-based and the capacitor-less power-rail ESD clamp circuits under different temperatures are also listed in Table II. We can observe that the MOS transistor drawn with large device

TABLE II
LEAKAGE CURRENTS OF THE CONVENTIONAL POWER-RAIL ESD CLAMP CIRCUITS UNDER DIFFERENT TEMPERATURES AT 1 V IN A 65-nm CMOS PROCESS

Standby Leakage Current at 1V Normal Operating Voltage	Traditional RC-Based Power-Rail ESD Clamp Circuit	Capacitor-Less Design of Power-Rail ESD Clamp Circuit [15]
25ºC	760.42μA	10.48μA
50ºC	12.62mA	32.24μA
100ºC	85.02mA	360.48μA

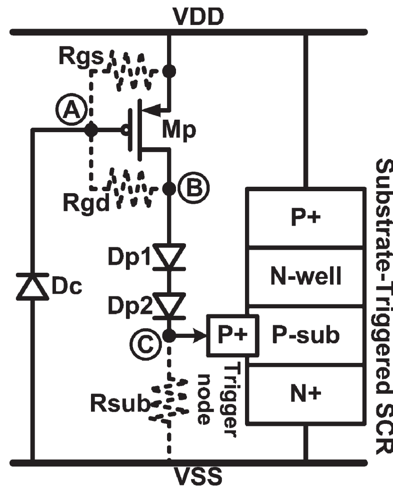


Fig. 4. Proposed resistor-less ESD detection circuit with the p-type substrate-triggered SCR device as the ESD clamp device.

dimensions as the ESD clamp device would be too leaky in nanometer CMOS technology, which is not suitable for portable products with the requirement of low power consumption.

III. Resistor-Less Design of ESD Detection Circuit

A. Circuit Schematic

The resistor-less design of the power-rail ESD clamp circuit is shown in Fig. 4 with the p-type triggered silicon-controlled rectifier (SCR) device as the main ESD clamp device. The SCR device [16] adopted as the main ESD clamp device can avoid the gate leakage current issue due to the non-poly-gate structure inside the SCR device. However, the ESD detection circuit is necessary to enhance the turn-on speed of the SCR device under the ESD stress condition. The new proposed ESD detection circuit is designed with considerations of the gate leakage current and gate oxide reliability. By inserting a diode in the ESD detection circuit, the voltage differences across the gate oxide of the pMOS transistor can be intentionally reduced. By using the gate leakage current of the pMOS transistor, the induced equivalent resistors can be part of the ESD detection mechanism. Therefore, the gate leakage current of the pMOS transistor can be well utilized to achieve the resistor-less design of the ESD detection circuit.

Under the normal circuit operating condition, Mp is kept off, and node C is kept at VSS through the parasitic p-substrate resistor Rsub. Therefore, the p-type triggered SCR device is turned off during the normal circuit operating condition. The RC-based ESD-transient detection mechanism is realized by the equivalent resistors (Rgs and Rgd) of Mp and the junction

TABLE III
DESIGN PARAMETERS OF THE RESISTOR-LESS DESIGN OF THE POWER-RAIL ESD CLAMP CIRCUIT

Device	Size								
Dp1 and Dp2 (μm²)	14								
Dc (μm²)	52.13			54.79			60.13		
Mp Width (μm)	35			70			140		
SCR Width (μm)	25	35	45	25	35	45	25	35	45

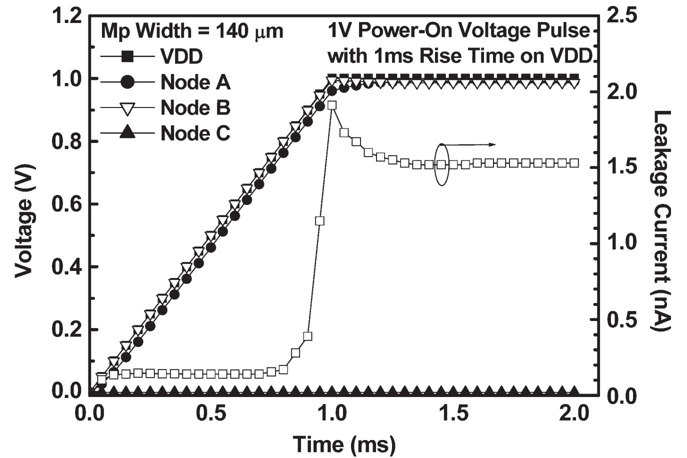


Fig. 5. Simulated voltage waveforms on the nodes and the leakage current of the proposed ESD detection circuit under the normal power-on transition with a VDD of 1 V and a rise time of 1 ms in a 65-nm 1-V CMOS process.

capacitance of the reverse-biased diode Dc, which can distinguish the ESD stress event from the normal power-on condition. In Fig. 4, the pMOS Mp is mainly used to generate the trigger current into the trigger node (node C in Fig. 4) of the p-type triggered SCR device during the ESD stress event. Compared to the MOS capacitor with thin gate oxide in the traditional RC circuit, the Dc used as capacitor in the proposed ESD detection circuit to realize the RC time constant can be free from the gate leakage current issue. The inserted diodes Dp1 and Dp2 in the ESD detection circuit are used to reduce the voltage differences across the gate oxide of Mp. Therefore, the total leakage current and gate oxide reliability of Mp can be safely relieved.

B. Operation Under Normal Power-On Transition

Under the normal circuit operation condition, the gate voltage of Mp (node A in Fig. 4) is biased at VDD through the resistors Rgs and Rgd induced by the gate leakage current. The cathode of Dp2 (node C) is simultaneously biased at VSS through the parasitic p-substrate resistor Rsub in the p-type triggered SCR device. Because Mp is kept off, no trigger current is generated into the trigger node of the p-type triggered SCR device. According to the normal circuit operation voltage, inserting two diodes (Dp1 and Dp2) in the ESD detection circuit can raise the voltage of node B to a voltage level near VDD. Therefore, all terminals of Mp are almost at the same voltage level of VDD to reduce its gate leakage current.

With the SPICE parameters provided from foundry and the device sizes listed in Table III (adopting an Mp width of 140 μm), the simulated voltage waveforms and the leakage current of the proposed ESD detection circuit during the normal power-on transition are shown in Fig. 5. In Fig. 5, the voltage of

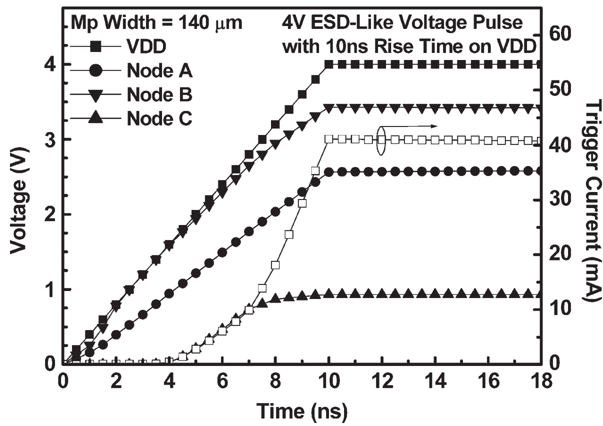


Fig. 6. Simulated voltage waveforms on the nodes and the trigger current of the proposed ESD detection circuit under the ESD-like transition with a VDD of 4 V and a rise time of 10 ns in a 65-nm 1-V CMOS process.

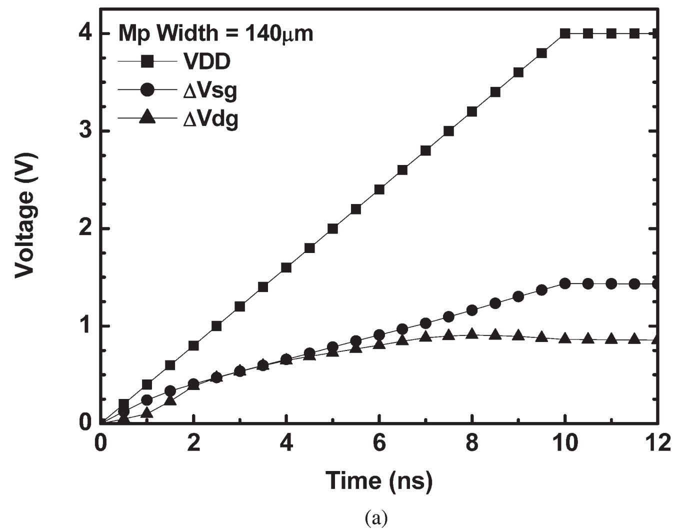
node A is successfully charged to the voltage level of VDD due to the gate leakage current. Therefore, Mp is completely turned off, and the simulated standby leakage current of the proposed ESD detection circuit is only 1.53 nA when VDD is raised up to 1 V.

C. Operation Under ESD Transition

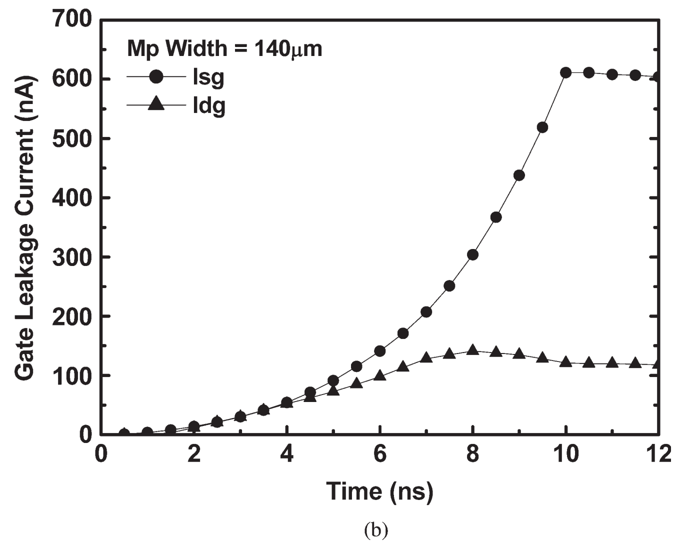
When a positive fast-transient ESD-like voltage is applied to VDD with VSS grounded, the RC time delay keeps node A at a relatively low voltage level as compared with that at VDD. The RC time delay is consisted by the equivalent resistors, which are induced by the gate leakage currents of Mp, and the reverse-biased diode Dc. Consequently, Mp can be quickly turned on to generate the trigger current into the trigger node (node C) of the p-type triggered SCR device.

In order to simulate the fast-transient edge of the human-body-model (HBM) ESD event [17] before the breakdown on the internal devices, a 4-V voltage pulse with a rise time of 10 ns is applied to VDD. The simulated transient voltage and the trigger current of the ESD detection circuit during such an ESD-like transition are shown in Fig. 6. Mp is successfully turned on to generate a trigger current of $\sim$41 mA into the p-type triggered SCR device. Therefore, the SCR device can be fully triggered on to discharge the ESD current from VDD to VSS.

According to the simulated results in Fig. 6, the voltages across the source to the gate and across the drain to the gate ($\Delta\mathrm{Vsg}$ and $\Delta\mathrm{Vdg}$) in time domain are plotted in Fig. 7(a). The corresponding gate leakage currents from the source to the gate and from the drain to the gate (Isg and Idg) in time domain are shown in Fig. 7(b). The gate leakage currents are on the order of nanoamperes. By using Ohm's law, the equivalent resistances ($\mathrm{Rgs} = \Delta\mathrm{Vsg}/\mathrm{Isg}$ and $\mathrm{Rgd} = \Delta\mathrm{Vdg}/\mathrm{Idg}$) can be extracted from the voltage differences and the corresponding gate leakage currents, as shown in Fig. 7(c). During the period of ESD-like transition, the minimum values of Rgs and Rgd are 2.35 and 6.43 MΩ, respectively. With these large intrinsic equivalent resistors induced by the gate leakage current of Mp, the RC time delay can be achieved by adopting a small-size reverse-biased diode Dc to reduce the layout area of the proposed ESD detection circuit.



(a)



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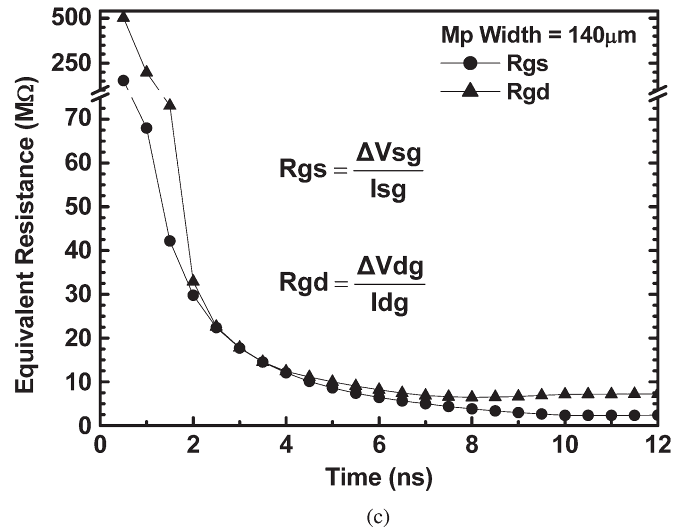


(c)

Fig. 7. Simulated values of (a) $\Delta\mathrm{Vsg}$ and $\Delta\mathrm{Vdg}$ and (b) Isg and Idg and (c) the extracted equivalent resistances of Rgs and Rgd under the ESD-like transition.

IV. Experimental Results

The resistor-less power-rail ESD clamp circuits with different device sizes have been fabricated in a 65-nm 1-V CMOS

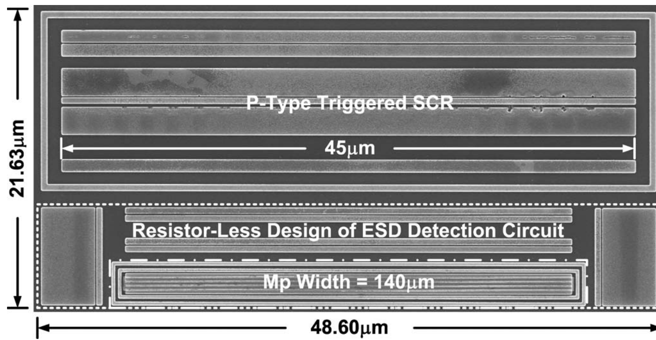


Fig. 8. Chip microphotograph of the fabricated power-rail ESD clamp circuit realized with the resistor-less design of the ESD detection circuit.

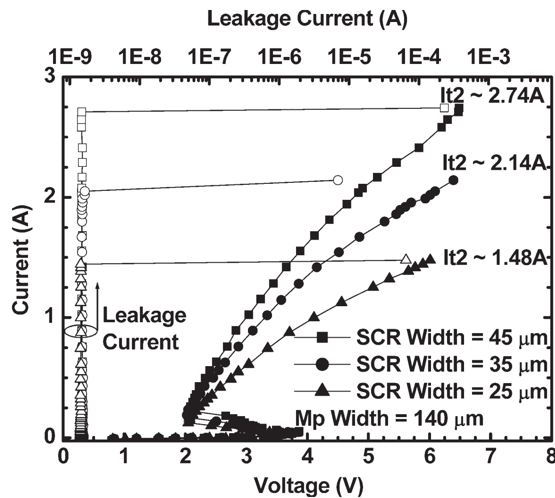


Fig. 9. TLP-measured I–V curves of the power-rail ESD clamp circuits with the resistor-less design of the ESD detection circuit.

process, as shown in Fig. 8. All devices in the proposed design are 1-V fully silicided devices, including the SCR device. The total layout area of the proposed power-rail ESD clamp circuit with an SCR width of 45 μm is 21.63×48.60 μm^2. The widths of the SCR devices are split into 25, 35, and 45 μm to verify the corresponding ESD robustness. The gate widths of Mp are split into 35, 70, and 140 μm to investigate the trigger voltage of the proposed power-rail ESD clamp circuit. These power-rail ESD clamp circuits are prepared for the measurements by transmission line pulsing (TLP), ESD test, dc I–V curve, and transient behavior.

A. TLP Measurement and ESD Robustness

A TLP generator with a pulsewidth of 100 ns and a rise time of $\sim$2 ns is used in this measurement [18]. The TLP-measured I–V curves of the new proposed power-rail ESD clamp circuits with different SCR widths are shown in Fig. 9, where the device dimension of Mp is kept at 140 $\mu\text{m}/0.12$ μm. The power-rail ESD clamp circuit with SCR widths of 25, 35, and 45 μm can achieve It2 values of 1.48, 2.14, and 2.74 A, respectively. The It2 and the trigger voltage of the power-rail ESD clamp circuit with different SCR widths and different Mp widths are listed in Table IV. As shown in Table IV, the It2 of the proposed power-rail ESD clamp circuit is proportional to the width of the SCR device. The trigger voltages of the proposed power-rail ESD clamp circuits are compared in Fig. 10. As shown in Fig. 10, the trigger voltage can be obviously reduced by increasing the Mp width to generate a larger trigger current. In addition, the SCR device with a small width also has a lower trigger voltage due to the larger parasitic p-substrate resistor Rsub. Therefore, the turn-on speed of the SCR device can be properly adjusted by the dimension of Mp. In Fig. 9, the holding voltages of the SCR devices are $\sim$2 V, which is higher than the VDD of 1 V under the normal circuit operation condition. Therefore, the proposed power-rail ESD clamp circuits are free from the latchup issue for 1-V applications [19], [20].

The measured HBM and machine-model (MM) [21] ESD levels of the proposed power-rail ESD clamp circuit under positive VDD-to-VSS ESD stress are also listed in Table IV. The measured HBM (MM) ESD levels of the SCRs with widths of 25, 35, and 45 μm are 3, 4, and 5 kV (200, 300, and 400 V), respectively. The measured HBM and MM ESD levels of the proposed power-rail ESD clamp circuits are also proportional to the width of the SCR device.

In a nanoscale CMOS process, the application of automotive electronics is increasingly important for driving safety. In order to meet the high-reliability need of automotive electronics, typically 8-kV HBM ESD level [22], the device width of an SCR can be appropriately enlarged. Because the SCR can be uniformly triggered by the trigger current generated from an independent ESD-transient detection circuit, the measured It2 and ESD levels as shown in Table IV are well proportional to the SCR width. Therefore, the proposed power-rail ESD clamp circuit with an enlarged SCR device width can sustain high-enough HBM ESD levels to meet the application requirement of automotive electronics.

B. Leakage Measurement

The dc I–V curves of the fabricated power-rail ESD clamp circuits are measured by HP4155 from 0 to 1 V with a voltage step of 20 mV at 25 °C, as shown in Fig. 11 and listed in Table IV. In Fig. 11, the standby leakage current of the power-rail ESD clamp circuit with an SCR width of 45 μm increases from 1.13 to 1.43 nA under 1-V bias when the width of Mp increases from 35 to 140 μm. In Table IV, the standby leakage currents of the power-rail ESD clamp circuits with SCR widths of 25, 35, and 45 μm are similar, because the leakage current in the SCR device is quite small. The measured standby leakage currents of the fabricated power-rail ESD clamp circuits under 1-V bias at 50 °C and 100 °C are also listed in Table IV. The standby leakage currents of the fabricated power-rail ESD clamp circuits are reduced to the order of nanoamperes because the voltage drop across the gate oxide of Mp is significantly reduced by inserting the reverse-biased diode Dc and the diodes (Dp1 and Dp2) in the ESD detection circuit. Although increasing the width of Mp causes a slightly increased standby leakage current under the normal circuit operating condition, it can increase the trigger current to improve the turn-on speed of the SCR device with a reduced trigger voltage (as shown in Fig. 10).

TABLE IV
MEASURED RESULTS OF THE PROPOSED POWER-RAIL ESD CLAMP CIRCUITS

Mp Width (μm)		35			70			140		
SCR Width (μm)		25	35	45	25	35	45	25	35	45
It2		1.48A	2.17A	2.74A	1.48A	2.11A	2.71A	1.48A	2.14A	2.74A
Trigger Voltage		4.26V	4.71V	5.17V	3.79V	4.02V	4.26V	3.60V	3.75V	3.86V
HBM ESD Level		3kV	4kV	5kV	3kV	4kV	5kV	3kV	4kV	5kV
MM ESD Level		200V	300V	400V	200V	300V	400V	200V	300V	400V
Leakage Current (@ 1V)	25°C	1.12nA	1.12nA	1.13nA	1.31nA	1.31nA	1.32nA	1.43nA	1.43nA	1.43nA
	50°C	6.69nA	6.80nA	6.84nA	8.18nA	8.48nA	8.65nA	12.13nA	12.55nA	12.62nA
	100°C	0.19μA	0.19μA	0.19μA	0.26μA	0.26μA	0.26μA	0.33μA	0.33μA	0.33μA

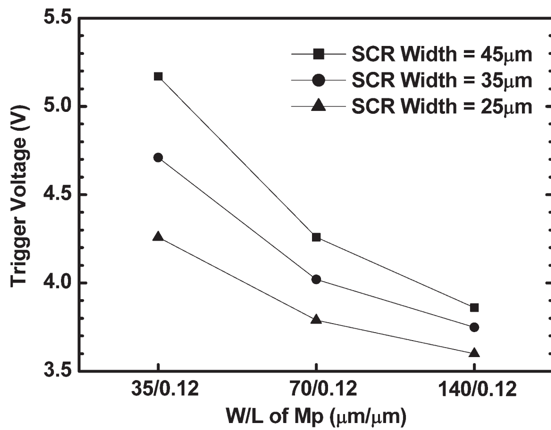


Fig. 10. Dependence of the TLP-measured trigger voltages on the device dimension of Mp.

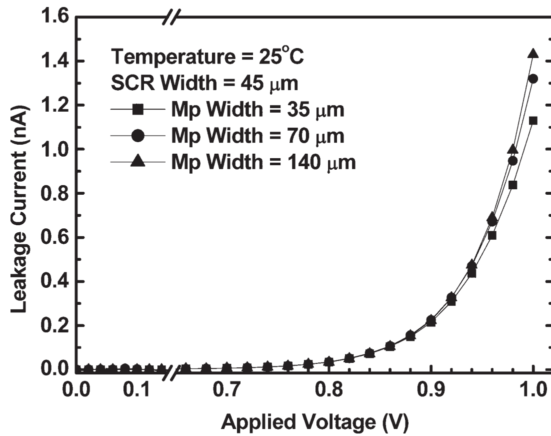
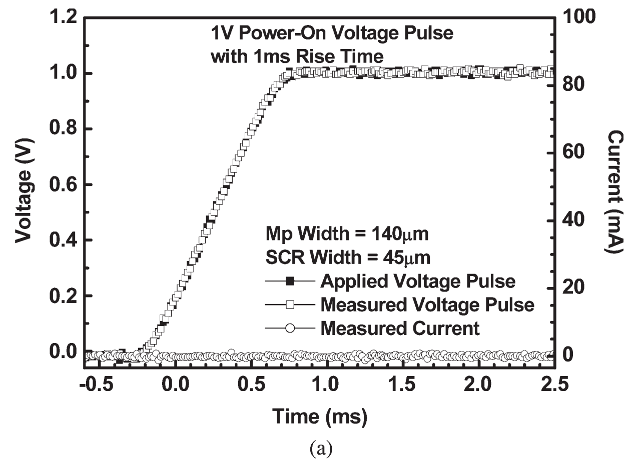
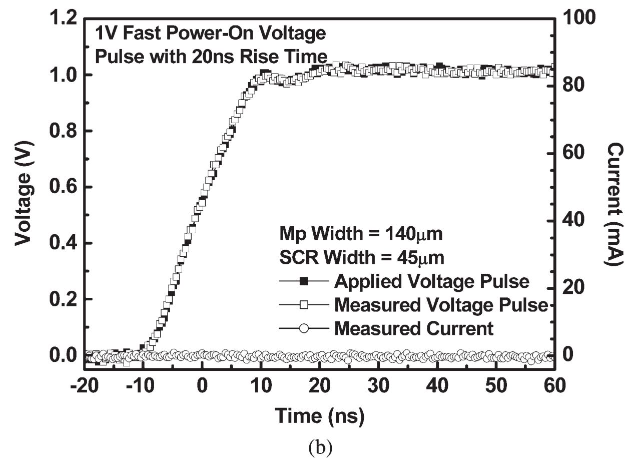


Fig. 11. Measured dc I–V curves of the fabricated power-rail ESD clamp circuits with different widths of Mp at room temperature.



(a)



(b)

Fig. 12. Measured transient voltage and current waveforms of the fabricated power-rail ESD clamp circuit under the 1-V power-on transition with rise times of (a) 1 ms and (b) 20 ns.

C. Turn-On Verification

For normal power-on condition, the voltage pulse usually has a rise time on the order of milliseconds. As shown in Fig. 12(a), the measured voltage on the VDD power line rises up to 1 V, and the measured current is near zero. However, some previous studies [8], [23] have demonstrated that power-rail ESD clamp circuits with RC-based ESD detection circuits were easily mistriggered or into the latch-on state under the fast power-on condition. The new proposed power-rail ESD clamp circuits have been applied with a 1-V voltage pulse with 20-ns rise time to investigate their immunity against mistrigger, as shown in Fig. 12(b). The measured voltage on the VDD power line is not degraded under the fast power-on condition. The measured current waveform is also smooth at the level near zero. The two diodes (Dp1 and Dp2) inserted in the ESD detection circuit can ensure that there would not be any on-current flowing through them from VDD to VSS. Therefore, the resistor-less design of the ESD detection circuit is free from transient-induced latch-on or mistrigger issues.

The transient voltage with a pulse height of 4 V and a rise time of 10 ns is applied to the VDD power line with 1-V

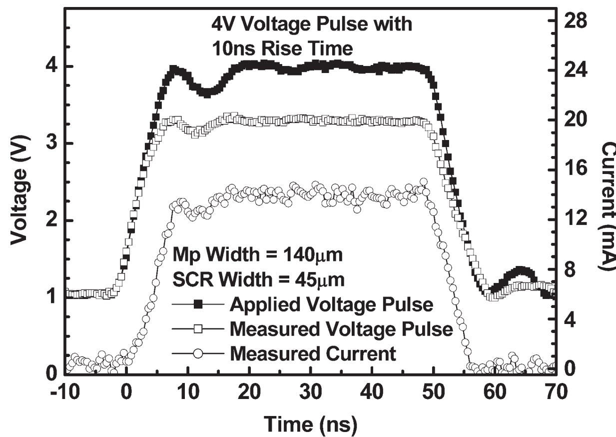


Fig. 13. Measured voltage and current waveforms of the power-rail ESD clamp circuit realized with the resistor-less design of the ESD detection circuit under transient noise condition.

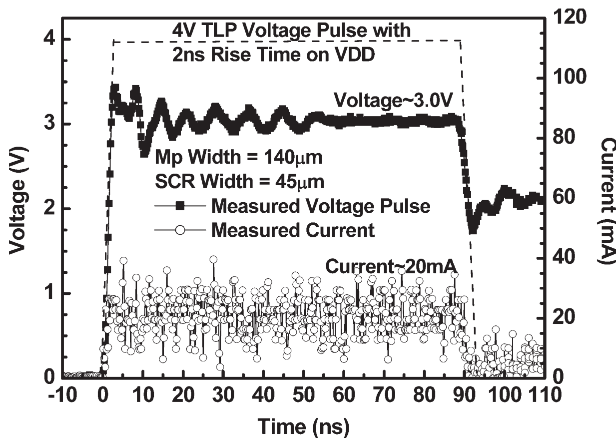


Fig. 14. Measured voltage and current waveforms of the power-rail ESD clamp circuit realized with the resistor-less design of the ESD detection circuit under TLP transition with a 4-V voltage pulse.

operation voltage to verify any latch-on issue. As shown in Fig. 13, the transient voltage pulse will activate the ESD detection circuit to generate a trigger current of $\sim$14 mA. The applied 4-V voltage pulse is clamped down to a lower voltage level of $\sim$3.3 V by the proposed power-rail ESD clamp circuit. After the transient, the voltage on the VDD power line is back to a 1-V operation voltage, and the current is almost zero.

In order to observe the transient behavior of the proposed ESD detection circuit, a TLP voltage pulse with a rise time of 2 ns and a pulse height of 4 V is applied to the VDD power line with the VSS grounded. The TLP voltage pulse will initiate the ESD detection circuit to generate the trigger current to trigger on the SCR device. The measured voltage and current waveforms in time domain on the VDD power line under a 4-V voltage pulse are shown in Fig. 14. The applied 4-V voltage pulse can be quickly clamped down to a lower voltage level of $\sim$3.0 V by the proposed ESD detection circuit with a trigger current of $\sim$20 mA. When the TLP voltage pulse height is increased, the proposed ESD detection circuit can generate more trigger currents into the SCR device. The triggered-on SCR device can provide a low-impedance path from VDD to VSS to discharge the ESD current and clamp down the voltage level. Overall, the proposed ESD detection circuit can be successfully activated by the voltage pulse with a fast-transient edge to trigger on the SCR device.

V. Conclusion

The resistor-less design of an ESD detection circuit to achieve ultralow standby leakage current and small layout area has been proposed and successfully verified in a 1-V 65-nm fully silicided CMOS technology. The proposed ESD detection circuit has been realized with only 1-V devices without suffering the gate leakage issue. According to the measured results, the proposed power-rail ESD clamp circuit demonstrates an ultralow standby leakage current of only 1.43 nA under 1-V bias at 25 °C, where the device dimension of Mp is drawn as 140 μm/0.12 μm. Moreover, the proposed power-rail ESD clamp circuit has excellent immunity against transient-induced latch-on or mistrigger issues. The proposed resistor-less power-rail ESD clamp circuit is an excellent circuit solution to achieve effective and efficient on-chip ESD protection in advanced nanoscale CMOS technologies.

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