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Bias-Dependent Radio Frequency Performance for 40 nm InAs High-Electron-Mobility Transistor with a Cutoff Frequency Higher than 600 GHz

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In this paper, we present the fabrication and characterization of 40 nm InAs-channel high-electron-mobility-transistor (HEMT) devices. Both DC and RF measurements were performed under various bias conditions. We have also extracted bias-dependent intrinsic device parameters to determine the optimum conditions of operation. It is concluded that a high current-gain cutoff frequency (f_T) of 615 GHz can be achieved when the device is biased near the occurrence of impact ionization. © 2012 The Japan Society of Applied Physics

The InAs/$In_xGa_{1-x}As$ high-electron-mobility transistor (HEMT) with high indium content in the channel is an important device for future low-power, high-frequency, and low-noise applications.[1)] In fact, the device is an excellent choice for operation in the terahertz (THz) regime. Excellent high-speed and high-frequency performances of In-rich $In_xGa_{1-x}As$-channel HEMTs with ultrashort gate length have been reported over the past decade.[2–5)] The improvement of current gain cutoff frequency (f_T) towards the THz range has become possible by combining suitable materials and device technologies, such as high-mobility channel materials, vertical and lateral scaling, and optimization of device structure to minimize the parasitics.

Despite all the excellent features provided, the determination of the optimum bias condition for such a narrow energy band gap of high-indium-content channel devices ($In_{0.53}Ga_{0.47}As$: 0.72 eV, InAs: 0.36 eV) has been a critical issue, since the occurrence of impact ionization under high drain bias causes performance degradation.[6,7)] Devices suffer from a severe current–voltage (I–V) kink effect, high output conductance, current instability, high gate current, low breakdown voltage, and excess channel noise once impact ionization occurs.[8,9)]

In this study, we carefully examined the effect of impact ionization on 40 nm InAs-channel HEMTs under different drain bias conditions. We observed that a high f_T of 615 GHz could be achieved when the device was biased prior to the occurrence of impact ionization. Further increase in drain bias leads to the increase in total gate capacitance owing to impact ionization, which causes degradation in f_T.

The epitaxial layer structure of the InAs thin-channel device was grown by molecular beam epitaxy (MBE) on a 3-in. InP substrate, as shown in Fig. 1. The channel consists of a trilayer of $In_{0.53}Ga_{0.47}As$, InAs, and $In_{0.53}Ga_{0.47}As$ with thicknesses, from bottom to top, of 3, 5, and 2 nm. The measured room-temperature two-dimensional electron gas (2DEG) density and electron mobility were 4.34×10^{12} cm^{-2} and 12,000 $cm^2 V^{-1} s^{-1}$, respectively.

For device fabrication, mesa isolation was carried out by wet etching and a low contact resistance of the alloyed Au/Ge/Ni/Au source and drain ohmic contact with 2 μm spacing was attained. Gate recessing was performed in three different stages, as illustrated in our earlier work.[10)] After E-beam exposure, the two-step recess method and Pt-buried gate were adopted to further recess the 2DEG channel and mitigate the short-channel effects. A 60-nm-thick silicon nitride was deposited as the passivation layer by plasma enhanced chemical vapor deposition (PECVD). The inset of Fig. 1 is the scanning electron microscope (SEM) image of the 40 nm T-shaped gate after SiN_x passivation.

Figure 2(a) shows the DC I_{DS} versus V_{DS} curves of the fabricated $0.04 \times 100\,\mu m^2$ device. High transistor drive current was observed at a low drain bias of 0.5 V as a result of the superior electron mobility and conductivity in the InAs channel. An increase in the drain current at a constant slope is clearly observed when V_{DS} is high. Figure 2(b) shows the DC transconductance (g_m) as a function of gate bias with different drain biases from 0.5 to 1 V. The increase in the peak g_m with drain bias at a specific gate bias is mainly due to the generation of additional electron–hole pairs in the channel, which is also an indication of the occurrence of impact ionization.

Figure 2(c) shows the measured total gate current under different bias conditions. Note that the gate remained reverse biased when varying the drain bias. The total gate current includes the Schottky gate leakage current and the induced hole current due to impact ionization.[11)] The characteristic hump in the curves for V_{DS} higher than 1.0 V indicates the occurrence of the impact ionization that occurs when a large number of electron–hole pairs are generated in the channel and a high electric field intensity exists near the drain area, causing hole injection into the gate even when the gate is reverse biased.[11)] The impact ionization can occur only when both the carrier concentration in the channel and the electric field between the drain and gate are high. The electron–hole pairs are then generated in the high-field region between the gate and drain, and some of the holes will be collected by the negatively biased gate. A plot of the gate current due to impact ionization, I_{Gii}, as a function of V_{GS} with various V_{DS} is included in Fig. 2(d). We obtained I_{Gii} by subtracting the Schottky current from the total gate current following the standard extraction procedure.

The high-frequency performance of the device was characterized through S-parameter measurement over a frequency range of 1 to 80 GHz using an HP 8510 XF vector network analyzer. The current gain (H_{21}), maximum stable gain (MSG), Mason's unilateral gain (U), and the stability factor (K) after the removal of parasitics as a function of

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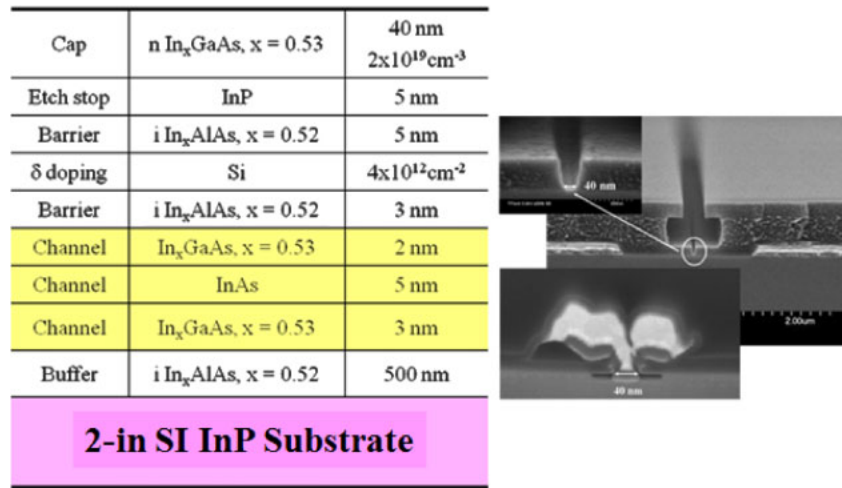

Cap	n In$_x$GaAs, x = 0.53	40 nm 2x10^{19}cm^{-3}
Etch stop	InP	5 nm
Barrier	i In$_x$AlAs, x = 0.52	5 nm
δ doping	Si	4x10^{12}cm^{-2}
Barrier	i In$_x$AlAs, x = 0.52	3 nm
Channel	In$_x$GaAs, x = 0.53	2 nm
Channel	InAs	5 nm
Channel	In$_x$GaAs, x = 0.53	3 nm
Buffer	i In$_x$AlAs, x = 0.52	500 nm
2-in SI InP Substrate		

Fig. 1. (Color online) Schematic of 40 nm InAs-channel HEMTs. The inset is an SEM image of the 40 nm T-shaped gate.

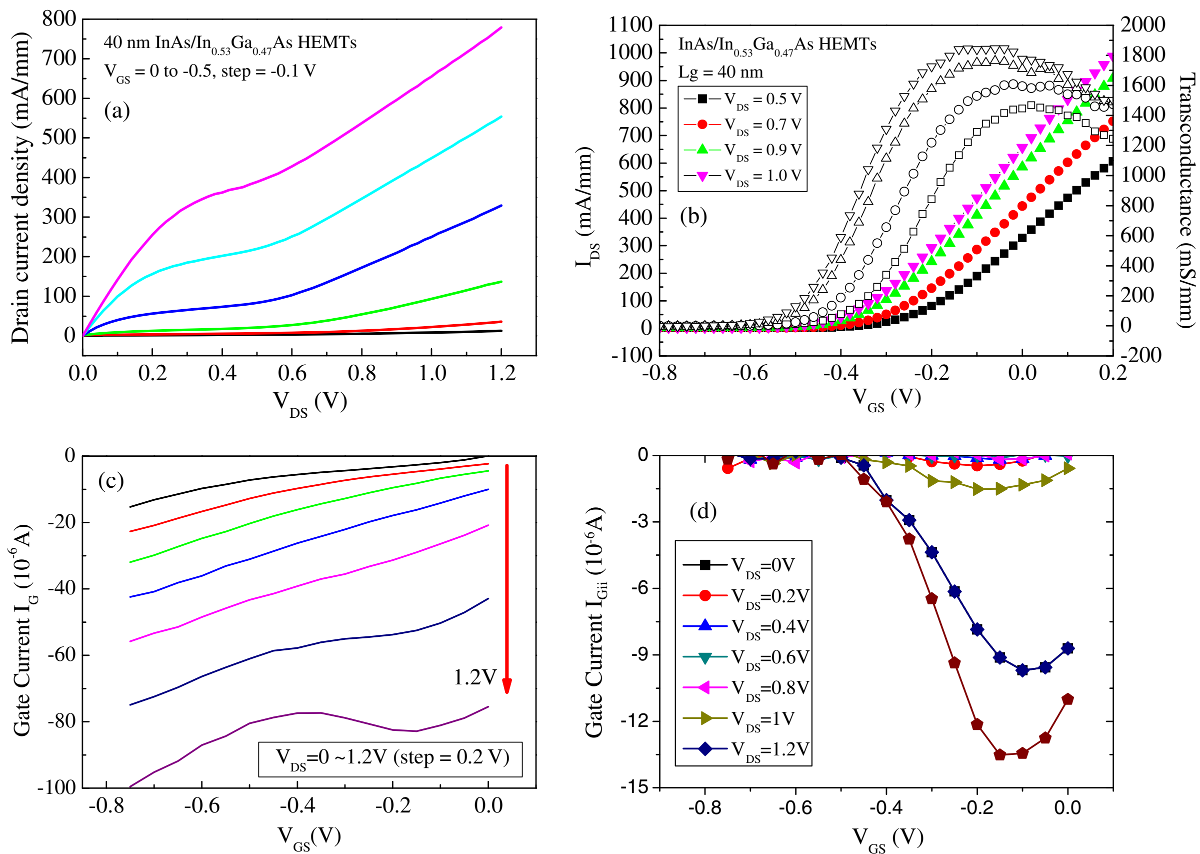

Fig. 2. (Color online) (a) Drain–source current versus drain–source voltage. (b) Transfer and g_m characteristics of InAs-channel HEMTs. (c) Gate leakage current of InAs/In$_{0.53}$Ga$_{0.47}$As composite channel HEMTs as a function of gate voltage at different drain biases. (d) Extracted gate current due to impact ionization as a function of gate voltage at different drain bias.

frequency are plotted in Fig. 3 at a drain bias of 0.9 V with the gate bias set at peak g_m close to 0 V. The parasitic pad capacitance was extracted through the *S*-parameter measurement of open pads and converted to the *Y*-parameters. To guarantee the accuracy of the extracted device performances, the open-pad test structure was measured before and after measuring the working devices, and it was confirmed that the difference between the two measured capacitances was small. For our specific device layout, the parasitic pad capacitances at the gate side and drain side were extracted as 11.3 and 9.5 fF, respectively. The current-gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) of 615 and 430 GHz, respectively, were extracted by extrapolating H_{21} and MAG/MSG with a −20 dB/decade slope. Figure 4 shows the dependence of f_T and f_{max} on the drain bias when the gate was biased at peak g_m. It is observed that the extracted f_T increases as V_{DS} increases from 0.5 to 0.9 V and starts to decrease at $V_{DS} = 1$ V, where impact ionization

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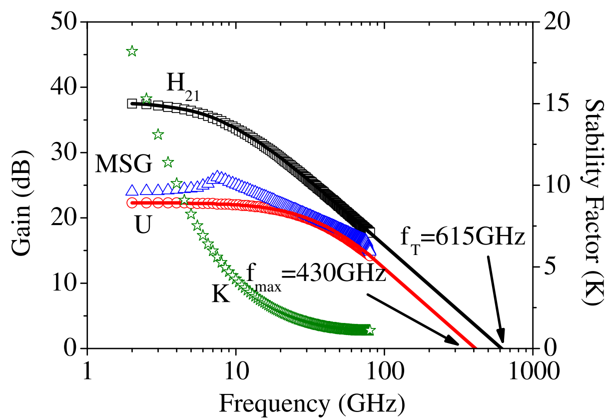

Fig. 3. (Color online) Current gain (H_{21}), maximum stable gain (MSG), Mason's unilateral gain (U), and stability factor (K) as functions of frequency ranging from 1 to 80 GHz at $V_{DS} = 0.9$ V.

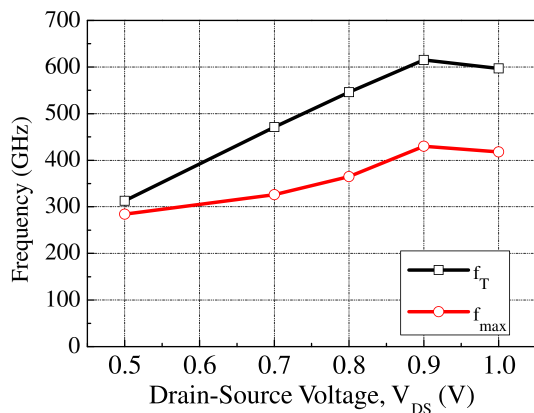

Fig. 4. (Color online) Dependence of f_T and f_{max} on drain bias when the gate is biased at peak g_m.

begins. Note that the gate biases have been set at peak DC g_m for all cases. Figure 5 shows plots of the two key parameters determining f_T, RF g_m and total gate capacitance, as functions of V_{DS} when the gate biases were set at peak DC g_m. We observe a significant increase in RF g_m with low V_{DS}, and the increase is not as drastic beyond 0.7 V. On the other hand, a slight decreasing trend of total gate capacitance with respect to the drain bias is observed before the onset of impact ionization. One of the contributing factors is the decrease in gate-to-drain capacitance (C_{GD}) owing to the widening of the depletion region as V_{DS} increases. Once V_{DS} increases beyond 0.9 V, a slight increase in the total gate capacitance occurs mainly because of the large numbers of excess charge carriers caused by impact ionization. Such an increase in the total gate capacitance leads to the slight decrease in f_T shown in Fig. 4. We can thus conclude that for such low-band-gap devices, maximum f_T can be obtained

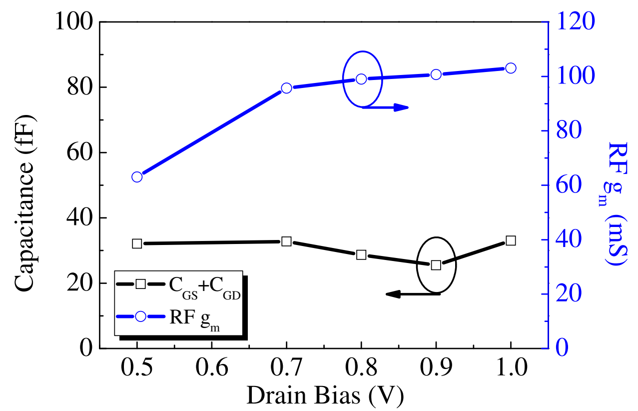

Fig. 5. (Color online) Extracted gate-to-source capacitance, gate-to-drain capacitance, and RF g_m versus drain voltage.

when the device is biased near the occurrence of impact ionization.

In conclusion, we fabricated the 40 nm InAs-channel HEMT device and characterized its performance. The device showed a high f_T of 615 GHz when biased near the occurrence of impact ionization. Further increase of the drain bias degrades the RF performance owing to large numbers of excess charge carriers in the channel generated by impact ionization. Therefore, under optimum bias conditions, such InAs devices show tremendous potential for future submillimeter wave applications.

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1) A. Tessmann, A. Leuther, H. Massler, V. Hurm, M. Kuri, M. Zink, M. Riessle, and R. Losch: IEEE MTT-S Int. Microw. Symp. Dig., 2010, p. 53.
2) A. Leuther, S. Koch, A. Tessmann, I. Kallfass, T. Merkle, H. Massler, R. Loesch, M. Schlechtweg, S. Saito, and O. Ambacher: Proc. 23rd Int. Conf. Indium Phosphide and Related Materials, 2011, p. 1.
3) S. J. Yeon, M. Park, J. Choi, and K. Seo: IEDM Tech. Dig., 2007, p. 613.
4) D. H. Kim and J. A. del Alamo: IEEE Electron Device Lett. **31** (2010) 806.
5) D. H. Kim, B. Brar, and J. A. del Alamo: IEDM Tech. Dig., 2011, p. 319.
6) C. Y. Chang, H. T. Hsu, E. Y. Chang, C. I. Kuo, S. Datta, M. Radosavljevic, Y. Miyamoto, and G. W. Huang: IEEE Electron Device Lett. **28** (2007) 856.
7) A. A. Moolji, S. R. Bahl, and J. A. del Alamo: IEEE Electron Device Lett. **15** (1994) 313.
8) H. Wang, Y. Liu, R. Zeng, and C. L. Tan: Appl. Phys. Lett. **90** (2007) 103503.
9) W. Kruppa and J. B. Boos: IEEE Trans. Electron Devices **42** (1995) 1717.
10) C. I. Kuo, H. T. Hsu, C. Y. Wu, E. Y. Chang, Y. L. Chen, and W. C. Lim: Microelectron. Eng. **87** (2010) 2625.
11) R. T. Webster, S. Wu, and A. F. M. Anwar: IEEE Electron Device Lett. **21** (2000) 193.

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