A Near-Optimum Dynamic Voltage Scaling (DVS) in 65-nm Energy-Efficient Power Management With Frequency-Based Control (FBC) for SoC System

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***Abstract*—A 65-nm energy-efficient power management with frequency-based control (FBC) is proposed to achieve the near-optimum dynamic voltage scaling (DVS) in a system-on-chip system. Since DVS and dynamic frequency scaling (DFS) operations are demanded for system processor, control loop of the proposed single-inductor dual-output (SIDO) power module is merged with the frequency-controlled phase-locked loop (PLL) to constitute the operation of hybrid control loop. This means that both DVS and DFS operations can be guaranteed and are not affected by process, supply voltage, and temperature variations. The proposed power management can receive the demand of system processor by hybrid control loop and can help realize the supply voltage with different operation tasks for near-optimum DVS operation. The fabricated chip occupies a 1.12-mm^2 silicon area. Experimental results show that the SIDO power module achieves a peak efficiency of 90% and the highest power reduction of 33% with the proposed near-optimum DVS operation.**

***Index Terms*—Dynamic frequency scaling (DFS), dynamic voltage scaling (DVS), frequency-based control (FBC), hybrid control loop, phase-locked loop (PLL), power efficiency, power management, single-inductor dual-output (SIDO) converter.**

I. Introduction

With the rising trend of system-on-chip (SoC) integration, various circuit functions are now required to be merged into a single chip. Since the minimized power consumption has become one of the most important design issues, implementation of embedded power management would affect the entire performance in SoC [1], [2]. A switching regulator is often utilized for the power management module because of its inductor-based energy delivery scheme [3], [4], which is capable of providing large amounts of energy and keeping the relatively high power efficiency compared with linear regulators [5], [6]. Dynamic voltage scaling (DVS) is the commonly used technique for modulating adequate supply voltages in SoC [7]–[9]. Distinct levels of voltage scaling can be used to adjust the variable delay block for achieving dynamic frequency scaling (DFS) operation [10]. This guarantees the proper operation with different operation modes in system processor. Delay-locked loops (DLLs) are also utilized to realize the demanded operation frequency for SoC [11]. Fig. 1 illustrates the conventional DVS and DFS implementations for achieving the demands of system processor. There are two separate control loops, namely, power loop and PLL, used to control the supply voltage $V_{\rm DVS}$ and the operation frequency $F_{\rm DFS}$ for system processor, respectively. There are dual independent power modules generating the two distinct voltage supplies, which are $V_{\rm ANG}$ and $V_{\rm DVS}$ for powering analog circuits and the system processor, respectively. $V_{\rm ANG}$ is kept with a constant value for the noise-sensitive analog circuits in order to ensure their correct functions. Meanwhile, $V_{\rm DVS}$ equips DVS functions with power loop to realize the optimal supply function for the system processor. This means that the supply voltage is raised when the busy execution in system processor is activated, whereas it would be decreased to reduce power consumption when the processor acts with a leisured operation scheme. Therefore, $V_{\rm DVS}$ can be adjusted to an appropriate supply voltage level according to the DVS code, which helps meet the adequate energy demand in the system processor with the distinct operation tasks. Moreover, the operation frequency of the processor is guaranteed through the PLL modulation. The frequency register can indicate the request from the system processor to carry out the distinct operation frequency along with the different operation modes. As a result, DVS and DFS functions can be achieved to ensure the effective SoC performance.

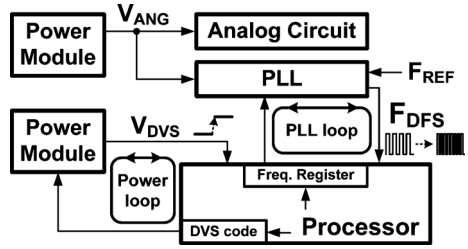

Fig. 1. Conventional DVS and DFS implementation in SoC with the separated control loops and the distinct power modules.

Relationships between $V_{\rm DVS}$ and $F_{\rm DFS}$ are determined by system processor with the different operation modes to achieve the energy-efficient operations. Power scheme of system processor in Fig. 2 indicates the need of both $V_{\rm DVS}$ and $F_{\rm DFS}$ with correspondence of processor's instructions. However, the fabricated process, supply voltage, and temperature (PVT) varia-

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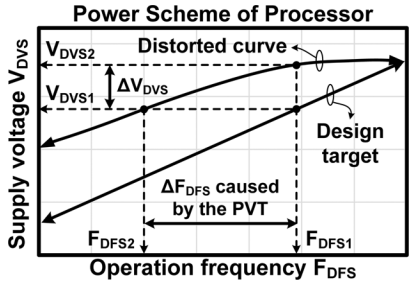


Fig. 2. Relationship between the supply voltage and the operation frequency for system processor with/without the PVT-caused distortion.

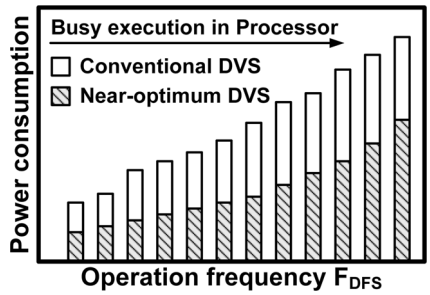


Fig. 3. Illustration of power consumption with the embedded near-optimum DVS power management in SoC.

tions tend to distort the ideal power scheme, causing variations in operation frequency. In turn, these variations deteriorate the performance of system processor. For example, when processor asks the power module to execute the DVS function by providing the supply voltage $V_{\rm DVS1}$, the operation frequency would be obtained as $F_{\rm DFS2}$ due to the supposed distorted curve, rather than the anticipative target of $F_{\rm DFS1}$. This means that the separated control loops are easily affected by PVT variations since the power loop and the PLL are operated by themselves, instead of related to each other. Although the PVT-caused distortion would not extremely deteriorate the existing control scheme due to the closed-loop modulation in each of them, the expected outcome of processor cannot be perfectly assured. Moreover, insufficient operation frequency may lead to the decrease of million instructions per second (MIPS) performance [12], [13] when the processor works with the complicated data execution. Therefore, a correction methodology must be adopted to compensate for this nonideal effect, which can be achieved by adjusting the supply voltage from $V_{\rm DVS1}$ to $V_{\rm DVS2}$ in order to obtain the desired system frequency $F_{\rm DFS1}$ with the distorted curve. Nevertheless, it needs to detect the difference between the inadequate operation frequency and the target value that increases design difficulty and cost due to the extra implementations. As a result, the proposed near-optimum DVS power management is designed to generate the demanded operation frequency and automatically realize the proper supply voltage for system processor. As such, it can generate the identical operation frequency with the distinct PVT conditions and simultaneously provide the different supply voltages.

Power consumption of the system processor with the integrated near-optimum DVS power management is depicted in Fig. 3. As the busy execution is continuously activated in the system processor, the operation frequency $F_{\rm DFS}$ needs to be increased in order to cope with the heavy data executed flow. In conventional DVS implementation with the separated loop modulation, as depicted in Fig. 1, the supply voltage for the system processor is raised to allow high-speed operation scheme. However, to perfectly guarantee the correct functions in all of the operation tasks, supply voltage $V_{\rm DVS}$ will be settled at a relative high value in order to avoid the effect caused by PVT variation. Therefore, it surely deserves the larger power consumption compared with that of the proposed near-optimum DVS operation which can dynamically adjust the supply voltage by using the hybrid control loop to ensure the proper operation scheme in SoC, that is, the correct operation function in SoC systems can be guaranteed, and power consumption can be greatly minimized.

In this paper, the proposed near-optimum DVS with single-inductor dual-output (SIDO) power module is depicted in Section II. Detailed operations of the hybrid control loop are illustrated in Section III. Circuit implementations are described in Section IV. Experimental results are shown in Section V. Finally, a conclusion is made in Section VI.

II. Proposed Near-Optimum DVS With the SIDO Power Module

The proposed near-optimum DVS SIDO power module is realized by the hybrid control loop, which merges power loop and PLL depicted in Fig. 1, to accomplish the request of both operation frequency and supply voltage for system processor. SIDO power module [14]–[19] can be used to generate two independent supply voltages by using only one off-chip inductor. It has the capability of providing dual energy-driving outputs for achieving the compact power management solution in SoC. Ordered power-distributive control shown in [14] reports the control methodology of single-inductor multi-output (SIMO) converter. However, load currents of the comparator-controlled outputs are limited. The last output which is regulated by an error amplifier (EA) needs to operate with the largest load current. Energy distribution can be guaranteed by properly arranging the energy paths for outputs [15], [16]; nevertheless, a step-up regulation path must exist to ensure the stable operation. In addition, to control the energy delivery path in the power stage of SIDO converter, voltage-mode [17] and current-programmed [18], [19] control schemes have also been adopted. Fig. 4 shows the structure of the proposed SIDO power module with near-optimum DVS operation for SoC. There are four power switches, namely, M_{D1} to M_{D4}, that transfer energy from the battery input $V_{\rm BAT}$ to both two outputs $V_{\rm ANG}$ and $V_{\rm DVS}$. Analog circuits in SoC are supplied by the $V_{\rm ANG}$, which provides a constant voltage to ensure correct functions. On the other hand, system processor is powered by the output $V_{\rm DVS}$, which is implemented with a DVS function. The low-dropout (LDO) regulator is put at the output of the SIDO power module $V_{\rm ANG}$ to achieve ripple reduction for the noise sensitive analog subcircuits. $V_{\rm DVS}$ is equipped with the DVS function; therefore, its voltage level becomes varied by utilizing the hybrid control loop, thereby achieving the near-optimum DVS operation. Moreover, both of the output voltages of the SIDO power module are monitored through the voltage divider, which is realized by the resistor string, to feedback the output voltage conditions to the EA and the energy scheme controller. The EA generates the error signals $V_{\rm EA}$ and

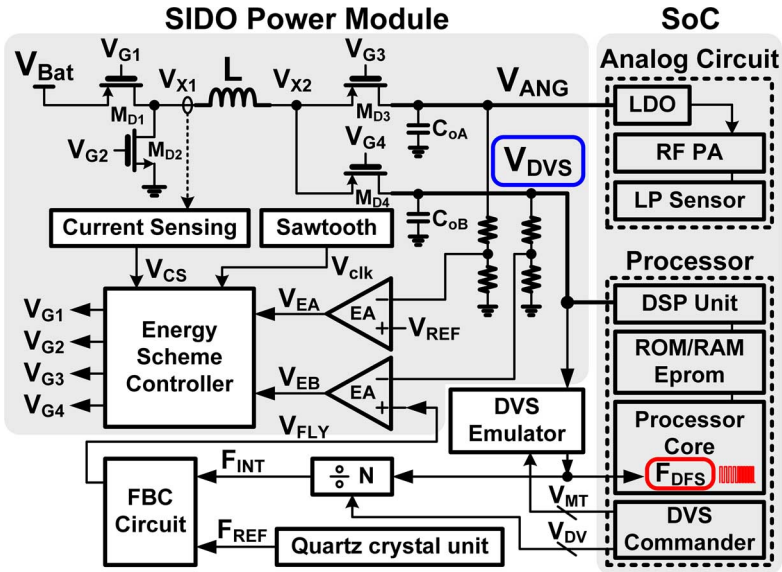


Fig. 4. Structure of the proposed SIDO power module with near-optimum DVS operation.

$V_{\rm EB}$ in response to the load conditions of $V_{\rm ANG}$ and $V_{\rm DVS}$, respectively. Besides, the on-chip compensator can ensure the stability. The current-sensing circuit is implemented with the full-range sensing structure to obtain the exact inductor current information by the signal $V_{\rm CS}$ and determine duty cycles for the two outputs due to the utilization of the current-programmed operation scheme [19]. The sawtooth circuit, meanwhile, generates a fixed frequency $V_{\rm clk}$ to achieve the pulse-width-modulation (PWM) in the SIDO power module. Then, the energy scheme controller produces the control signals V_{G1} to V_{G4} for power switches to form the different energy delivery paths in the power stage. Both outputs will receive energy in every PWM switching cycle and have the proper response. A sensed inductor current can be directly sent to the energy scheme controller to achieve the current-programmed control, which helps realize the energy delivery scheme in the proposed SIDO power module.

The DVS commander in the system processor can send the energy request by the signals $V_{\rm MT}$ and $V_{\rm DV}$ to the DVS emulator and the divider, respectively. It would like to simultaneously guarantee the supply voltage $V_{\rm DVS}$ and the operation frequency $F_{\rm DFS}$ for DVS function and DFS operation, respectively. Therefore, the DVS code for the supply voltage is no longer necessary as the target output $V_{\rm DVS}$ in the SIDO power module is indicated by a PLL-based frequency-based control (FBC) scheme. The system processor only needs to indicate the operation frequency to the proposed hybrid control loop, which differs from prior work that needs to know the relationship between operation frequency and supply voltage with the separated control loop. In addition, the embedded PLL implementation in a hybrid control loop, which is mainly composed of the DVS emulator, the divider, and the FBC circuit, is used to generate the operation frequency for system processor and guarantee the DVS operation simultaneously. DVS emulator generates the operation frequency $F_{\rm DFS}$ for the system processor with the task indicated signal $V_{\rm MT}$, which delivers the requested operation frequency of the system processor for achieving the DFS operation. Voltage level of the $V_{\rm DVS}$ can also be detected by the DVS emulator to achieve the near-optimum DVS operation. The divider provides a multiple factor of the frequency between $F_{\rm DFS}$ and $F_{\rm INT}$ for guaranteeing the PLL operation. The divisor is controlled by the signal $V_{\rm DV}$ from the system processor, which carries out the instruction for dynamically adjusting both $V_{\rm DVS}$ and $F_{\rm DFS}$, in accordance with the distinct operation modes in system processor. The FBC circuit has the capability to synchronize the frequency difference between $F_{\rm INT}$ and the constant reference frequency $F_{\rm REF}$, which is generated from the quartz crystal unit, producing the indicative voltage $V_{\rm FLY}$ to the SIDO power module. Therefore, supply voltage $V_{\rm DVS}$ can be adjusted in the SIDO power module to achieve the near-optimum DVS operation through the hybrid control loop. Operation frequency for the system processor is also guaranteed by the FBC scheme, which is capable of realizing the DFS operation.

However, the SIDO power module suffers the effect of cross regulation from the single inductor utilization. This means that, when the sudden up-tracking occurs at $V_{\rm DVS}$, energy delivering to the $V_{\rm ANG}$ will become insufficient, resulting in an unwilling voltage drop. It may also lead to abnormal operation in analog circuits. As a result, an energy cross-modulation scheme is proposed to ease the cross-regulation effect in SIDO power module. Dual outputs can be viewed as two independent supply voltages for further guaranteeing correct functions in SoC.

III. Operation of the Hybrid Control Loop

Operation flow of the proposed hybrid control loop, which helps achieve the near-optimum DVS and DFS operations simultaneously, is shown in Fig. 5. The DVS commander can indicate operation tasks and operation modes of system processor using the signal $V_{\rm MT}$ and $V_{\rm DV}$, respectively. When the task is decided by the processor, the operation frequency $F_{\rm DFS}$ generated by DVS emulator would be changed. This means that a phase difference will be obtained between $F_{\rm INT}$ and $F_{\rm REF}$ although the divisor is unchanged. Thus, the FBC circuit can adjust the voltage $V_{\rm FLY}$ for the SIDO power module to activate DVS operation. Supply voltage $V_{\rm DVS}$ can be changed

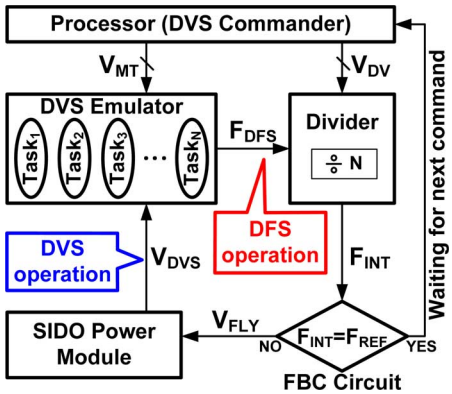


Fig. 5. Flowchart of the proposed hybrid control loop for the near-optimum DVS operation.

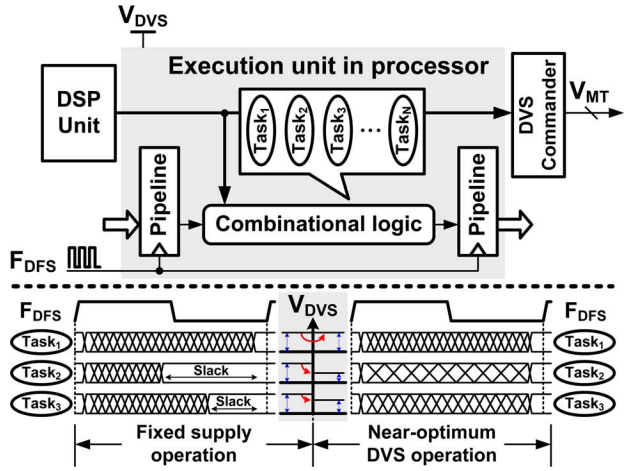


Fig. 6. Near-optimum DVS operation with the different operation tasks in the system processor.

along with the variations of voltage V_{FLY}. Since the DVS emulator is supplied by V_{DVS}, F_{DFS} generated by the DVS emulator can also be changed until F_{DFS} gets back to its demand value, wherein there is no phase difference between F_{INT} and F_{REF}. Therefore, supply voltage V_{DVS} can be naturally obtained through this hybrid control loop, which realizes that the V_{DVS} can be obtained with a near-optimum value without the need for precise indication from the system processor. A similar operation takes place when the operation mode is changed with a designate operation task. The V_{DV} can modify the divisor so as to vary both supply voltage V_{DVS} and operation frequency F_{DFS}, that is, both the DVS and the DFS operations will occur when different operation modes are executed with determined operation task in system processor.

Fig. 6 shows the near-optimum DVS operation with different operation tasks in system processor. The execution unit, which is composed of the combinational logic and the pipeline operator, is controlled by DSP unit. The combinational logic is accomplished according to the distinct tasks realizing the different execution periods within one operation cycle. In addition, operation frequency F_{DFS} is used to indicate the activation in the combinational logic, that is, each task needs to complete its operation within one clock period of F_{DFS}. Thus, the operation performance of system processor is still dominated by the F_{DFS}. However, since the logic propagation delay is mainly determined by the supply voltage, the constant supply voltage would carry out the distinct execution periods when it operates with the distinct operation tasks. The slack period will then be obtained if one operation task contains fewer logic gate counts but is supplied by an unchanged supply voltage V_{DVS}. Furthermore, V_{DVS} must be set at a relatively high voltage level in order to guarantee the correct operations for all of the task conditions. This also results in the extra energy dissipation in some leisure tasks. Therefore, the proposed hybrid control loop with the signal V_{MT} generated by the DVS commander can help activate the near-optimum DVS operation to realize the proper supply voltage for the distinct operation tasks in system processor. When one task contains the complicated logic gate count, V_{DVS} will be raised to a high voltage level to ensure the complete execution in one operation cycle. On the other hand, the V_{DVS} will be lowered down once the tasks have fewer mathematical counting in their signal path so as to properly minimize

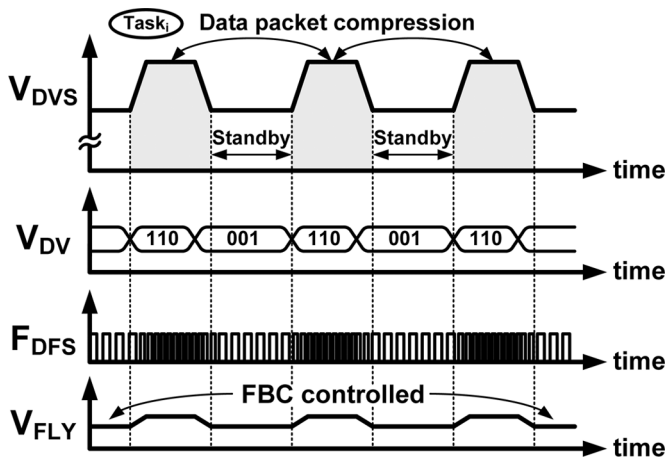


Fig. 7. Time diagram of the near-optimum DVS operation with the different operation modes.

power consumption. As a result, the near-optimum DVS operation can reduce energy dissipation with different operation tasks and ensure proper operation of the system processor.

Fig. 7 shows the time diagram of the near-optimum DVS operation with different operation modes in system processor. When one operation task is selected in the system processor, distinct operation modes may demand different operation frequencies and distinct supply voltages to minimize energy consumption. Operation of the data packet compressor is necessary in advance of data transmission to ensure the quality of the transmitted data. Thus, when data compression is activated, a higher operation frequency is demanded as well as higher supply voltage for guaranteeing proper operation. However, there are vacant time intervals which appear sequentially in series data chain. To achieve energy-efficient operation in the system processor, both the supply voltage and operation frequency can be lowered to reduce power consumption. The V_{DV} generated by the DVS commander in the system processor helps change the divisor in hybrid control loop. Then, the FBC circuit can recognize the frequency difference between F_{INT} and F_{REF} to adjust the V_{FLY} for SIDO power module and the V_{DVS}. The operation frequency is also changed due to the

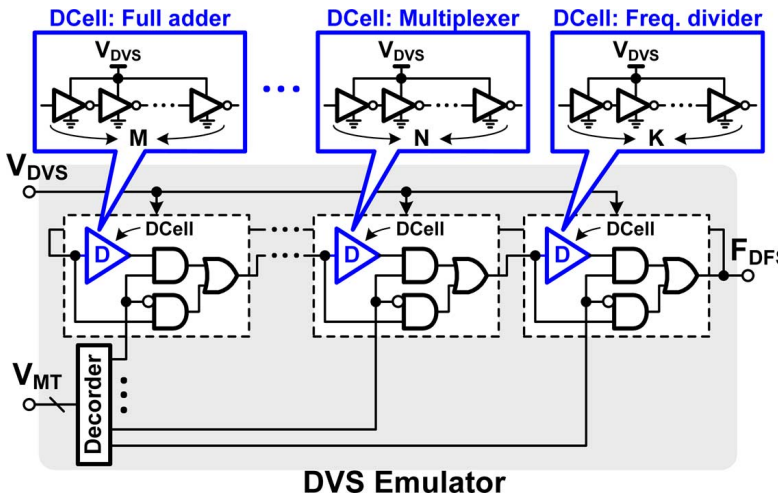


Fig. 8. Implementation of the proposed DVS emulator.

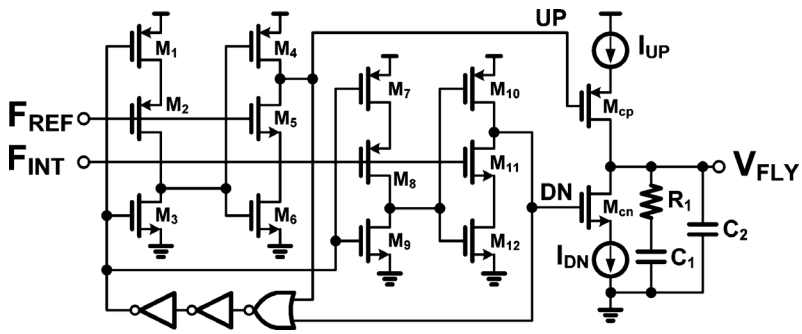


Fig. 9. Schematic of the FBC circuit.

variation of divisor. Therefore, the hybrid control loop guarantees the demanded operation frequency F_{DFS} and achieves the near-optimum supply voltage with both DFS and DVS operations.

IV. Circuit Implementation

A. DVS Emulator

Fig. 8 shows the implementation of the DVS emulator, which generates the operation frequency F_{DFS} for the system processor. F_{DFS} is varied according to V_{DVS} and the operation tasks in the system processor. Operation tasks of the processor are achieved by adopting different combinations of basic logic functions, such as the full adder, the multiplexer, or the frequency divider, which are indicated by the signal V_{MT} generated from the DVS commander in the system processor. The propagation delay of each basic logic function can be simulated through the delay cell (DCell) stage, that is, the number of inverter chains is proportional to the gate count of basic logic functions. The decoder can enable the distinct DCell stages to realize the operation of the ring oscillator for generating the demanded F_{DFS} according to the processor's operation tasks. Additionally, the DCell stages are powered by V_{DVS}, which also help achieve the near-optimum DVS operation. Once the operation task is changed in the system processor, the activation of distinct DCell stages, which is directed by V_{MT}, carries out the varied operation frequency. Fortunately, the FBC circuit and the SIDO power module can help adjust V_{DVS}, thereby varying the propagation delay of the DCell stages to obtain the demanded F_{DFS} for the execution unit in processor. The DVS emulator can be regarded as the voltage monitor of V_{DVS} along with the hybrid control loop. Consequently, the DVS emulator not only generates the satisfactory operation frequency with distinct operation tasks, but also achieves the near-optimum DVS operation for proper supply voltage.

B. FBC Circuit

The FBC circuit in Fig. 9 is used to generate the voltage V_{FLY}, which helps indicate the near-optimum DVS operation in the SIDO power module. The FBC circuit, which contains the phase detector and the charge pump (CP) structure, is considered as an error reflector to detect the frequency difference between F_{REF} and F_{INT}. The frequency F_{INT} is related to the system operation frequency F_{DFS}. To achieve the near-optimum supply function in the SIDO power module, the frequency difference between F_{REF} and F_{INT} can be reflected on both the up and down signals to adjust the reference voltage V_{FLY}, so as to adjust the supply voltage V_{DVS} for the near-optimum DVS operation. Thus, when the processor demands the higher operation frequency, voltage V_{FLY} would be raised as well as V_{DVS}, guaranteeing the optimal supply voltage level for ensuring the proper operations in system processor. As such, V_{DVS} can be adjusted according to the request of operation frequency in proposed hybrid control loop.

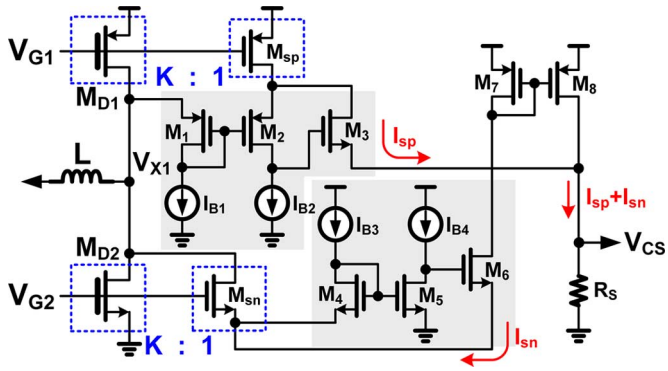


Fig. 10. Schematic of the current sensing circuit.

C. Current-Sensing Circuit

Fig. 10 shows the schematic of the current-sensing circuit. Due to the current-programmed control in the proposed SIDO power module, the current-sensing circuit is utilized to generate the full-range current-sensing signal $V_{\rm CS}$, as well as the duty cycles for dual outputs $V_{\rm ANG}$ and $V_{\rm DVS}$. With the defined sensing factor K, which is set between the switches M_{D1} and M_{D2} to the sensing MOSFETs $M_{\rm sp}$ and $M_{\rm sn}$, respectively, the high-side and the low-side sensing currents are obtained as $I_{\rm sp}$ and $I_{\rm sn}$, respectively. Transistor $M_{\rm Sp}$ generates the sensing current when the inductor is charging in the SIDO power module. The common-gate amplifier, which is realized by M_1 to M_3 achieves the operation with a simple structure and fast response. The source-to-drain voltage between M_{D1} and M_{sp} can be equalized to enhance the precision of the current-sensing operation. Similarly, another common-gate amplifier realized by M_4 to M_6 also helps achieve the low-side current sensing with the sensing current $I_{\rm sn}$ when the inductor discharging period is activated. Therefore, the full-range current-sensing signal can be obtained as $V_{\rm CS}$, which can be used to monitor the instantaneous inductor current information in order to achieve current-programmed operation in the SIDO power module.

D. Energy Scheme Controller

Fig. 11 shows the schematic of the energy scheme controller in the proposed SIDO power module. Error signals, $V_{\rm EA}$ and $V_{\rm EB}$, are produced by EAs to monitor the outputs of $V_{\rm ANG}$ and $V_{\rm DVS}$, respectively. Voltage levels of the error signals are varied determined by the requested power at outputs because of current-programmed control scheme. Since the voltage level of $V_{\rm DVS}$ is often adjusted to achieve near-optimum DVS operation, the voltage variation at $V_{\rm ANG}$ would be derived due to the effect of cross regulation. $V_{\rm ANG}$ needs to be maintained as a stable supply voltage for analog circuits in SoC. Therefore, to effectively reduce the occurrence of cross regulation, the energy cross-modulation scheme is used to correlate the energy demands with each output on both error signals. In this case, $V_{\rm EAR}$ and $V_{\rm EBR}$, which can be used to determine the duty cycles for both outputs, are generated by correlating both $V_{\rm EA}$ and $V_{\rm EB}$. Once an energy request is demanded at one specific output, such as $V_{\rm DVS}$, both the correlated error signals $V_{\rm EAR}$ and $V_{\rm EBR}$ will be varied simultaneously. This process helps ensure the unchanged energy distribution for the output with a constant requested power, which can effectively minimize cross regulation in the proposed SIDO power module. The current-sensing signal

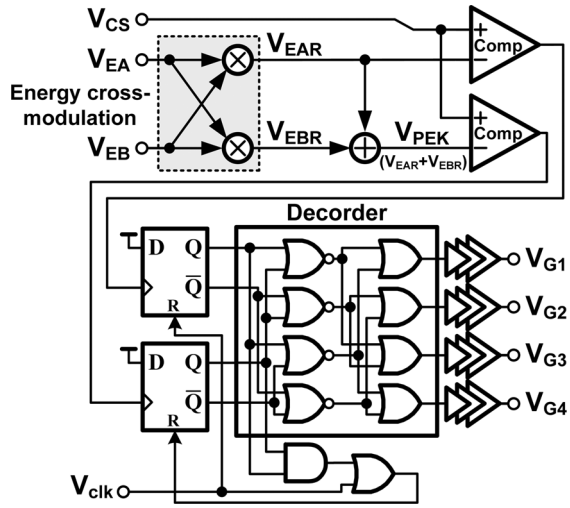


Fig. 11. Schematic of the energy scheme controller in the SIDO power module.

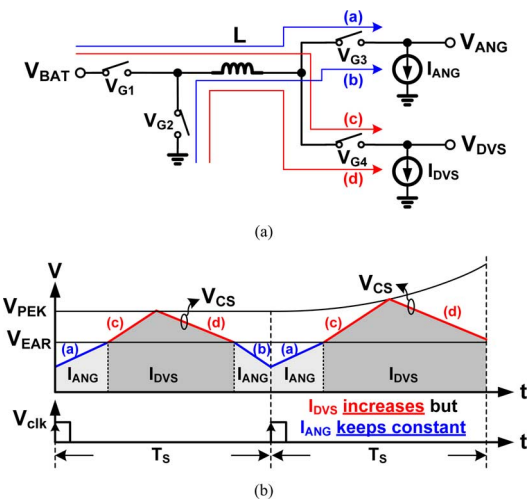
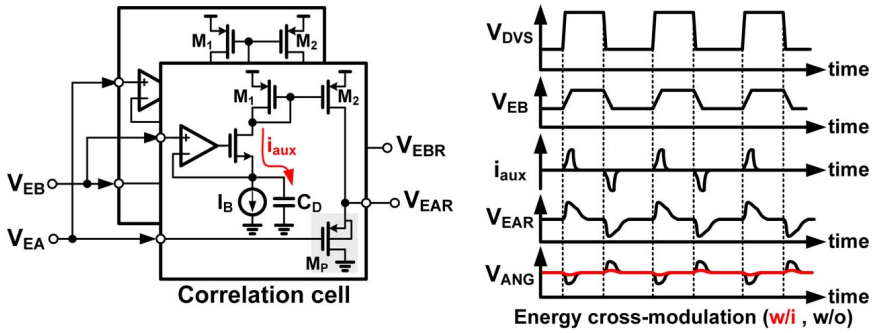


Fig. 12. Operation of the SIDO power module. (a) Energy delivery paths in the power stage. (b) Energy delivery methodology in steady-state and the near-optimum DVS operation.

$V_{\rm CS}$ helps determine the duty cycle with the correlated error signals $V_{\rm EAR}$ and $V_{\rm EBR}$ for dual outputs. Due to the superposition technique [18], the peak inductor current level can be addressed in every PWM switching cycle through the voltage $V_{\rm PEK}$. It also guarantees the inductor dc current to be equal to the summation of dual output loads. In addition, voltage $V_{\rm EBR}$ is used to indicate the energy allocation for dual outputs. Comparators decide the transition of energy paths in power stage, while the signal $V_{\rm clk}$ realizes the PWM operation. Finally, control signals V_{G1} to V_{G4} are generated for power switches with the decoder and the driver circuit. A dead-time mechanism is embedded in driver circuits with the nonoverlapping realization to avoid the shoot-through current in the power stage.

Fig. 12 shows the operation of the SIDO power module. Fig. 12(a) depicts the energy delivery paths in the power stage. There are four different energy delivery paths to transfer energy from input voltage $V_{\rm BAT}$ to the dual outputs $V_{\rm ANG}$ and $V_{\rm DVS}$ through the single off-chip inductor. Path-(a) and path-(c) are the inductor charging paths, while path-(b) and path-(d) are the inductor discharging paths. The energy-delivery methodology



(a) (b)

Fig. 13. (a) Implementation of the energy cross-modulation scheme. (b) Time diagram of the energy cross-modulation operation.

is shown in Fig. 12(b). With the peak current indication signal $V_{\rm PEK}$ and the correlated error signal $V_{\rm EAR}$, operation of the four different energy delivery paths can be achieved in steady state along with the current-sensing signal $V_{\rm CS}$. The energy here is sequentially allocated to the output of $V_{\rm ANG}$, $V_{\rm DVS}$, and $V_{\rm ANG}$ in every PWM switching cycle, which realizes the superposition technique with the current-programmed control for achieving the energy delivery methodology. Therefore, the operation function of the SIDO power module can be guaranteed without the need of freewheel stage [14]; this process can minimize the output voltage ripple and enhance the power efficiency due to lower inductor dc current level. However, when the near-optimum DVS operation is activated with an up-tracking response on $V_{\rm DVS}$, the increased energy request raises the voltage $V_{\rm EBR}$ as well as the peak indication voltage $V_{\rm PEK}$. Consequently, energy delivering to the output $V_{\rm ANG}$ will be insufficient at the next PWM switching cycle, resulting in cross regulation with the unwilling voltage drop at the $V_{\rm ANG}$.

The proposed energy cross-modulation scheme shown in Fig. 13 is designed to reduce the effect of cross regulation in the SIDO power module. Fig. 13(a) shows the schematic of the energy cross-modulation circuits. $V_{\rm EAR}$ and $V_{\rm EBR}$ are mainly determined by $V_{\rm EA}$ and $V_{\rm EB}$, respectively. The correlation cell is composed of the voltage follower and the voltage-controlled current-source (VCCS) circuit [20]. The voltage follower is achieved through the MOSFET M_P, which can directly send the voltage variations from $V_{\rm EA}$ to $V_{\rm EAR}$ or $V_{\rm EB}$ to $V_{\rm EBR}$. Furthermore, the VCCS circuit is used to correlate the voltage variations of $V_{\rm EB}$ to $V_{\rm EAR}$ or $V_{\rm EA}$ to $V_{\rm EBR}$, so that the voltage variation on $V_{\rm ANG}$ and $V_{\rm DVS}$ would simultaneously vary both error signals. The constant current I_B determines the dc bias of the VCCS circuit and thus ensures the operation of voltage follower. Capacitor C_D is used to detect the variation on the error signals $V_{\rm EA}$ and $V_{\rm EB}$ by generating the auxiliary current $i_{\rm aux}$. Here, $i_{\rm aux}$ can be expressed as

$$i_{\rm aux} = \frac{v_{\rm EB}}{1/sC_D} = sC_D v_{\rm EB}. \tag{1}$$

As the VCCS circuit can be regarded as the differentiator, expression of the $i_{\rm aux}$ in (1) is modified as

$$i_{\rm aux}(t) = C_D \frac{dV_{\rm EB}}{dt}. \tag{2}$$

As a result, the variation of the correlated error signal $V_{\rm EAR}$ can be obtained as

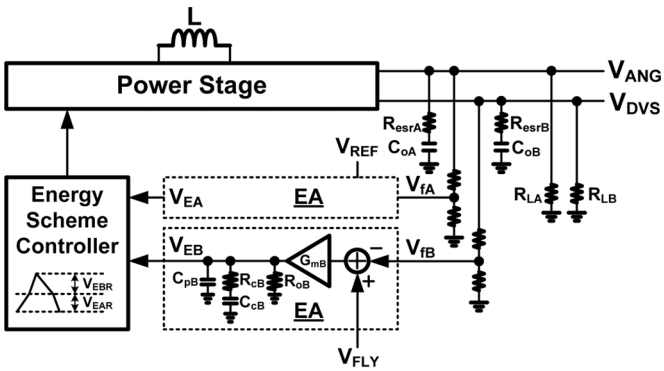
$$v_{\rm EAR} = v_{\rm EA} + \frac{i_{\rm aux}}{g_{m,MP}} = v_{\rm EA} + \left(\frac{sC_D}{g_{m,MP}}\right) v_{\rm EB} \tag{3}$$

where $g_{m,MP}$ is the transconductance of MOSFET M_P.

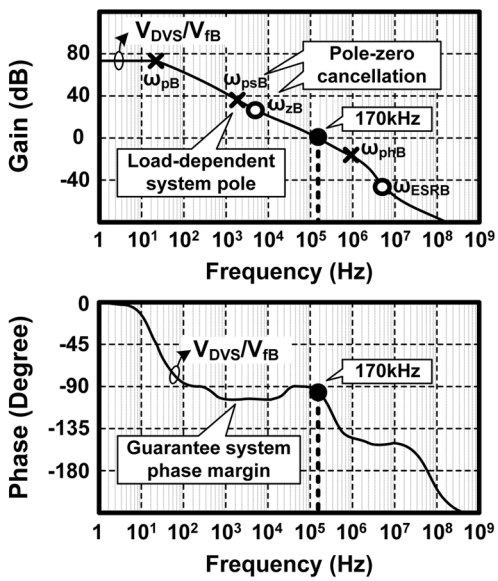
According to the equation shown in (3), variation of $V_{\rm EAR}$ is resulted from the variations on both $V_{\rm EA}$ and $V_{\rm EB}$. A similar operation is also realized to obtain the correlated error signal $V_{\rm EBR}$. Therefore, the correlated error signals, $V_{\rm EAR}$ and $V_{\rm EBR}$, receive energy conditions not only from the voltage variations of their self-modulated outputs, but also from the voltage variations at the other output. In addition, the proposed energy cross-modulation scheme is operated in the bidirectional way without any restrictions in the proposed SIDO power modules. Time diagram of the proposed energy cross-modulation scheme during the near-optimum DVS operation period is shown in Fig. 13(b). $V_{\rm DVS}$ can be adjusted to guarantee proper supply voltage for system processor. VCCS circuit in the proposed correlation cell shown in Fig. 13(a) can detect the voltage variation on $V_{\rm EB}$ that generates the auxiliary current $i_{\rm aux}$, such that $V_{\rm EAR}$ can be varied even through the error signal $V_{\rm EA}$ gains zero voltage variation. The increase of $V_{\rm EAR}$ helps obtain the satisfactory energy for the $V_{\rm ANG}$ to maintain the constant request power. Consequently, voltage drop on the $V_{\rm ANG}$ can be minimized greatly when the tracking response is activated on $V_{\rm DVS}$. Effect of cross-regulation in the proposed SIDO power module can be removed during the period of near-optimum DVS operation.

E. Frequency Characteristic of the SIDO Power Module

To guarantee the stability of proposed SIDO power module as well as the hybrid control loop, analysis of frequency response is depicted in Fig. 14. Since the PLL implementation in hybrid control loop merely produces a reference voltage $V_{\rm FLY}$, system stability of the proposed power management is dominated through the SIDO power module. As shown in Fig. 14(a), dual feedback loops are used to monitor the voltage regulation for both $V_{\rm ANG}$ and $V_{\rm DVS}$. EA including the proportional-integral (PI) compensator helps ensure the system stability. The energy scheme controller operates with the superposition technique which helps realize energy delivery scheme to dual outputs in every PWM switching cycle. That is, energy requirement for each output can be directly reflected by the error signals as



(a)



(b)

Fig. 14. (a) Analysis of the control loop in the proposed SIDO power module. (b) Measured frequency response for the loop of $V_{\rm DVS}$ in the proposed SIDO power module.

well as the energy delivery scheme. As illustrated in Fig. 12(b), $V_{\rm PEK}$ and $V_{\rm EAR}$ are used to determine duty cycle as well as energy delivery methodology with the current-programmed control in proposed SIDO power module. Voltage difference between $V_{\rm PEK}$ and $V_{\rm EAR}$ indicates the correlated error signal $V_{\rm EBR}$. In other words, the energy delivery scheme is identical to that in conventional single output current-programmed buck converter. This process also guarantees independent energy delivery scheme of dual outputs. Thus, the stability of SIDO power module can be viewed from the separated modulated loops of $V_{\rm ANG}$ and $V_{\rm DVS}$ in Fig. 14(a), so as to demonstrate frequency characteristic and stable operation for whole loop of the proposed SIDO power module.

Control-to-output transfer function for the loop of $V_{\rm DVS}$ for near-optimum DVS operation can be described as

$$G_{vd}(s)=\frac{\hat{v}_{\rm DVS}}{\hat{v}_{\rm EB}}\approx\frac{R_{LB}}{R_S\left(1+\frac{R_{LB}T_S}{L}\right)}\frac{(1+sR_{esrB}C_{oB})}{(1+sR_{LB}C_{oB})}$$
$$=\frac{R_{LB}}{R_S\left(1+\frac{R_{LB}T_S}{L}\right)}\left(1+\frac{s}{\omega_{\rm ESRB}}\right)\left(1+\frac{s}{\omega_{\rm psB}}\right)\quad(4)$$

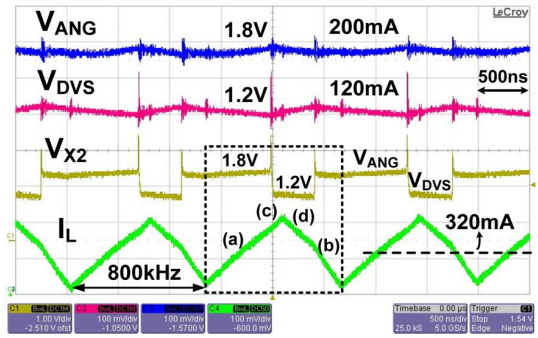


Fig. 15. Measured steady-state operation of the SIDO power module.

where R_{LB} is the load resistance obtained at $V_{\rm DVS}$, R_S is gotten from the current-sensing mechanism in the current loop of the current-programmed control, and T_S is one PWM switching period. Sampling function is contained within the current-loop in the current-programmed control to simplify frequency characteristic of the power stage, so as to derive the single load-dependent system pole ω_{psB} at the $V_{\rm DVS}$ [21]. In addition, input voltage variation has little effect on the operation since the current-loop implementation can be regard as the feed-forward function. Thus, the dependency of input voltage to the current-programmed control loop is relatively low and is omitted in the frequency analysis. The zero $\omega_{\rm ESRB}$ appears due to the equivalent-series-resistance R_{esrB} on the output capacitor C_{oB}. Additionally, the transfer function of both EA and PI compensator in the modulated loop for $V_{\rm DVS}$ can be expressed as

$$G_{cvB}(s)=\frac{\hat{v}_{\rm EB}}{\hat{v}_{\rm fB}}$$
$$=\frac{G_{mB}R_{oB}(1+sR_{cB}C_{cB})}{(1+sR_{oB}C_{cB})(1+sR_{oB}C_{pB})}$$
$$=G_{mB}R_{oB}\frac{\left(1+\frac{s}{\omega_{zB}}\right)}{\left(1+\frac{s}{\omega_{pB}}\right)\left(1+\frac{s}{\omega_{phB}}\right)}\quad(5)$$

where G_{mB} is the transconductance and R_{oB} is the equivalent output resistance of EA in the control loop for $V_{\rm DVS}$. The PI compensator is composed of the compensation resistor R_{cB} and the compensation capacitor C_{cB}. C_{pB} is the parasitic capacitance obtained at the output of EA. R_{cB} and C_{cB} are 150 kΩ and 200 pF, respectively, where the compensation capacitor C_{cB} is accomplished by the capacitor-multiplier method [22] to achieve on-chip compensation. ω_{pB} is regarded as the system dominant pole to ensure the stability, while ω_{phB} is the high-frequency nondominant pole. ω_{zB} is the system compensation zero, which is used to compensate the effect of the output load-dependent system pole ω_{psB}. The pole-zero cancellation is achieved within the specification-defined output load ranges. Therefore, loop gain for the loop of $V_{\rm DVS}$ is shown as

$$L_B(s)\approx G_{vd}(s)G_{cvB}(s)$$
$$=\frac{G_{mB}R_{oB}R_{LB}}{R_S\left(1+\frac{R_{LB}T_S}{L}\right)}$$
$$\times\frac{\left(1+\frac{s}{\omega_{zB}}\right)\left(1+\frac{s}{\omega_{\rm ESRB}}\right)}{\left(1+\frac{s}{\omega_{psB}}\right)\left(1+\frac{s}{\omega_{pB}}\right)\left(1+\frac{s}{\omega_{phB}}\right)}\quad(6)$$

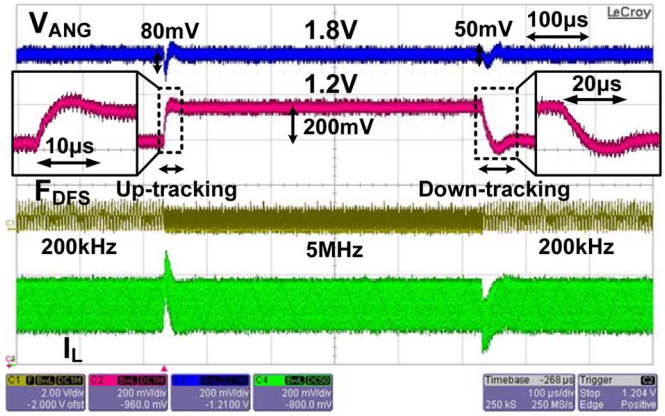


Fig. 16. Measured near-optimum DVS operation with the up-tracking and the down-tracking responses.

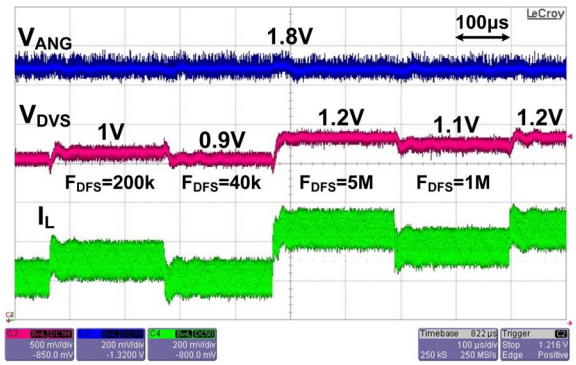


Fig. 17. Measured near-optimum DVS operation with the different operation frequency $\mathrm{F_{DFS}}$.

and its frequency response is depicted in Fig. 14(b).

The system phase margin is guaranteed with a proper safe region. Loop gain for the V_{ANG} in the proposed SIDO power module is similar to (6). The frequency response is shown in Fig. 14(b). Consequently, the system stability in the proposed SIDO power module can be ensured because of the current-programmed control and the superposition technique which also indicate the stable operation in the proposed hybrid control loop.

V. Experimental Results

The proposed near-optimum DVS operation with the SIDO power module was fabricated by 65-nm CMOS technology. Fig. 15 shows the measured steady-state operation of proposed SIDO power module. Nominal voltages of V_{ANG} and V_{DVS} are 1.8 and 1.2 V, respectively, with the input voltage of 3.3 V. Load currents at both V_{ANG} and V_{DVS} are 200 and 120 mA, respectively. Both the output voltage ripples are smaller than 25 mV. In addition, V_{X2} can indicate the energy distribution in proposed SIDO power module since the voltage at the right-hand side of the inductor is regularly connected to V_{ANG} or V_{DVS} in every PWM switching cycle. The average inductor current will be the summation of two output loads due to the current-programmed control. Fig. 16 shows the measured near-optimum DVS operation. When DVS commander in system processor indicates the demanded operation frequency, both DFS and DVS operations are activated to provide proper supply functions. As the operation frequency is

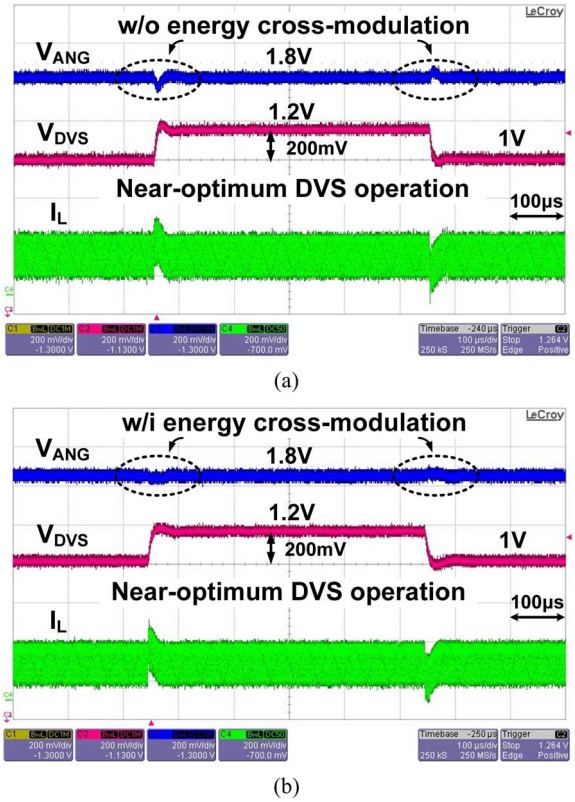


Fig. 18. Measured energy cross-modulation scheme in the proposed SIDO power module (a) without the energy cross-modulation scheme and (b) with the energy cross-modulation scheme.

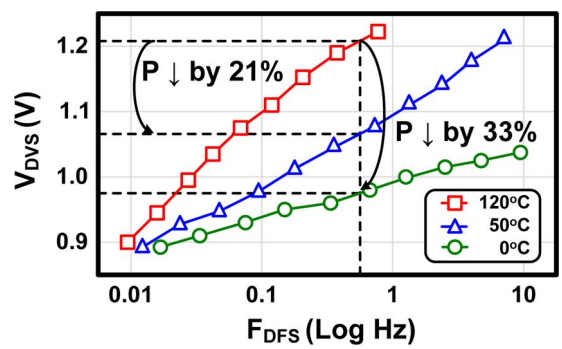
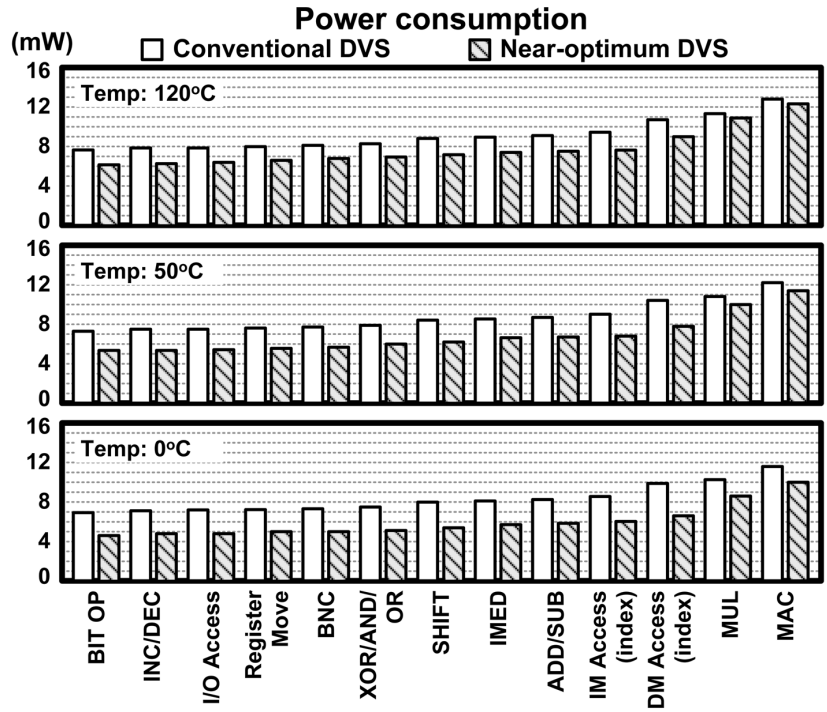


Fig. 19. Measured operation frequency $\mathrm{F_{DFS}}$ and the supply voltage $\mathrm{V_{DVS}}$ with the different temperature conditions.

changed from 200 kHz to 5 MHz, V_{DVS} realizes the up-tracking response to raise the voltage from 1 to 1.2 V for achieving the near-optimum supply voltage. Similarly, the down-tracking response also occurs when the operation frequency of system processor is requested to be lowered. Speeds of up-tracking and down-tracking responses on V_{DVS} with a 0.2-V voltage variations are 10 and 20 μs, respectively. V_{ANG} is maintained at the same voltage level since the energy scheme controller in SIDO power module can ensure the proper energy delivery function in the transient response. Fig. 17 shows the measured near-optimum DVS operation with the different demanded operation frequency F_{DFS}. Once F_{DFS} for system processor is requested to be changed, the proposed hybrid control loop can smoothly adjust the supply voltage V_{DVS} by the FBC



(a)

Measured power consumption with distinct operation tasks in system processor (0°/50°/120°C)

Task**	Gate Switching	Conventional DVS [23] (mW)	Near-optimum DVS (mW)	Power Saving (%)
BIT OP	32k	6.9 / 7.4 / 7.8	4.7 / 5.3 / 6.2	32 / 28 / 21
INC/DEC	33k	7.1 / 7.6 / 7.9	4.8 / 5.3 / 6.3	32 / 30 / 20
I/O Access	33.5k	7.2 / 7.7 / 7.9	4.9 / 5.5 / 6.5	31 / 28 / 18
Register Move	34k	7.2 / 7.8 / 8	5 / 5.7 / 6.7	30 / 26 / 16
BNC	34.5k	7.3 / 7.9 / 8	5 / 5.8 / 6.8	31 / 26 / 15
XOR/AND/OR	35k	7.5 / 7.9 / 8.3	5.1 / 6 / 6.9	32 / 24 / 17
SHIFT	36.5k	8 / 8.4 / 8.9	5.4 / 6.1 / 7.1	32 / 27 / 20
IMED	37.5k	8.1 / 8.6 / 9	5.7 / 6.6 / 7.2	29 / 23 / 20
ADD/SUB	38k	8.2 / 8.8 / 9.1	5.9 / 6.8 / 7.4	28 / 23 / 19
IM Access (index)	39k	8.7 / 9 / 9.4	6 / 6.9 / 7.7	31 / 23 / 18
DM Access (index)	45k	9.9 / 10.4 / 10.8	6.7 / 7.8 / 9	32 / 25 / 17
MUL	47k	10.2 / 10.9 / 11.2	8.7 / 10 / 10.9	15 / 8 / 3
MAC	53k	11.6 / 12.1 / 12.9	10 / 11.3 / 12.3	14 / 7 / 4

Processor feature:
1. 65nm implementation
2. 32 bit DSP operation
3. 200k logic gate counts

** Each task is activated with one specific instruction for measuring power consumption.

Task illustration:
BIT OP: Bit operation
INC/DEC: Register increment / decrement
BNC: Branch on no carry
IMED: Immediate value operation
IM Access (index): Instruction memory access
DM Access (index): Data memory access
MUL: Multiply
MAC: Multiply + accumulate (for convolution)

(b)

Fig. 20. (a) Measured power consumption with different operation tasks in system processor. (b) Comparison between conventional DVS and the proposed near-optimum DVS.

scheme. The FBC circuit then indicates the near-optimum DVS operation for the SIDO power module in order to generate the optimal $V_{\rm DVS}$, that is, near-optimum DVS operation can ensure the variation of $V_{\rm DVS}$ from 0.9 to 1.2 V with the requested operation frequency from 40 kHz to 5 MHz. Additionally, load current conditions for system processor would also be changed simultaneously with the adjusted $V_{\rm DVS}$. The proposed energy cross-modulation scheme helps eliminate the cross-regulation and ensures the regulated output voltage on $V_{\rm ANG}$.

Fig. 18 shows the measured energy cross modulation in the proposed energy scheme controller of the SIDO power module. To guarantee the proper voltage supply function at the output $V_{\rm ANG}$ for analog circuits, the effect of cross regulation must be minimized when the near-optimum DVS operation is activated. Fig. 18(a) shows the measured near-optimum DVS operation without the work of energy cross-modulation scheme. The obvious voltage variation at $V_{\rm ANG}$ occurs due to the utiliza-

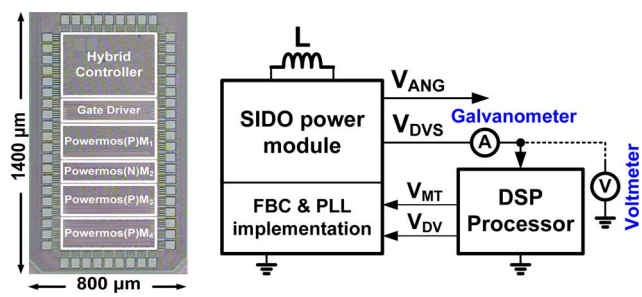


Fig. 21. Chip micrograph and experimental setup for power measurement.

TABLE I
DESIGN SPECIFICATIONS OF SIDO POWER MODULE

Technology	65 nm CMOS process	
Input voltage	2.7 V – 3.6 V	
Off-chip inductor	4.7 μH	
Switching frequency in the SIDO module	800 kHz	
System freq. range	40 kHz – 5 MHz	
Outputs	V_{OA} = 1.8 V	V_{OB} = 0.9 – 1.2 V (Near-optimum DVS)
Output capacitor	4.7 μF	4.7 μF
Maximum load current	200 mA	200 mA
Cross-regulation	Not noticeable	
Output voltage ripple	Smaller than 20 mV	
Power efficiency	Max. 90 %	
Active chip area	1.12 mm^2	

TABLE II
COMPARISONS OF THE TRACKING RESPONSE WITH INDUCTOR-BASED POWER MODULE

	This work	[8]	[24]	[25]	[26]
Topology	SIDO converter	Buck-Boost converter	Buck converter	Boost converter	Buck-Boost converter
Technology	65 nm CMOS	0.25 μm CMOS	0.35 μm CMOS	0.25 μm CMOS	0.35 μm CMOS
Supply voltage	2.7 – 3.6 V	2.5 – 4.5 V	2.4 – 3.3 V	8 – 13.5 V	1.6 – 3.3 V
Switching frequency	800 kHz	5 MHz	850 kHz	1.5 MHz	250 kHz (Variable)
Inductor	4.7 μH	1 μH	N/A	10 μH	10 μH
Output capacitor	4.7 μF	0.88 μF	N/A	2.2 μF	10 μF
Numbers of output	2	1	1	1	1
Output voltage	1.8 V / 1.2 V	2 – 4 V	0.3 – 2.1 V	16 – 30 V	0.9 – 3 V
Max. load current	400 mA	400 mA	N/A	300 mA	800 mA
Up-tracking	10 μs / 0.2 V	20 μs / 1 V	1 ms / 1.8V	18 μs / 4V	150 μs / 1 V
Down-tracking	20 μs / 0.2 V	15 μs / 1 V	2 ms / 1.8V	1.8 ms / 4V	37 μs / 1 V
Peak efficiency	90%	91%	N/A	N/A	96.5%
Active area	1.12 mm^2	4.86 mm^2	2.2 mm^2	6.18 mm^2	1.3 mm^2
Application	SoC integration	Power amplifier	N/A	RGB LED driver	N/A

tion of a single inductor in SIDO power module, which could not guarantee the constant energy delivery scheme when the sudden transient response occurs. Fig. 18(b) demonstrates that voltage variation at V_{ANG} is greatly minimized when the near-optimum DVS operation at the V_{DVS} is activated. The proposed energy cross-modulation scheme can be used to ensure adequate energy delivering for the transient-less output of the SIDO power module. Fig. 19 shows the measured results of the operation frequency F_{DFS} and the supply voltage V_{DVS} with near-optimum DVS operation. Once the operation frequency can be fixed at a constant value along with the specific task in system processor, the supply voltage will be automatically adjusted by the proposed hybrid control loop to obtain optimal voltage level. Supply voltage can be raised to 1.21 V or be lowered to 0.975 V with a selected operation frequency when the temperature condition is 120° or 0°, respectively. However, the supply voltage must be set with the worst operating conditions in conventional implementation, such as the measured result with the temperature of 120° shown in Fig. 19 to guarantee the correct operation for the system processor. The proposed hybrid control loop can indicate the different V_{DVS} for the proposed SIDO power module while maintaining a constant operation frequency F_{DFS} under the different temperature conditions. Thus, the proposed near-optimum DVS operation has the capability to reduce power consumption up to 33%, thereby providing the optimal supply voltage level for the system processor.

Fig. 20(a) shows the measured power consumption of system processor with the different operation tasks. Different operation tasks consume distinct power in system processor. The fabricated chip can alter the operation with conventional DVS or the proposed hybrid control scheme, so as to realize a fair comparison. In conventional DVS, the system processor indicates the supply voltage directly without the demand of operation frequency. The supply voltage is needed with a relative high value to guarantee correct operation in all conditions, as depicted in Fig. 19. Thus, power consumption is large. The proposed hybrid control loop with near-optimum DVS operation can effectively reduce power consumption, since the supply voltage can be adjusted to optimal voltage levels with the different operated circumstances. Conventional DVS methodology in [23], which is commonly used DVS methodology in SoC, is also implemented in the proposed power management. Conventional DVS operation only modulates the supply voltage according to processor's demands without monitoring operation frequency. Fig. 20(b) shows the comparison between conventional DVS operation and the proposed near-optimum DVS operation. Power consumption of system processor varies according to the different operation tasks which realize the

distinct gate switching. The near-optimum DVS operation can effectively reduce power consumption under different temperature conditions. Fig. 21 shows the chip micrograph and the experimental setup for power measurement. Active silicon area of the fabricated chip is 1.12 mm^2. The fabricated chip contains the SIDO power module, DVS emulator, FBC circuit, and divider constituting the hybrid control loop, thereby achieving the near-optimum DVS operation. Moreover, power measurement of the system processor for the hybrid control scheme is achieved by the Voltmeter and the Galvanometer. Specifications of the proposed SIDO power module are listed in Table I. Comparisons of the tracking response with the inductor-based power module are shown in Table II.

VI. Conclusion

An energy-efficient SIDO power module with the frequency-based hybrid control loop is proposed to achieve the near-optimum DVS operation in SoC system. Power loop for controlling the SIDO power module has been merged into PLL to simultaneously realize proper supply voltage and operation frequency. Near-optimum DVS operation is achieved by the demand of system processor, which overcomes the PVT-caused distortion to obtain the near-optimum supply voltage. In addition, the FBC circuit helps achieve the hybrid control scheme in accordance with demanded operation frequency. Therefore, DVS and DFS operations can be achieved at the same time. Experimental results demonstrate correct near-optimum DVS operation and proper energy delivery scheme in the SIDO power module, as well as the requested operation frequency. The proposed power management fabricated by 65-nm technology occupies a 1.12 mm^2 silicon area and achieves highest power reduction by 33%.

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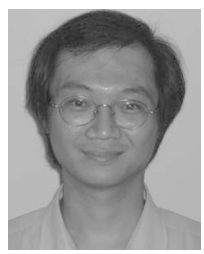

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