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Investigations of an Independent Double-Gated Polycrystalline Silicon Nanowire Thin Film Transistor for Nonvolatile Memory Operations

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In this study, we investigate the merits of an independent double-gated configuration for nonvolatile memory operations. In contrast to the convention where the programming/erasing gate also acts as the read gate, a dedicated read gate with an oxide-only dielectric is proposed in the new mode. Using the same device under identical programming/erasing conditions, greatly improved programming speed (e.g., 61% increase under the stress condition of 18 V for 10 μs) is achieved, while the erasing speed, albeit initially retarded, shows enhancement when the erasing time is larger than a certain value, which can be explained by the back-gate bias effects. Retention characterization indicates that the new mode offers a larger memory window after 10 year extrapolation. In addition, a proper auxiliary gate bias applied during programming/erasing processes is found to improve the programming/erasing speed. Finally, by taking advantage of the separate-gated feature, two independent storage sites can be obtained by employing an oxide–nitride–oxide layer as the dielectric for both gates, thus realizing 2-bit/cell functionality.
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1. Introduction

With ever increasing demand for flash memory products (e.g., cell phones, USB drives, memory cards), cost reduction-oriented memory industries have devoted to circumventing the scaling limit.[1] Among the various nonvolatile memory (NVM) architectures, a charge-trapping (CT) device has demonstrated its high performance and strong potential to succeed the conventional floating-gate (FG) device. Silicon–oxide–nitride–oxide–silicon (SONOS), in particular, has received renewed interest owing to its less stringent limitation on the tunneling oxide thickness and stronger immunity against interference coupling.[2] Akin to a nitride read-only memory (NROM),[3] SONOS relies on the nonconductive nitride to trap electrons coming from the channel. In contrast to the conductive polycrystalline silicon (poly-Si) used in the FG device, this unique feature helps realize 2-bit/cell functionality by storing electrons at two different sites. In addition to trapping layer engineering, three-dimensional (3D) technology is also under the spotlight as it not only is compatible with conventional planar processes by simply adding more layers in the vertical direction, but also greatly improves interconnect density, reduces cost, and provides a platform for heterogeneous integration.[4] Recent works have demonstrated the feasibility and strong potential of 3D technology in NVM applications.[5–7] It is worth noting that in those 3D stacked structures, poly-Si is adopted as the channel material to avoid the complexity and difficulty in the high-temperature deposition of single-crystalline Si layers. Although grain boundary effects are a concern in poly-Si, poly-Si-based thin film transistors (TFTs) with a nanowire (NW) channel and a multi-gated scheme have been shown to perform comparably to their bulk-Si counterparts.[8,9] In addition, poly-Si TFTs greatly facilitate the integration of a wide array of circuit components, making possible system-on-panel (SOP) applications.[10]

Most of the previous works regarding NW SONOS devices put emphasis on tie-gated structures owing to their better gate controllability and simpler fabrication procedure than separate-gated counterparts.[11–14] However, an independent double-gated (IDG) device has started to demonstrate its merits for more flexible operations based on the opposite gate bias effects.[15–17] In light of this and employing a very simple and low-cost procedure, we have recently proposed an IDG poly-Si NW TFT as a SONOS-type memory device.[18,19] We found in ref. 18 that the threshold voltage (V_{TH}) windows under two feasible read modes (i.e., read by two different gates) show distinctly different dependences on the auxiliary gate (AG) bias. Here, the AG refers to the gate with a fixed bias during current–voltage (I–V) measurement in contrast to the driving gate. A different degree of AG bias shielding from trapped charges depending on the location of trapped charges relative to the read gate was used to qualitatively explain this behavior. In fact, this phenomenon has been observed when an IDG SONOS device was read by a gate without an ONO stack,[20] i.e., the unconventional read approach as opposed to the convention where the programming/erasing (P/E) gate (the gate with an ONO dielectric) also serves as the read gate. However, the P/E speed comparison between these two read modes and the implications for retention characteristics have never been reported. In this study, we investigate the mechanism leading to the different P/E efficiencies of two read modes in detail, and discuss the merits of the unconventional read approach and its retention characteristics. Considering that the device studied in this work is programmed and erased by Fowler–Nordheim (FN) tunneling, which is compatible with a NAND flash memory, an ONO stack is used as the dielectric of both gates to realize the 2-bit/cell feature.

The contents of this paper are arranged as follows. The underlying principle governing the different dependences of the V_{TH} window on AG bias under two read modes is discussed in §2 along with its implications for P/E speed and retention characteristics when different read modes are adopted. Section 3 then investigates the effect of AG bias on P/E speed. The 2-bit/cell feature is analyzed in §4. Finally, a brief conclusion is drawn in §5. Through the analysis performed in this work, it is believed that the proposed concept will be highly advantageous in facilitating the advancement of 3D high-density memory technology.

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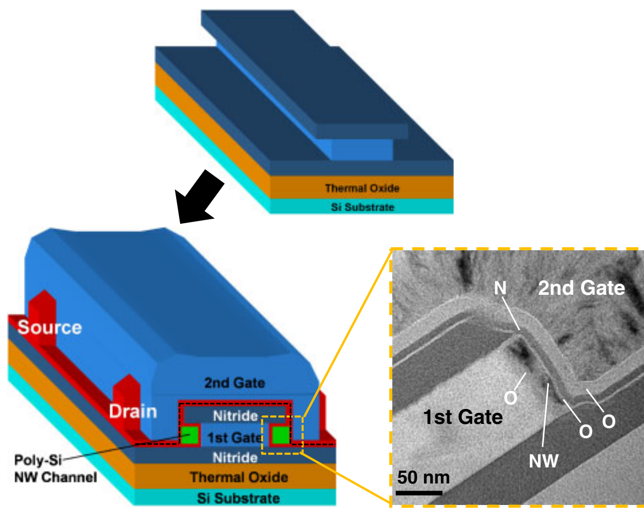
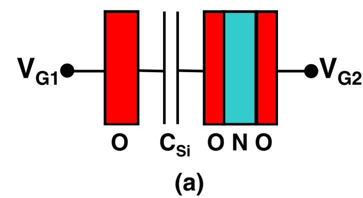


Fig. 1. (Color online) Major processing steps and the TEM image of the proposed device.



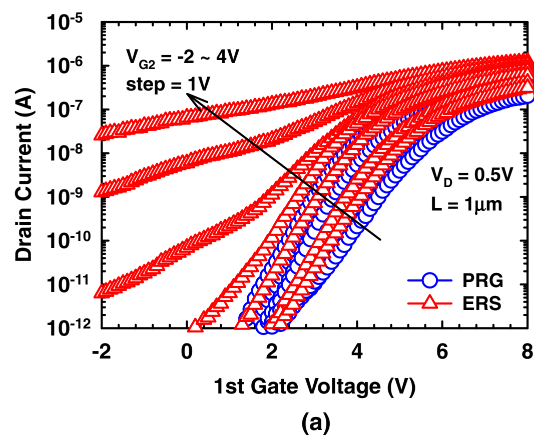
	1st gate	2nd gate
SG-1 mode	driving gate	auxiliary gate
SG-2 mode	auxiliary gate	driving gate

(b)

Fig. 2. (Color online) (a) Graphic representation for indicating the composition of the gate dielectrics and notation for the applied biases. (b) Definition of the read modes in characterization of transfer curves.

2. Concept Description and Explanation

Figure 1 shows the major processing steps and the transmission electron microscopic (TEM) image of a fabricated device. The device fabrication process was elaborated in refs. 19 and 21. Simply put, the recess of the first *in situ* doped poly-Si gate underneath the nitride was formed by selective plasma etching followed by refilling with the first gate dielectric (oxide) and active layer. After low energy implantation, source/drain regions and NW channels were subsequently defined by chlorine-based anisotropic dry etching. Finally, the device was completed after the deposition and patterning of the second gate stack that comprised an oxide/nitride/oxide (ONO) stack and *in situ* doped poly-Si. Throughout the entire process flow, no advanced lithographic apparatus is required as the width and height of NW are controlled by the duration of selective etching and the thickness of the first poly-Si gate, respectively. Figure 2(a) gives a graphic representation of the composition of the gate dielectrics and the applied biases to the first gate (V_{G1}) and second gate (V_{G2}) during I–V measurements. A 12 nm oxide layer and a 3/8/13 nm ONO stack obtained by low pressure chemical vapor deposition (LPCVD) were employed as the dielectrics of the first and second gate, respectively. The NW channel thickness is around 14 nm. The read modes in the characterization of transfer curves, denoted as SG-1 and SG-2, are defined in Fig. 2(b). Figures 3(a) and 3(b) show respectively the resultant transfer curves for the SG-1 and SG-2 modes with varying AG bias under P/E states. Here, the AG bias ranges from -2 to 4 V in 1 V steps. FN tunneling is utilized to program and erase the device in this work by applying appropriate biases to the first and second gates while the source and drain are grounded. Regardless of the read mode, a programmed device refers to one in which electrons tunneling from the NW body with the aid of the FN tunneling mechanism are trapped in the nitride layer of the second gate dielectric; for an erased device, some portions of those trapped electrons are removed through tunneling back into the NW body, which then flow to the source and



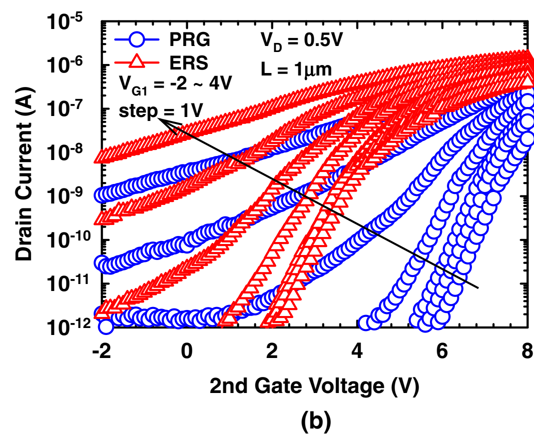


Fig. 3. (Color online) Transfer curves under P/E states with varying AG bias when the device is read by (a) SG-1 and (b) SG-2 modes. Programming and erasing are achieved by applying $V_{G1} = 0$ V and $V_{G2} = 16$ V for 10 ms, and $V_{G1} = 0$ V and $V_{G2} = -12$ V for 100 ms, respectively.

drain, leading to a negative V_{TH} shift compared with the programmed state.

In Fig. 3(a), the device is first programmed by applying $V_{G1} = 0$ V and $V_{G2} = 16$ V for 10 ms, after which the I_D–V_{G1} transfer curves are measured as a function of V_{G2}, resulting in the curves shown as blue circles. Afterwards, $V_{G1} = 0$ V and $V_{G2} = -12$ V are applied for 100 ms to erase the device, and the I_D–V_{G1} transfer curves are again

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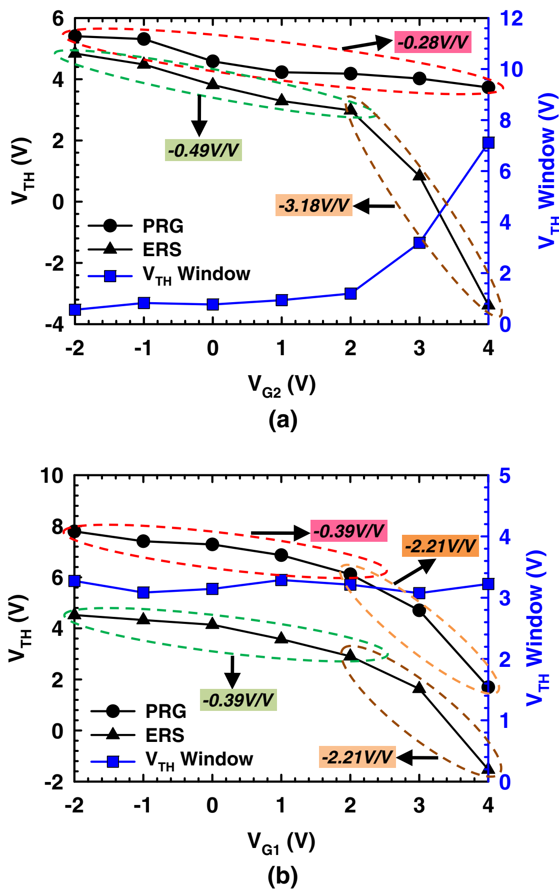

Fig. 4. (Color online) Extracted V_{TH} under programmed and erased states (left vertical axis) from Fig. 3 and V_{TH} window (right vertical axis) as a function of AG bias in (a) SG-1 and (b) SG-2 modes. Depending on the condition of the back surface, the magnitude of γ for each operation regime is indicated.

measured as a function of V_{G2}, giving rise to those shown in red triangles. The results in Fig. 3(b) were obtained in a similar manner except that during the I–V measurement, the roles of the first and second gates are exchanged, compared with those in Fig. 3(a). Defining V_{TH} as the driving gate voltage when the drain current reaches 10 nA, it can be seen from Fig. 3(b) that when the device is driven by the second gate with the ONO stack in the SG-2 mode (i.e., the conventional approach), the extent of the V_{TH} distribution with respect to AG bias is similar in both P/E states. In stark contrast, the V_{TH} of the SG-1 mode (i.e., the unconventional approach) is much less dependent on the AG bias in the programmed state than in the erased state. The V_{TH} versus AG bias characteristics observed in P/E states that correspond to the SG-1 and SG-2 modes are extracted in the left vertical axes of Figs. 4(a) and 4(b), respectively. The V_{TH} window, the difference in V_{TH} between P/E states, is also displayed in Figs. 4(a) and 4(b) in the right vertical axis. One can see that the V_{TH} window under the SG-1 mode shows a sudden increase in AG bias to a value larger than 2 V, whereas that of the SG-2 mode is fairly independent of AG bias.

In addition to the qualitative explanation in ref. 18, the aforementioned phenomena can be described in a more quantitative way using the back-gate effects in ref. 22. The rate of the V_{TH} adjustment by the back gate, the so-called back-gate factor (γ), strongly depends on the condition of the back gate/channel interface where there is a transitional point demarcating two piecewise linear V_{TH}-versus-back-gate-bias curves corresponding to the condition of depletion and inversion of the back surface. Inversion would take place first at the front or back surface for back-gate bias below or larger than this point. The overall behavior of the V_{TH}-versus-back-gate-bias curve is in a way that γ within the range where the AG bias is higher than the transitional point tends to be larger than that of the other portion. In this paper, the AG assumes a role similar to that of the back gate. The slope for each piecewise linear curve in Figs. 4(a) and 4(b), the magnitude of which is equivalent to γ, is labeled.

In the SG-1 mode, the back interface is controlled by the second gate so when the nitride is trapped with electrons in the programmed state, the transitional point shifts to a larger value compared with the erased situation. The curve of V_{TH} against AG bias then mainly shows a horizontal shift, as depicted in Fig. 4(a). Even though this curve does not display a specific point where an obvious change in slope occurs, this point is believed to lie outside the range of the applied V_{G2} and will appear if V_{G2} is further increased. A rather minor vertical shift can occur because the trapped electrons may still slightly affect the electrostatics of the front surface. On the contrary, the V_{TH}–V_{G2} curve for the erased state in Fig. 4(a) exhibits an evident transitional point separating two piecewise linear curves whose respective γ values are 0.49 and 3.18 V/V. Thus, an AG bias range rendering the back surface inverted in the erased state but only depleted in the programmed state (V_{G2} within the range from 2 to 4 V) will increase the V_{TH} window in a linear manner. A similar theory can be applied to SG-2 mode except that the back surface is now essentially unchanged between P/E states, and the V_{TH} against AG bias curve shifts upward as a whole. The V_{TH} window then shows an insignificant variation in the characterized AG bias range. The above statement is clearly illustrated in Fig. 4(b), where one can see that regardless of the state of the device (i.e., programmed or erased), the γ values of the two piecewise linear curves are identical. However, as for Fig. 4(a), γ is 0.28 V/V in the programmed state and is smaller than that in the corresponding regime for the erased state, which is 0.49 V/V. This discrepancy is believed to be caused by the fact that for the applied V_{G2} bias range under the SG-1 mode in the programmed state in Fig. 4(a), the device may have entered into the accumulation situation instead of depletion.[23]

To further probe the impact of such an intriguing effect, the results of P/E speed characterization will next be compared between the two feasible read modes. Programming speed is first depicted in Fig. 5, where for a given programming condition, the characteristics of both the SG-1 and SG-2 modes are measured from the same device. Here, the respective AG biases for the SG-1 and SG-2 modes are $V_{G2} = 3$ V and $V_{G1} = 0$ V since these conditions have comparable V_{TH} windows from Figs. 4(a) and 4(b), and there are two sets of programming conditions utilized in Fig. 5 ($V_{G1} = 0$ V/$V_{G2} = 14$ V and $V_{G1} = 0$ V/$V_{G2} = 18$ V). It can be observed that the V_{TH} shift as read by the SG-1 mode with $V_{G2} = 3$ V is appreciably larger than that of the

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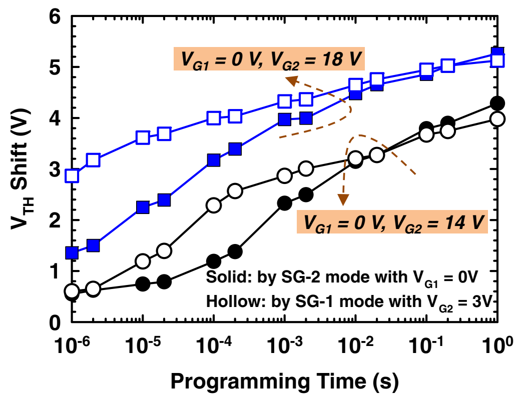

Fig. 5. (Color online) Programming speed comparison between two read modes. The SG-1 mode shows a higher efficiency than the SG-2 mode for up to 20 ms. Programming conditions are $V_{G1} = 0$ V and $V_{G2} = 14$ V, and $V_{G1} = 0$ V and $V_{G2} = 18$ V for curves with circles and squares, respectively.

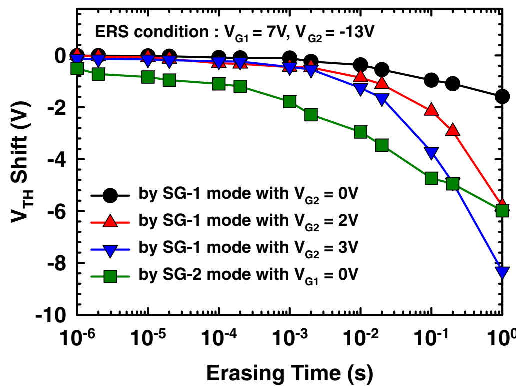

Fig. 6. (Color online) Erasing speed characterization showing that SG-1 mode does not exhibit any V_{TH} shift until 10 ms after which a substantially decreased V_{TH} value is observed for SG-1 mode with $V_{G2} = 3$ V. The erasing speed as read by the SG-1 mode is increased with a larger V_{G2} since inversion would be reached earlier by a larger V_{G2} in a given erasing time.

SG-2 mode with $V_{G1} = 0$ V for at least up to 20 ms of programming time. For the programming condition of $V_{G1} = 0$ V/$V_{G2} = 18$ V applied for 10 µs, the V_{TH} shift in the SG-1 mode is 3.61 V compared with 2.24 V in the SG-2 mode, amounting to a 61% increase in programming speed. On the other hand, for the erasing speed in Fig. 6, a markedly different trend is obtained. The applied biases are $V_{G1} = 7$ V and $V_{G2} = -13$ V for erasure. The reason for choosing such a combination will become clear in the next section. As opposed to the gradually decreasing V_{TH} in the SG-2 mode, SG-1 mode does not exhibit any V_{TH} alteration until around 10 ms, and then a rapidly decreasing V_{TH} is attained when read by the SG-1 mode with $V_{G2} = 3$ V, reaching even smaller V_{TH} over SG-2 mode at 1 s. In fact, the root cause for such a dissimilar P/E speed behavior can also be interpreted on the basis of the back-gate effects. As illustrated in Fig. 7 for the device being read by the SG-1 mode, the initial states before P/E stressing are a fresh [solid line in Fig. 7(a)] and pre-programmed [by applying $V_{G1} = 0$ V and $V_{G2} = 16$ V for 10 msec; dotted line in Fig. 7(b)] device, respectively, for which a V_{G2} bias of 3 V corresponds to the condition of the inversion and depletion [or even

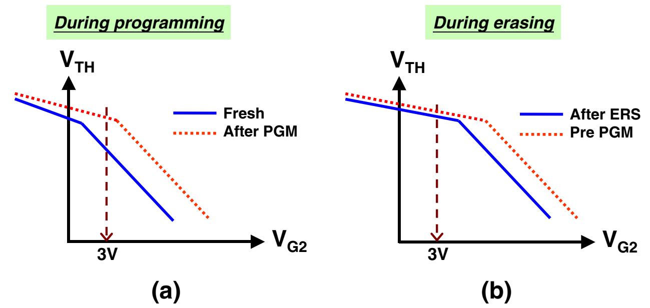

Fig. 7. (Color online) Schematic of the evolution of V_{TH}–V_{G2} curves during (a) programming and (b) erasing when read by SG-1 mode. Owing to the selected V_{G2} (= 3 V) and the back-gate effect, an appreciable V_{TH} shift during programming can initially be obtained compared with a negligible V_{TH} shift during erasing.

accumulation from Fig. 4(a)] of the surface adjacent to the second gate. The dotted line in Fig. 7(a) indicates the V_{TH}–V_{G2} curve when the device has been programmed; while the solid line in Fig. 7(b) represents the V_{TH}–V_{G2} curve when the device has been erased for a particular duration such that the surface governed by the second gate for $V_{G2} = 3$ V is still in the depletion regime.

The V_{TH} differences of the two intersection points determined by the arrow and the two V_{TH}–V_{G2} curves in Figs. 7(a) and 7(b) are by definition the programming and erasing speeds, respectively. It is obvious that the programming speed is much higher than the erasing speed, which can be interpreted as follows. A V_{G2} bias of 3 V that originally inverts the second gate surface for a fresh device would result in the depletion of the second gate surface instead when the device is programmed in Fig. 7(a). On the other hand, the second gate surface is always depleted for $V_{G2} = 3$ V for both the pre-programmed and erased states in Fig. 7(b). Accordingly, a small shift in the V_{TH}–V_{G2} curve in the SG-1 mode will cause a reasonable V_{TH} shift during programming, whereas there will not be any significant V_{TH} shift during erasing until the device is sufficiently erased to the extent that $V_{G2} = 3$ V inverts the surface controlled by the second gate. Considering that the magnitude of γ is strongly related to the chosen operation regime as discussed previously, it is then reasonable to initially observe a higher programming speed yet a lower erasing speed for the unconventional read method as compared with the conventional one. This also explains the increase in erasing speed as read by the SG-1 mode with a larger V_{G2} in Fig. 6, since inversion would be reached earlier by a larger V_{G2} in a given erasing time, and the root cause leading to the SG-1 mode displaying a higher initial programming speed than the SG-2 mode in Fig. 5 is related to the chosen AG bias of the SG-1 mode ($V_{G2} = 3$ V) situated in a regime yielding a large γ in the fresh state, so much so that a more sizable V_{TH} shift between the fresh and programmed states can be attained in the SG-1 mode.

Figure 8 shows the baked retention characteristics of two read approaches. The initial V_{TH} windows are 2.6 and 3.5 V for the SG-2 and SG-1 modes, respectively, and decrease to 0.5 and 1.8 V after 10 year extrapolation. The V_{TH} reduction rate within 10^4 s in the programmed state of the SG-2 mode from 6.7 to 5.8 V is larger than in the programmed state

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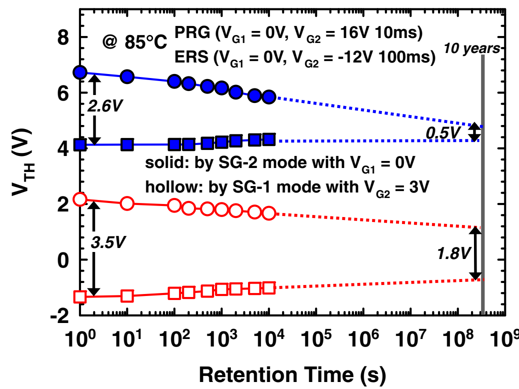

Fig. 8. (Color online) Baked retention characteristics indicating that V_{TH} of the programmed state in SG-1 mode is lowered to a lesser extent than that of SG-2 mode, while these two modes are comparable in terms of their V_{TH} enlargement at erased states.

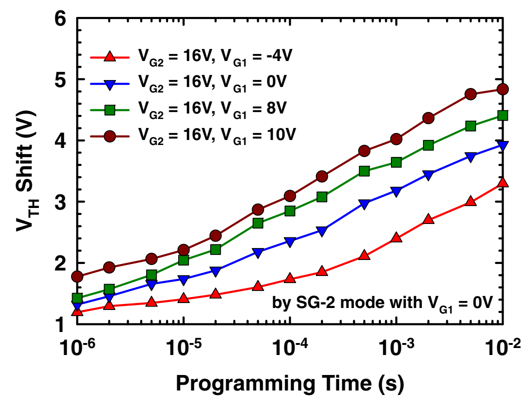

Fig. 9. (Color online) Programming speed characterization as a function of applied V_{G1} during programming stressing. The V_{TH} shift is seen to increase with a larger V_{G1} bias on account of additional number of electrons available for tunneling.

of the SG-1 mode, which is from 2.1 to 1.6 V. It is so as in the SG-1 mode with $V_{G2} = 3$ V, the effective capacitance between the stored charges and the inverted channel consists of a serial combination of tunneling oxide and NW body, which is smaller than the tunneling oxide alone in the SG-2 mode. Hence, an identical amount of charge loss in the programmed state leads to a smaller V_{TH} reduction in the SG-1 mode. For the erased state, inversion tends to occur first at the second gate/channel interface for both modes, so that comparable amounts of V_{TH} uprising are obtained, i.e., 0.3 and 0.2 V for the SG-1 and SG-2 modes, respectively. Simple and straightforward as the concept looks, this is the first time that such a scheme is used to help improve the performance of the NVM device, including the programming speed and retention characteristics. Although the erasing speed is degraded initially for the unconventional read approach, it is believed that this issue could be ameliorated by adjusting γ so that the point where V_{TH} starts to show a decent shift occurs earlier.

It should be emphasized that as will be demonstrated in the next section, the values of applied biases for programming and erasing are not optimized in the above discussion. That is, the programming/erasing speed and V_{TH} window presented hereinbefore are only for proof of concept and only serve as the preliminary assessment of the true potential the proposed technique has to offer. In addition, though our device is based on poly-Si, the underlying principle applies equally well to single-crystalline Si counterparts.

3. Effect of the Auxiliary Gate on P/E Speed

Figure 9 shows the V_{TH} shift versus programming time as a function of V_{G1} that is applied during programming. Here, the device is programmed by applying $V_{G2} = 16$ V and varying V_{G1}, and is read by the SG-2 mode with $V_{G1} = 0$ V. As reported in ref. 18, during programming, a positive AG bias can help induce an additional number of electrons that are available for tunneling into the nitride layer, while a negative one tends to deplete electrons present in the channel. In this regard, the V_{TH} shift for a given programming time in Fig. 9 is seen to increase with the applied AG bias. The effect of AG bias on erasing speed

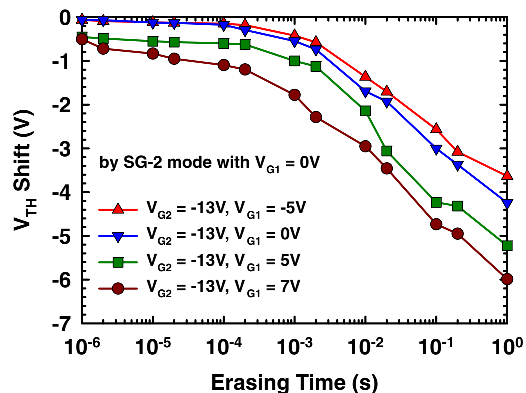

Fig. 10. (Color online) Erasing speed characterization as a function of applied V_{G1} during erasing stressing. The magnitude of V_{TH} shift is seen to increase with a larger V_{G1} bias owing to the reduced resistance experienced by detrapped electrons when flowing to the source/drain.

is also explicit in Fig. 10. It is worth noting that the dependence of erasing speed on AG bias in Fig. 10 is completely opposite to that in ref. 18, where severe electron injection from the gate electrode during erasing due to the use of a thin blocking oxide layer results in a low erasing speed so that the effect of AG bias observed therein may not represent the entire picture. In contrast, the reasonable erasing efficiency in Fig. 10 suggests that the detrimental effect of electron injection is minimized and the merit of AG in increasing the erasing speed is fully demonstrated. Under the erasing scenario, electrons originally trapped in the nitride would be detrapped into the channel and would flow to the grounded source/drain. A larger AG bias facilitates this out-draining process by forming an inverted channel to reduce the channel resistance experienced by the detrapped electrons, which is consistent with the scheme in ref. 24, where a back-gate bias whose value is larger than the V_{TH} of the back channel is applied to erase the front side charges.

One thing to note is that the read mode adopted in this section is the SG-2 mode, but the impact of AG bias on P/E speed will also manifest itself in the SG-1 mode.

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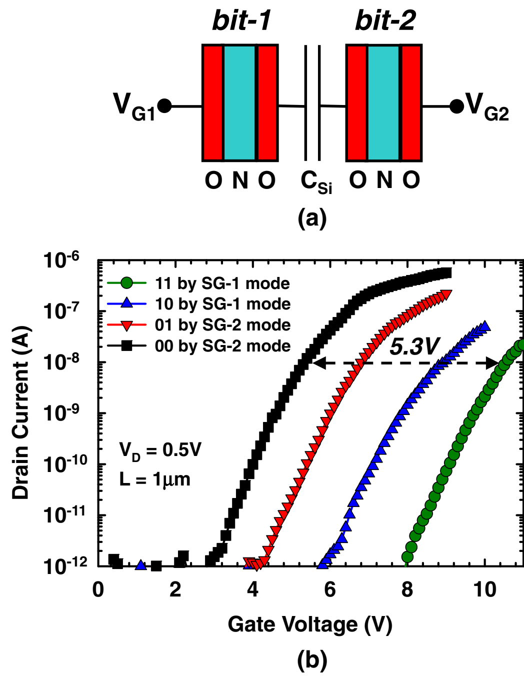

Fig. 11. (Color online) (a) Schematic illustration of the device configuration for 2-bit/cell characterization. Bit-1 and bit-2 refer to the bits located in the nitride of the first and second gate dielectrics, respectively. (b) Four distinguishable states can be observed when the dielectrics of both gates are made up of ONO, thus realizing the 2-bit/cell feature. The V_{TH} difference between state-11 and state-00 is 5.3 V.

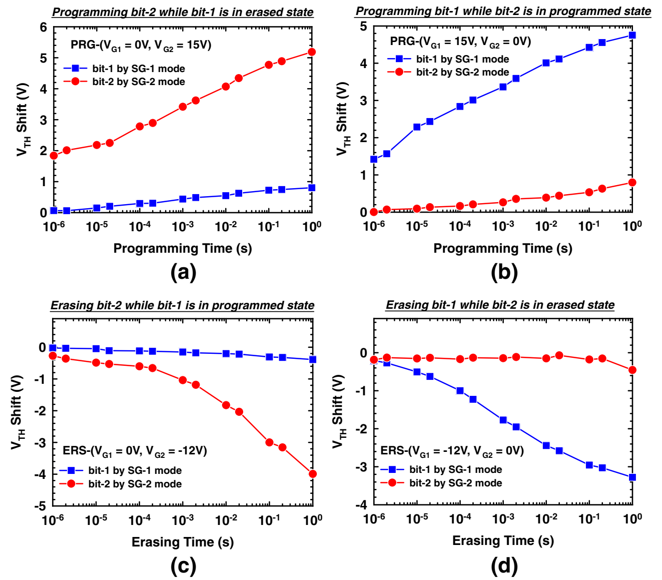

Fig. 12. (Color online) (a, b) Programming and (c, d) erasing disturbance characterization for 2-bit/cell operation. A reasonable P/E speed is attained without a significant disturbance. The measured device has 50-nm-thick NW channels.

4. 2-Bit/Cell Feature

To realize 2-bit/cell functionality in the proposed IDG NW device, 3/8/12 and 3/8/13 nm ONO layers are used as the dielectrics for the first and second gates, respectively. To minimize bit-to-bit coupling effects, the device used for 2-bit/cell measurement is with 50-nm-thick NW channels. With regard to the denomination of two bits, the bits stored in the nitride of the first and second gates are referred to as bit-1 and bit-2, respectively, as illustrated in Fig. 11(a). Moreover, the programmed state is designated as the "1" state and the erased state as the "0" state. As an example, state-11 indicates one in which bit-1 and bit-2 are programmed simultaneously by applying the gate voltage stress $V_{G1} = V_{G2} = 16$ V for 5 ms so that nitride layers in both the first and second gate dielectrics are trapped with electrons. State-10 is attained by erasing bit-2 from state-11 (i.e., removing electrons stored in the nitride of the second gate dielectric) using the stress conditions of $V_{G1} = 0$ V and $V_{G2} = -14$ V for 20 ms. By the same token, state-01 and state-00 are accomplished by erasing bit-1 and bit-1 and 2, from state-11 through applying $V_{G1} = -14$ V and $V_{G2} = 0$ V for 20 ms, and $V_{G1} = V_{G2} = -14$ V for 20 ms, respectively. Characteristics of these four distinguishable states are shown in Fig. 11(b). The V_{TH} difference between state-11 and state-00 is 5.3 V. The read mode assigned for each state is determined by first measuring each state with both modes and then choosing the one that maximizes the V_{TH} difference between states. From another viewpoint, since the SG-1 mode (with the AG bias $V_{G2} = 0$ V) already yields a higher V_{TH} than the SG-2 mode (with the AG bias $V_{G1} = 0$ V) in the fresh state owing to the inherent asymmetry of the proposed device,[19] it is then reasonable that with the aim of enlarging the V_{TH} sensing window, the SG-1 mode is to be used for reading out state-11, whereas the SG-2 mode is to be used for reading out state-00. As for state-10 and state-01, unlike in ref. 24, where an intentionally formed asymmetric structure consisting of two gates with different work functions is exploited to differentiate state-10 from state-01, the device proposed in this paper is inherently asymmetric in terms of the controllability over channels provided by two independent gates.[19] Thus, the SG-1 and SG-2 modes are directly applied to read out state-10 and state-01, respectively. The P/E disturbance characterization shown in Fig. 12 suggests that a reasonable P/E speed can be achieved without significantly altering the state of the other bit.

5. Conclusions

To sum up, impacts of an IDG scheme on a poly-Si NW NVM device are comprehensively analyzed in this paper. The origin of the varying V_{TH} window dependence on AG bias is investigated and found to be a consequence of the back-gate effect. The same effect also explains the distinct P/E efficiency for the two read methods, where it is observed that the unconventional one yields a larger V_{TH} shift within the first 20 ms over the conventional one when being programmed, while no significant V_{TH} shift is attained when being erased until 10 ms. Retention characterization suggests that the unconventional read mode is less vulnerable to V_{TH} window shrinkage. P/E speed is seen to be improved as the applied AG bias becomes larger, which is due to the increased number of electrons available for tunneling into the nitride and the reduced channel resistance experienced by detrapped electrons under programming and erasing scenarios, respectively. Using ONO as the dielectrics for both gates, the 2-bit/cell feature can be realized with a 5.3 V V_{TH} difference between state-11 and state-00.

In addition to the aforementioned features, the IDG scheme could also help eliminate the necessity of applying

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an extremely large voltage to pass transistors in a series string that is typically required to ensure a sufficient read current. This merit also greatly relaxes the stringent requirement that the maximum V_{TH} after programming be safely lower than the read-pass voltage.[25] Moreover, with the aid of process modifications, the proposed concept could also be adopted in devices that are constructed in a vertical scheme.

Note that the P/E speed in this work is far from being optimized. Yet the fabricated device is a test vehicle that is highly beneficial for understanding the characteristics of SONOS under IDG operation. With further optimization of structural parameters to adjust γ for improving the initially retarded erasing speed of the unconventional read approach, the proposed concept combined with the TFT structure appears to be very promising for 3D-stacked high-density memory applications.

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