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Investigation on CDM ESD events at core circuits in a 65-nm CMOS process

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A B S T R A C T

Among three chip-level electrostatic discharge (ESD) test standards, which were human-body model (HBM), machine model (MM), and charged-device model (CDM), the CDM ESD events became critical due to the larger and faster discharging currents. Besides input/output (I/O) circuits which were connected to I/O pads, core circuits also suffered from CDM ESD events caused by coupled currents between I/O lines and core lines. In this work, the CDM ESD robustness of the core circuits with and without inserting shielding lines were investigated in a 65-nm CMOS process. Verified in a silicon chip, the CDM ESD robustness of the core circuits with shielding lines were degraded. The failure mechanism of the test circuits was also investigated in this work.

1. Introduction

The major reliability issue for IC products is the damage caused by electrostatic discharge (ESD) [1,2]. Against ESD damages, on-chip ESD protection circuit must be included in IC products. A general concept of on-chip ESD protection for ICs is shown in Fig. 1 [3,4]. The ESD protection device at input/output (I/O) pad and the power-rail ESD clamp circuit must be provided to accomplish the whole-chip ESD protection.

The ESD robustness of IC products can be tested. The chip-level ESD test standards are known as human-body model (HBM) [5], machine model (MM) [6], and charged-device model (CDM) [7]. The real-case HBM (MM) ESD events are caused from human (machine). The electrostatic charges are initially stored in the human (machine), and then transfer into the IC, when the human (machine) touches the IC. A 2-kV HBM (200-V MM) ESD event can generate an ESD current peak of ~1.3 A (~3.5 A) with a rise time of ~10 ns [8]. The CDM ESD event happens as a certain pin of the IC is suddenly grounded, and the electrostatic charges originally stored within the IC will be discharged through the grounded pin. The typical 1-kV CDM ESD event from a charged IC (with an equivalent 4-pF capacitance to ground) can generate a current peak as high as ~15 A within a rise time of only ~0.2 ns [8]. Among the chip-level ESD test standards, the CDM ESD events play major roles to cause failures in today's manufacturing and packaging environments [9,10]. Therefore, several ESD protection designs against CDM ESD events have been reported to protect the I/O circuits which are directly connected to the external pins [11–13]. Besides the I/O circuits, the core circuits would also suffer the dangers when the CDM ESD events happened at the I/O circuits. As compared with HBM and MM ESD events, the discharging current in CDM ESD event is larger and faster. Such very fast transient ESD pulse will be inherently conducted by the displacement current of capacitor, $I = C \times (dv/dt)$, to the external ground through the path with parasitic capacitance. Therefore, the coupling effects between I/O line and core line should be considered during CDM ESD events. The core circuit may also suffer from ESD stress caused by the coupled current when I/O circuit is stressed by ESD.

Adding the shielding lines near to the signal lines of high-speed circuits is an efficient method to limit the inductive coupling and to reduce the crosstalk noise between signal lines [14]. The signal lines are generally shielded by the shielding lines which are biased at V_{DD} or V_{SS}. However, the coupling effect between the shielding and signal lines during CDM ESD event could induce large transient current to damage the core circuits [15,16]. The coupling effect between I/O line and core line during CDM ESD event can induce large transient current to damage the core circuit, even if the shielding line is inserted. In this paper, the CDM ESD events at core circuits due to coupling effects are investigated in a 65-nm CMOS process.

2. Test circuits

To investigate the CDM ESD events at core circuits due to the coupling effects between I/O line and core line, the test circuit with and without shielding line is shown in Fig. 2. The I/O circuit realized with inverter is connected to the I/O pad through the I/O line with ESD protection device at the I/O pad. The ESD protection device is realized with the gate-grounded NMOS (GGNMOS) of 360 μm/0.12 μm (width/length). The power-rail ESD clamp circuit is included between V_{DD} and V_{SS}. The core circuits without (with)

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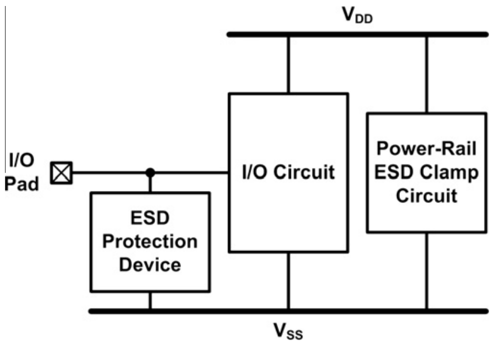

Fig. 1. ESD protection design at I/O pad.

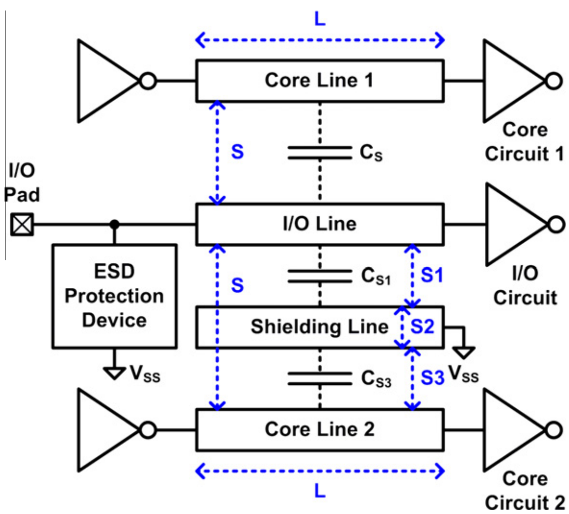

Fig. 2. Test circuit without (with) inserting shielding between I/O line and core line 1 (core line 2).

inserting the shielding line between I/O line and core line 1 (core line 2) are arranged in parallel to the I/O circuit. The I/O line and core line are realized with metal 3, while the shielding line is realized with metal 1 ~ metal 6. The spacing between I/O line and core line is labeled as *S*, and it is split with 0.78 μm and 1.98 μm. The length of I/O line, core line, and shielding line are the same and labeled as *L*. The length of *L* is split with 20 μm, 50 μm, and 100 μm. The spacing between I/O line and the shielding line, the width of shielding metal, and the spacing between the shielding line and the core line are labeled as *S*1, *S*2, and *S*3, respectively. The *S*1 and *S*2 are kept at 0.3 μm and 0.18 μm, respectively, while the *S*3 is split with 0.3 μm and 1.5 μm in the test circuit with shielding line. The split conditions of the test circuits with different *L*, *S*, *S*1, *S*2, and *S*3 are summarized in Tables 1 and 2. Fig. 3 shows the layout top view of one set of test circuits (A5 and B5).

3. CDM ESD test results

All test circuits have been fabricated in a 65-nm CMOS process with the thin-gate oxide of ~20 Å. The test circuits with a die size of ~2 × 1.5 mm^2 have been assembled in DIP-40-pin packages. The CDM ESD stresses are applied by the field-induced CDM tester. The electrostatic charges are stored into the IC, including *P*-substrate and V_{DD} metal bus, and then discharging through a grounded metal probe. The failure criterion is defined as the *I–V* characteristics seen at I/O pad shifting over 30% from its original curve after CDM ESD stressed at every test level. The measured CDM ESD robustness among these test circuits without and with shielding lines are listed in Tables 1 and 2, respectively. The negative CDM ESD robustness of all core circuits exceeded −600 V. The positive CDM ESD robustness of some core circuits without inserting the shielding line exceeded 600 V. Even if the metal length (*L*) of core circuits without inserting shielding is reduced, which leads to the lower impedance and higher overshoot voltage, the positive CDM ESD robustness can still achieve 400 V. However, the positive CDM ESD robustness of core circuits with inserting the shielding lines are seriously degraded to only 100 V.

4. Failure analysis and discussion

The leakage current of the test circuit will increase if the test circuit is failed after CDM ESD stresses. The scanning electron microscope (SEM) was used to find the failure location to cause the large leakage current. The SEM photo of the core circuit in test circuit A1 after 500-V CDM ESD test is shown in Fig. 4. Besides, the

Table 1
CDM ESD robustness of test circuits without inserting the shielding line between I/O line and core line.

Test circuit	*L* (μm)	*S* (μm)	*S1* (μm)	*S2* (μm)	*S3* (μm)	Positive CDM ESD robustness[a] (V)	Negative CDM ESD robustness[a] (V)
A1	20	0.78	N/A	N/A	N/A	400	<−600
A2	20	1.98	N/A	N/A	N/A	>600	<−600
A3	50	0.78	N/A	N/A	N/A	400	<−600
A4	50	1.98	N/A	N/A	N/A	>600	<−600
A5	100	0.78	N/A	N/A	N/A	>600	<−600
A6	100	1.98	N/A	N/A	N/A	>600	<−600

[a] The CDM ESD test voltage was increased in 100-V step.

Table 2
CDM ESD robustness of test circuits with inserting the shielding line between I/O line and core line.

Test circuit	*L* (μm)	*S* (μm)	*S1* (μm)	*S2* (μm)	*S3* (μm)	Positive CDM ESD robustness[a] (V)	Negative CDM ESD robustness[a] (V)
B1	20	0.78	0.3	0.18	0.3	100	<−600
B2	20	1.98	0.3	0.18	1.5	100	<−600
B3	50	0.78	0.3	0.18	0.3	100	<−600
B4	50	1.98	0.3	0.18	1.5	100	<−600
B5	100	0.78	0.3	0.18	0.3	100	<−600
B6	100	1.98	0.3	0.18	1.5	100	<−600

[a] The CDM ESD test voltage was increased in 100-V step.

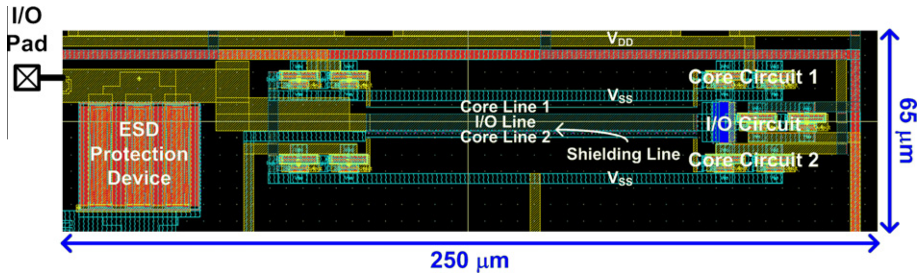

Fig. 3. Layout top view of one test circuit for fabrication in a 65-nm CMOS process with 1-V devices.

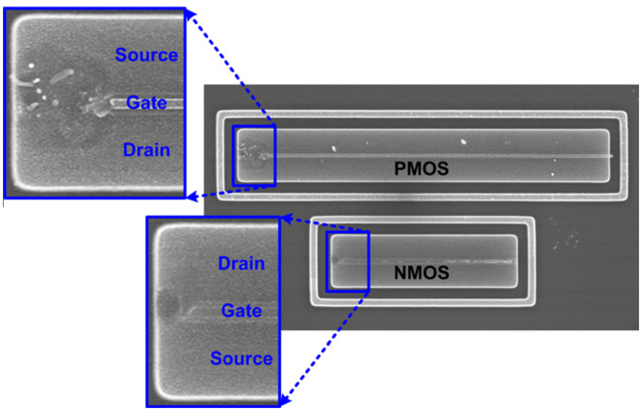

Fig. 4. SEM photo of core circuit 1 in test circuit A1 after 500-V CDM ESD test.

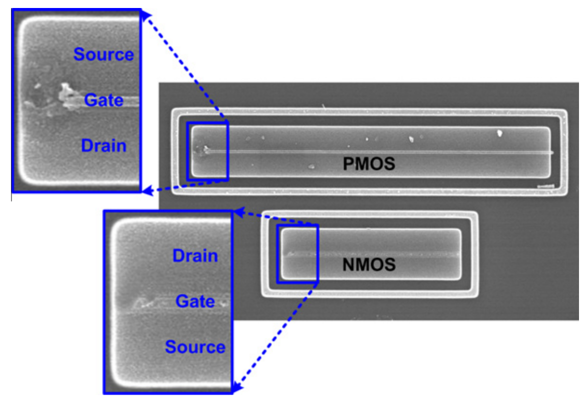

Fig. 6. SEM photo of core circuit 2 in test circuit B6 after 200-V CDM ESD test.

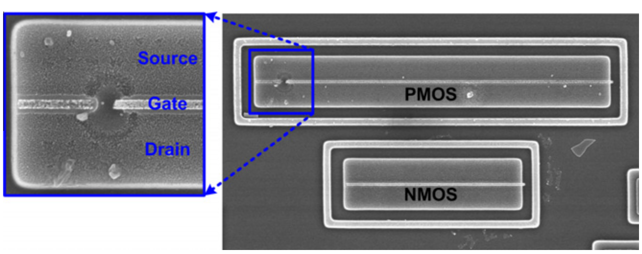

Fig. 5. SEM photo of core circuit 2 in test circuit B5 after 200-V CDM ESD test.

SEM photos of the core circuits in test circuits B5 and B6 after 200-V CDM ESD tests are shown in Figs. 5 and 6, respectively. The failure points are located at the poly gates of transistors in core circuits. The similar phenomena are founded in the other test circuits.

During negative CDM ESD stress, the negative charges located in *P*-substrate and V_{DD} metal bus of core circuit 1 can be discharged through the ESD protection device at the I/O pad, V_{SS} bus, and the power-rail ESD clamp circuit or the *P*+ pickup of NMOS in core circuit 1, as the current paths shown in Fig. 7a. Besides the core circuit 1, the main current discharging paths of negative charges located in *P*-substrate and V_{DD} metal bus of core circuit 2 consist of the ESD protection device, C_{S1}, V_{SS} bus, and the power-rail ESD clamp circuit or the *P*+ pickup of NMOS in core circuit 2, as the current paths shown in Fig. 7b. Although the capacitive current paths (C_S, C_{S1}, and C_{S3}) exist between the gate terminals of core circuits and the I/O pads, the main ESD currents will discharge through the low-impedance paths shown in Fig. 7a and b rather than the C_S and C_{S3} to prevent the gate oxide of core circuits from breakdown under negative CDM ESD stresses. Therefore, the negative CDM ESD robustness of all core circuits exceeded −600 V.

During positive CDM ESD stress, there are multiple current discharging paths from the core circuits to the grounded I/O pad, as shown in Fig. 8a and b. The positive electrostatic charges located in *P*-substrate and V_{DD} metal bus can be conducted through the *P*+ pickup of NMOS in core circuits or power-rail ESD clamp circuit into the V_{SS} bus, and then discharged through the ESD protection device or C_{S1} to external ground, as the dashed lines shown in Fig. 8a and b. However, if the power-rail ESD clamp circuit is located far from the I/O pad, the CDM current will not be efficiently discharged through this path. The positive electrostatic charges located in *P*-substrate and V_{DD} bus may also be conducted through the gate oxide in core circuits to damage the PMOS and NMOS. Without inserting the shielding line, the coupling current through C_S is less. Therefore, only some damages are found at the PMOS and NMOS in core circuit 1 after higher voltage CDM tests, as shown in Fig. 4. After inserting the shielding lines, the coupling effects of C_{S1} and C_{S3} are increased. If the C_{S3} is large enough, the current path consisted of the gate oxide of PMOS, C_{S3}, and ESD protection device or C_{S1} will be more destructive. This discharging current causes the damage on PMOS of core circuit 2, as shown in Fig. 5. If only the C_{S1} is increased, the current path consisted of the gate oxide of PMOS, gate oxide of NMOS, *P*+ pickup of NMOS, and C_{S1} will also be destructive. The damages of core circuit 2 are located at both PMOS and NMOS, as shown in Fig. 6. Therefore, the positive CDM ESD robustness of core circuits with inserting the shielding line are only 100 V in the test circuits. In contrast, the negative CDM ESD robustness was not degraded by inserting the shielding line in chip layout, as compared in Tables 1 and 2.

To prevent from ESD damage at core circuits, ESD protection devices are also needed for core circuits which are close to the I/O circuits, as shown in Fig. 9.

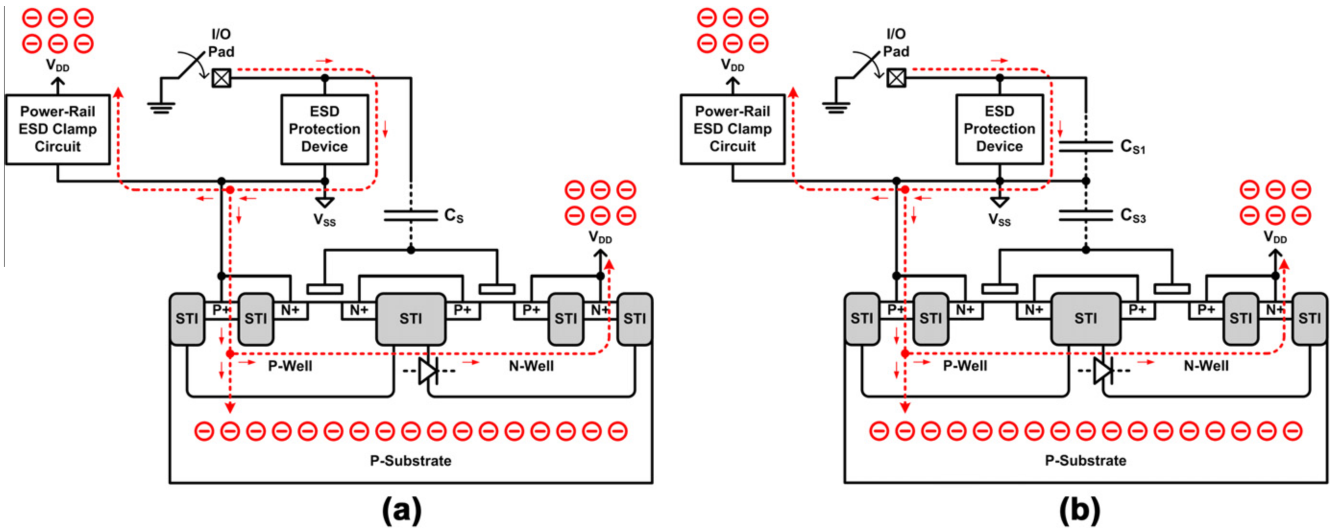

Fig. 7. (a) Core circuit 1 and (b) core circuit 2 under negative CDM ESD event.

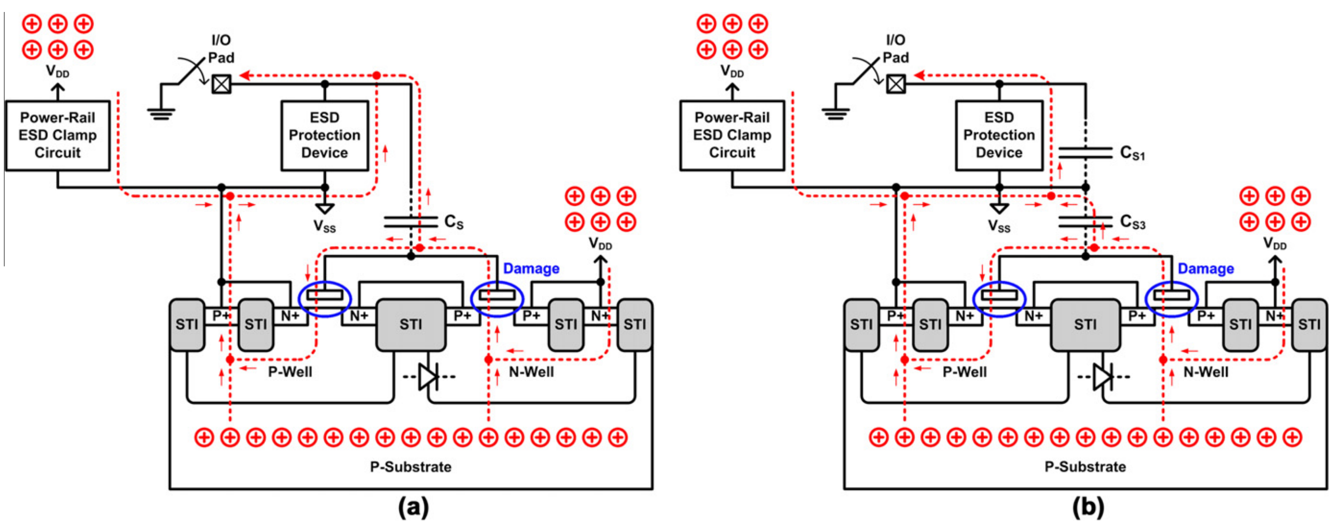

Fig. 8. (a) Core circuit 1 and (b) core circuit 2 under positive CDM ESD event.

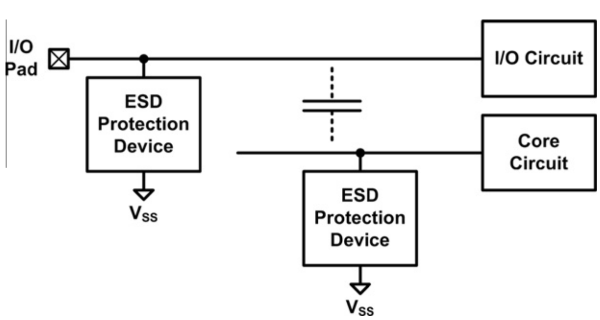

Fig. 9. Core circuit with ESD protection device.

5. Conclusion

In this paper, the CDM ESD issue at core circuit which is not connected to I/O pad has been addressed. The CDM ESD tests are performed to several test circuits fabricated in 65-nm CMOS process. The measured results show that the core circuit also suffers from CDM ESD issue due to the coupled current when I/O circuit is stressed by CDM ESD. The coupling effect during CDM ESD event is even critical to induce larger transient current to damage the core circuits, after inserting the shielding line between I/O line and core line. The failure mechanism is also addressed in this paper. This work can help foundries or IC design houses to improve their IC products with better CDM ESD robustness.

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