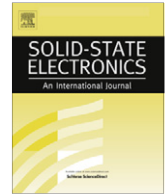
Solid-State Electronics 77 (2012) 12–19

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse



Statistical device simulation of physical and electrical characteristic fluctuations in 16-nm-gate high-κ/metal gate MOSFETs in the presence of random discrete dopants and random interface traps

Yiming Li *, Hui-Wen Cheng

Parallel and Scientific Computing Laboratory, Department of Electrical and Computer Engineering, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 300, Taiwan

A R T I C L E I N F O

Article history:
Available online 26 June 2012

Keywords:
Random discrete dopant
Random interface trap
DC/AC fluctuations
Random effect
High-κ/metal gate
16-nm-gate
MOSFETs
3D device simulation

A B S T R A C T

We estimate the effects of random discrete dopants (RDs) and random interface traps (ITs) on physical and electrical characteristic fluctuations of 16-nm-gate high-κ/metal gate (HKMG) metal–oxide-semiconductor field effect transistors (MOSFETs). Two-dimensional (2D) random ITs at the hafnium oxide (HfO_2)/silicon interface and 3D RDs inside the silicon channel of the 16-nm-gate HKMG MOSFETs are simultaneously incorporated into an experimentally validated 3D device simulation to quantify the RDs-and-ITs-fluctuated characteristics. The random effect of the combined RDs and ITs induces rather different fluctuation in the threshold voltage, the on-/off-state current, and the gate capacitance in the 16-nm-gate HKMG MOSFETs. The surface potential, DC and AC characteristic fluctuations are affected to different extents by the random combinatorial RDs and ITs. Nonlinearly correlated RDs and ITs violate the statistical assumption of independent identical distributions between the RDs- and ITs-induced random variables. Consequently, for the studied 16-nm-gate HKMG N-MOSFETs, the threshold voltage fluctuation induced by the combined RDs and ITs is 11% less than their statistical sum due to local interaction of surface potentials resulting from the RDs and ITs simultaneously. Similarly, it is about 8.9% for the P-MOSFET devices. Depending upon random position and number of the combined RDs and ITs, overestimation or underestimation between the statistical sum of variances and the 3D device simulation is also observed for the drain current and the gate capacitance.

© 2012 Elsevier Ltd. All rights reserved.

1. Introduction

Complementary metal oxide semiconductor (CMOS) device technology scaling and performance improvement follow the Moore's law [1] in the last four decades. Nowadays, continuously pursuing Moore's law requires not only overcoming a variety of fabrication challenges but also suppressing systematic variation and random effects [2,3]. Random dopant fluctuation (RDF), as one of known major intrinsic parameter fluctuations, complicates device scaling and design [4–11] in sub-65-nm CMOS devices era. High-κ/metal-gate (HKMG) technology has been a key way to reduce intrinsic parameter fluctuation and leakage current for sub-45-nm technology nodes. However, depending on different fabrication process, the HKMG approach may associate with random interface traps (ITs) at the high-κ/silicon interface [12–17]. This additional random source may degrade device characteristic; thus, except recent studies on RDF, computational simulation of device variability induced by the random ITs was reported using a simple one-dimensional (1D) model of ITs for sub-65-nm CMOS devices [16] and a 2D model of ITs for 16-nm-gate HKMG devices [17]. Unfortunately, local interaction of the combined RDs and ITs [18,19] and its impact on physical and electrical characteristic fluctuation of 16-nm-gate HKMG planar CMOS devices have not been discussed yet.

In this work, we statistically simulate the interaction of combined random ITs and RDs of 16-nm-gate metal–oxide-semiconductor field effect transistors (MOSFETs) using an experimentally calibrated 3D device simulation [4]. In contrast to 1D interface trap's model, a 2D ITs' model at HfO_2/silicon interface is established and incorporated into 3D device simulation, which is solved with 3D RDs in the device channel at the same time. To examine the insights of the combined RDs and ITs effects, quantum mechanical transport simulation is performed and compared with experimental data by solving a set of calibrated 3D density-gradient equation coupling with Poisson equation as well as electron–hole current continuity equations [4,20,21]. This analyzing technique enables us to explore both the individual and coupling effects of randomly existing RD and ITs on characteristic including fluctuations of the threshold voltage, the on-/off-state current, and the gate capacitance in a unified way. The RDs-, ITs-, and the combined RDs and ITs (denoted as "RDs and ITS")-fluctuated DC/AC characteristics are quite different

* Corresponding author.
E-mail address: ymli@faculty.nctu.edu.tw (Y. Li).

0038-1101/$ - see front matter © 2012 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.sse.2012.05.017

depending on (1) the random number and position of RDs in the channel; (2) the random number and position of ITs at the HfO_2/silicon interface; and (3) the random number and position of combined RDs and ITs appearing at the HfO_2/silicon interface as well as in the channel simultaneously. We assess the threshold voltage fluctuation (σV_{th}), the on-/off-state current ($\sigma I_{on}/\sigma I_{off}$), and the gate capacitance fluctuation (σC_G) with RDs, ITs, and "RDs and ITs" (i.e. 3D device simulation with including the combined RDs and ITs at the same time), respectively, and discuss the effects of random number and position on the aforementioned electrical quantities. The main finding of this study indicates: $\sigma V_{th,\text{"RDs and ITs"}} < (\sigma^2 V_{th,RDs} + \sigma^2 V_{th,ITs})^{0.5}$, where the $\sigma V_{th,\text{"RDs and ITs"}}$ is the combined "RDs and ITs"-induced threshold voltage fluctuation, $\sigma V_{th,RDs}$ is the RDs-induced threshold voltage fluctuation, and the $\sigma V_{th,ITs}$ is the ITs-induced threshold voltage fluctuation, respectively. Such overestimation on the threshold voltage fluctuation is the basic statistical assumption of independent identical distributions for the RDs-induced and ITs-induced random threshold voltages does not hold at all. Similarly, the impact of combined RDs and ITs on the σI_{on}, σI_{off}, and σC_G is estimated and discussed.

This article is organized as follows. In Section 2, we describe the simulation settings for RDs-, ITs-, and "RDs and ITs"-induced characteristic fluctuations. In Section 3, we discuss the findings of this study for the "RDs and ITs"-fluctuated 16-nm-gate CMOS devices. Finally, we draw conclusions and suggest future work.

2. The simulation technique of combined RDs and ITs

According to ITRS roadmap [22], the validated nominal device characteristic of studied 16-nm-gate HKMG MOSFETs is for low operating power. Using an experimentally quantified 3D device simulation [4], we calibrate the threshold voltage of the 16-nm-gate N- and P-MOSFETs to 250 mV. The devices we examined are the 16-nm titanium–nitride (TiN) gate planar MOSFETs (the device width is equal to the gate length of 16 nm which is designed for the most critical assessment) with amorphous-based TiN/HfO_2 gate stack with an effective oxide thickness (EOT) of 0.8 nm, as shown in Fig. 1a. For the RDF simulation, we mainly follow the detail of RDF simulation reported in our recent work [3–7]. As shown in Fig. 1a, the RDs in 3D device channel region are statistically incorporated into device simulation running on our parallel computing system [20]. A procedure for the RDF simulation is shown in Fig. 1b. Note that, for the best accuracy of our analyzing technique, the implemented statistical device simulation technique for estimating characteristic fluctuation has been experimentally validated with silicon data for sub-20-nm devices in our earlier work [4], where the RDs-fluctuated mobility was validated with experimentally measured current–voltage (I–V) data.

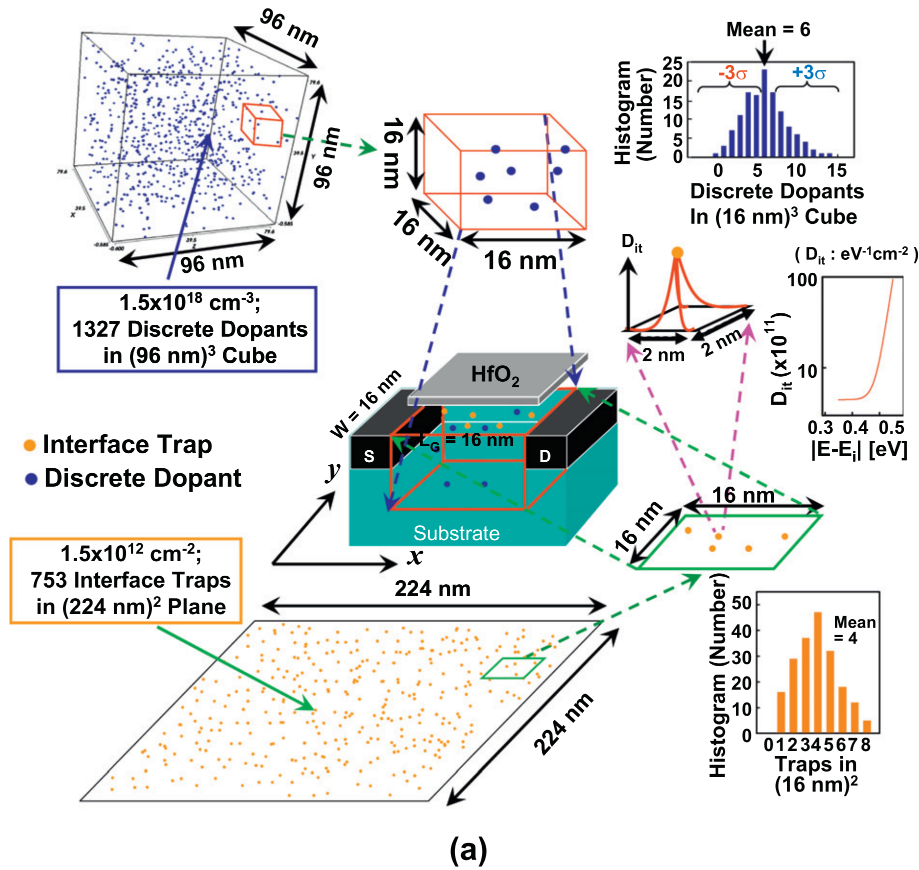
For the simulation of ITs fluctuation (ITF), we first generate 753 acceptor-like traps marked as orange color in a large 2D plane, as shown in Fig. 1a, where the interface trap's concentration in the large plane is around 1.5×10^{12} cm^{-2} (This value is mainly for generating the number of interface traps which is not equal to the effective entire density of interface traps.) and the total number of generated traps follows the Poisson distribution. Then, the statistically random generated large 2D plane is partitioned into many sub-planes, where the number of interface traps in the sub-planes varies from 1 to 8 and the average number of interface traps is 4, as shown in the plot of bar chart with orange color. The energy of each interface trap on a sub-plane is random assigned [12–14,16,17,23]. Thus, each interface trap's density is estimated according to its randomly assigned energy. Consequently, the entire density of interface traps (D_{it}) varies randomly in the range of [1×10^{10} eV^{-1} cm^{-2}, 1×10^{12} eV^{-1} cm^{-2}] which almost coincides with our experimental characterization for sub-20-nm HKMG CMOS devices. We repeat this process until all sub-regions are assigned, where a procedure for the ITF simulation setting is shown in Fig. 1c.

The randomly generated ITs at HfO_2/silicon interface are simultaneously combined with the discrete dopants inside the 3D device channel for the statistical 3D device simulation. To examine the insights of the combined RDs and ITs effects with proper quantum mechanical effects, the quantum mechanical transport simulation is performed by numerically solving a set of calibrated 3D density-gradient equation coupling with Poisson equation as well as electron–hole current continuity equations [4,20,21]. Thus, randomly generated hundreds 3D device samples are simulated to estimate the influence of the "ITs and RDs"-induced DC and AC characteristic fluctuations.

3. Results and discussion

Fig. 2 shows the "RDs and ITs"-fluctuated drain current–gate voltage (I_D–V_G) curves for the studied 16-nm-gate N- and P-MOSFETs, where the solid lines show the nominal I_D–V_G curves, the bars are the results of "RDs and ITs"-fluctuated devices. We note that, as shown in Fig. 2, the normalized on- and off-state currents (σI_{on} and σI_{off}) of the N-MOSFETs are 9.75% and 90.97%. For the P-MOSFETs, σI_{on} and σI_{off} are 17.3% and 76.93%, respectively. The fluctuation of drain current is minimized when the gate voltage is increased. It was reported that the screening effect can suppress the RDF for devices under strong inversion [10,11]. The magnitude of σI_{on} induced by the "RDs and ITs" still has 17% because the ITs locating at HfO_2/silicon interface may destroy the screening effect. If only ITs appear at HfO_2/silicon interface, the V_{th} is simply raised [24]; however, the concurrently existing RDs inside the device channel complicate the V_{th} as well as the I_D–V_G, as shown in Fig. 2. The statistically simulated I_D–V_G curves enable us to extract the σV_{th}, induced by different sources of fluctuations. Table 1 summarizes the RDs-, ITs- and the "RDs and ITs"-induced threshold voltage fluctuations of the studied 16-nm-gate N- and P-MOSFETs. The device exhibits $\sigma V_{th,RDs}$ = 43 mV, $\sigma V_{th,ITs}$ = 26.3 mV and $\sigma V_{th,\text{"RDs and ITs"}}$ = 45.4 mV. We note $\sigma V_{th,\text{"RDs and ITs"}}$ = 45.4 mV is smaller than the result calculated by $(\sigma^2 V_{th,RDs} + \sigma^2 V_{th,ITs})^{0.5}$ = 50.4 mV in which the random variables follow statistically independent identical distribution (*iid*) is assumed. However, the *iid* assumption on the random variables of $V_{th,RDs}$ and $V_{th,ITs}$ is not always true owing to local interaction of surface potentials between RDs and ITs concurrently existing in the surface/channel region of the N-MOSFETs. The relative error between the statistical sum of V_{th}'s variances and the 3D simulation is calculated by the expression: Error = $((\sigma^2 V_{th,RDs} + \sigma^2 V_{th,ITs})^{0.5} - \sigma V_{th,\text{"RDs and ITs"}})/\sigma V_{th,\text{"RDs and ITs"}} \times 100\%$. It is about 11% overestimation compared with the $\sigma V_{th,\text{"RDs and ITs"}}$ of the N-MOSFETs; similarly, for the studied 16 nm P-MOSFETs, $\sigma V_{th,\text{"RDs and ITs"}}$ = 45.1 mV is smaller than the statistically sum $(\sigma^2 V_{th,RDs} + \sigma^2 V_{th,ITs})^{0.5}$ = 49.1 mV. The σI_{on} and σI_{off} induced by RDs, ITs, and "RDs and ITs", respectively, for the studied CMOS devices are listed in Table 1.

Owing to sizeable threshold voltage fluctuation, the statistical sums of the variances of two random variables induced by RDs and ITs disclose significant errors, compared with the 3D device simulation together with the combined RDs and ITs. The large relative errors of σI_{on} and σI_{off} direct to the random number and position effects of combined RD and ITs. Therefore, to understand the influence of local interaction of surface potentials, we further examine the RDs-, ITs-, and "RDs and ITs"-induced surface potentials and the conducting current densities, respectively. The off-state (V_D = 0.8 V and V_G = 0 V) potential distributions and the on-state (V_D = V_G = 0.8 V) current densities for the N-MOSFETs with three different variability sources: RDs and ITs, and combined



753 acceptor-like interface traps are generated in a large 2D plane (size is 224 nm)^2) for N-MOSFETs

↓

The Interface trap's concentration is around $1.5\text{x}10^{12}$ cm^{-2} and the total number of interface traps follows the Poisson distribution

↓

Partition the entire 2D plane into (16 nm)^2 sub-planes

↓

Energy of each Interface trap is assigned according to the distribution of its density

↓

Map the partitioned 196 sub-planes into HfO_2/Si interface randomly

(c)

Discrete dopants are randomly distributed in a large 3D cube (size is (96 nm)^3) with an average concentration of $1.5\text{x}10^{18}$ cm^{-3}

↓

1327 discrete dopants are within the large cube and the number of discrete dopants varies from 0 to 14 (the average number is 6)

↓

Map the partitioned 216 sub-cubes (size is (16 nm)^3) into the device's channel region randomly

(b)

Fig. 1. (a) The two sources of randomness (orange dots are interface traps and blue dots are discrete dopants) and statistical 3D device simulation settings for the fluctuations of random ITs and RDs. We first generate 753 acceptor-like traps in a large plane for N-MOSFET devices, where the interface trap's concentration in the plane is around 1.5×10^{12} cm^{-2} and the total number of generated interface traps follows the Poisson distribution. The energy of each interface trap on the plane is independently assigned according to the distribution of its density. Then, the entire plane is partitioned into sub-planes (size: 16 nm × 16 nm), where the number of interface traps in each sub-plane may vary from 1 to 8 and the average number is 4. Thus, the effective density of interface traps (D_{it}) is in an order of 10^{11} eV^{-1} cm^{-2}. For the settings of discrete dopants, impurities are randomly generated and distributed in (96 nm)^3 cube with the average concentration of 1.5×10^{18} cm^{-3}. There will be 1327 discrete dopants within the cube and the number of discrete dopants varies from 0 to 14 (the average number is six) for all 216 sub-cubes. The size of each sub-cube is (16 nm)^3. The total sub-cubes and sub-planes are then mapped into device's 3D channel and 2D surface for RDs and ITs' position and number simulations. (b) and (c) are the procedures for setting the RDs and ITs in the statistical device simulation.

RDs and ITs are shown in Fig. 3a–c, respectively. Inside the silicon channel (just below the channel surface), there are 8 RDs (blue discrete dopants) and the circled RD near channel surface fluctuates the surface potential, as shown in the upper left plot of

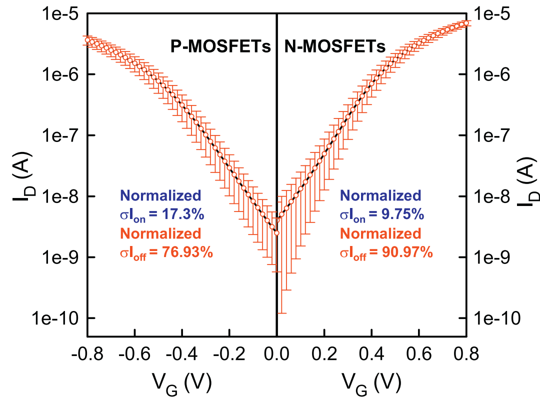


Fig. 2. The I_D–V_G curves fluctuated by the combined RDs and ITs simultaneously for the 16 nm N- and P-MOSFETs, where the solid lines show the nominal case of I_D–V_G curves, the bars are the RDs and ITs fluctuated results. The normalized σI_{on} and σI_{off} of the N-MOSFETs are 9.75% and 90.97%. For the P-MOSFETs, σI_{on} and σI_{off} are 17.3% and 76.93%, respectively. The fluctuation of drain current is reduced when the gate bias is increased.

Fig. 3a, where the absolute value of local spike is 0.4492 eV (i.e. $|\text{potential}_{(\text{at the RD-induced peak})} - \text{potential}_{(\text{at the source end; } x = 0\text{ nm})}| = |-0.0941-(-0.5433)| = 0.4492$ eV). The associated low current density is found around the local spike of potential barrier as shown in the lower right plot of Fig. 3a. The surface potential fluctuated by 4 ITs (orange interface traps), as shown in the upper left plot of Fig. 3b, results in an absolute value of spike of 0.4372 eV which is larger than that of RDs because all ITs locating at HfO_2/silicon interface. The conducting current paths from the source end (S) to the drain end (D) are obstructed by the existing ITs, as shown in the lower right plot of Fig. 3b. By considering the same location of the RDs and ITs above, as shown in the lower left pattern of Fig. 3c, the device possesses rather different potential profile and current density induced by the combined 8 RDs and 4 ITs. The local interaction effect of the combined RDs and ITs on the potential profile has an enhanced peak of localized spikes. The 3D simulated absolute values of the local barrier's peak are 0.4627 eV and 0.4611 eV induced by the combined RDs and ITs, as shown in the upper left plot of Fig. 3c, where the potential profile has about 8.9% enhancement; cutting from S to D, 1D potential profiles passing through the peak of each spike with respect to the aforementioned three cases are shown in the upper right plots of Fig. 3a–c. Note the coverage range of localized spikes in the upper right plot of Fig. 3c is broadened owing to nonlinear potentials' interaction resulting from the combined RDs and ITs. Consequently, the vortex-like on-state current density spreads apart from S to D, as shown in the lower right plot of Fig. 3c. This investigation shows that the local interaction of surface potentials owing to different sources of fluctuations and the combined RDs and ITs could not be calculated independently. This further explains why the *iid* assumption overestimates the threshold voltage fluctuations induced by the combined RDs and ITs.

The impacts of space charge and interaction between RD and IT are also explored. For example, the potentials in the case ⟨1′⟩, the case ⟨2′⟩, and the case ⟨3′⟩ are fluctuated by 1 IT locating at HfO_2/silicon interface, 1 RD and 1RD at 2 and 4 nm below the surface, respectively, as shown in Fig. 4a. If we consider the effect of combined ⟨1′⟩ and ⟨2′⟩(denoted as ⟨1′⟩ + ⟨2′⟩) with a line-up location at near the channel surface , the potential difference is increased due to the interaction between RD and IT, as shown in Fig. 4b, where the difference values of corresponding potential are summarized in Table 2. Replaced the IT by a RD at very similar place near the channel surface, the increment of potential difference is more obvious owing to the increase of space charges, as shown in the combined ⟨2′⟩ and ⟨3′⟩(denoted as ⟨2′⟩ + ⟨3′⟩). It implies that the coupling effect induced by RD and RD is larger than the interaction between RD and IT. Besides, the calculated V_{th} of the cases ⟨1′⟩ + ⟨2′⟩ and ⟨2′⟩ + ⟨3′⟩ are 0.312 and 0.362 V which are different from their statistical sum: the case of ⟨1′⟩ and ⟨2′⟩ is: $(0.196^2 + 0.304^2)^{0.5} = 0.362$ V and the case of ⟨2′⟩ and ⟨3′⟩ is $(0.304^2 + 0.298^2)^{0.5} = 0.426$ V. It confirms that the fluctuation sources should be considered at the same time in order to get proper fluctuation estimations.

Fig. 5a shows the "RDs and ITs" fluctuated I_{on}–I_{off} characteristics of the N- and P-MOSFETs, respectively. Each symbol indicates the result induced by the combined RDs and ITs. The inset log–log plot shows the scatter relationship for the N- and P-MOSFETs. We consider the N-MOSFETs, as shown in Fig. 5a, to examine the random number and position effects, where orange dots are ITs and blue dots are RDs. Among all simulation cases, the randomly selected two cases of the "RDs and ITs" with similar I_{off} but different I_{on} are shown in Fig. 5b and c. The large random number of the "RDs and ITs" increases the threshold voltage and thus reduces the level of drain current density as shown in Fig. 5b, b' and b". 5 RDs in Figs. 5b and 6 RDs in Fig. 5c are deep into channels which contribute insignificant fluctuation to the surface potentials. In contrast with RDs, the ITs locating at HfO_2/silicon interface alter the local spike of surface potential; in particular, for ITs near the source end, as shown in Fig. 5b' and 5c'. There are 6 ITs in the case of Fig. 5b, but the impact of most ITs near the drain end on surface potential is dominated and suppressed except those near the source end. Fig. 5b' discloses that fluctuation of surface potential is suppressed when these ITs are away from S of the channel. Notably, the ITs near the drain end do not have significant potential fluctuations owing to applied high drain bias. On the other hand, ITs locating near S may locally capture the conducting electrons

Table 1
Summary of various fluctuations of the V_{th}, the I_{on}, and the I_{off} induced by RDs, ITs, and "RDs and ITs", respectively, for the studied 16-nm-gate HKMG N- and P-MOSFETs. The statistical sums of the variances of two random variables induced by RDs and ITs show different errors, compared with the results of the 3D device simulation with combined RDs and ITs. The relative error between the statistical sums of the variances of the V_{th} and the 3D simulation of the V_{th} is calculated by the expression: Error = $((\sigma^2 V_{th,RDs} + \sigma^2 V_{th,ITs})^{0.5} - \sigma V_{th,\text{"RDs and ITs"}})/\sigma V_{th,\text{"RDs and ITs"}} \times 100\%$. Similarly, we can calculate the relative errors of the on- and off-state currents. The unit of σV_{th} is mV and the unit of σI_{on} and σI_{off} is A.

	$V_{th,RDs}$	$V_{th,ITs}$	$(\sigma^2 V_{th,RDs} + \sigma^2 V_{th,ITs})^{0.5}$	$\sigma V_{th,\text{"RDs and ITs"}}$	Error (%)
N-MOSFETs	43	26.3	50.4	45.4	+11
P-MOSFETs	41	27.1	49.1	45.1	+8.9
	$\sigma I_{on,RDs}$	$\sigma I_{on,ITs}$	$(\sigma^2 I_{on,RDs} + \sigma^2 I_{on,ITs})^{0.5}$	$\sigma I_{on,\text{"RDs and ITs"}}$	Error (%)
N-MOSFETs	7.51×10^{-7}	6.99×10^{-7}	1.03×10^{-6}	1.09×10^{-6}	−2.8
P-MOSFETs	3.75×10^{-7}	5.29×10^{-7}	6.48×10^{-7}	4.42×10^{-7}	+46.6
	$\sigma I_{off,RDs}$	$\sigma I_{off,ITs}$	$(\sigma^2 I_{off,RDs} + \sigma^2 I_{off,ITs})^{0.5}$	$\sigma I_{off,\text{"RDs and ITs"}}$	Error (%)
N-MOSFETs	2.94×10^{-9}	7.81×10^{-10}	3.04×10^{-9}	1.83×10^{-9}	+66.1
P-MOSFETs	2.03×10^{-9}	5.13×10^{-10}	2.09×10^{-9}	2.50×10^{-9}	+16.4

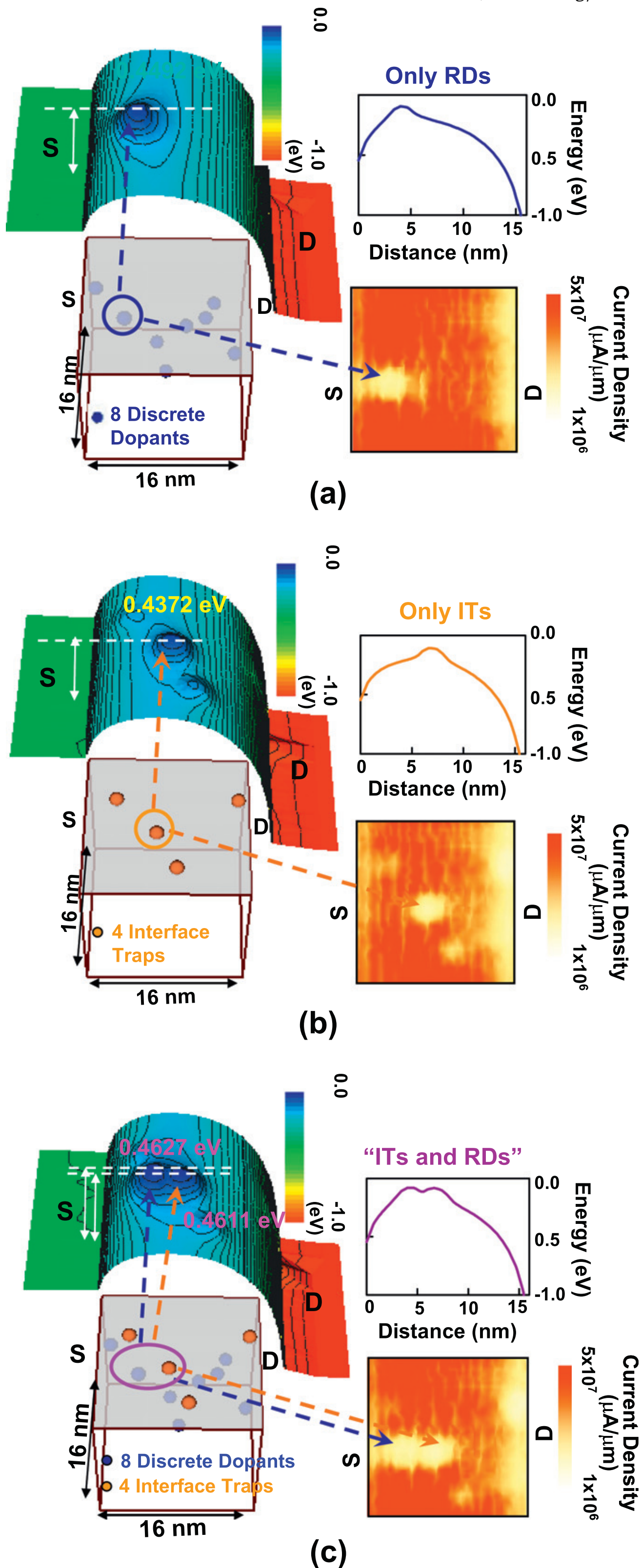
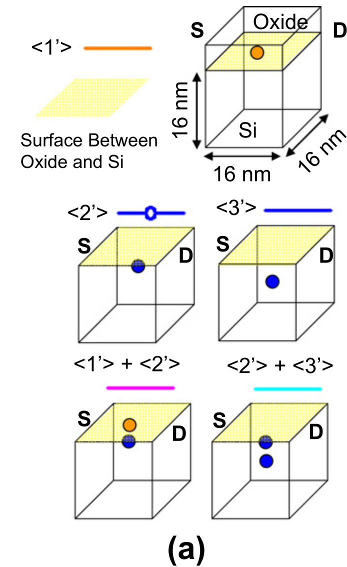


Fig. 3. The off-state (V_D = 0.8 V and V_G = 0 V) potential distributions and the on-state (V_D = V_G = 0.8 V) current densities of the channel surface for the simulated 16-nm-gate devices with only RDs, only ITs, and combined RD and ITS, respectively. As shown in the lower left plots, the devices are fluctuated by (a) 8 RDs locating inside the silicon channel below the channel surface, (b) 4 random ITs at HfO_2/silicon interface, (c) and 12 combined RDs and ITs simultaneously. As shown in the upper left plots, the local interactions of surface potentials resulting from the RDs, ITs, and the combined RDs and ITs exhibit different band profile, measuring from the source (S) to drain (D), and current density, as shown in the right plots. In particular, the combined RDs and ITs complicate the local spikes of the surface potentials.



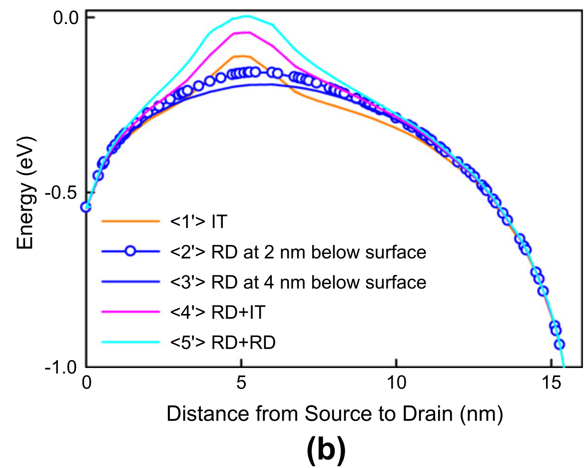


Fig. 4. (a) The schematics of channel and (b) corresponding potentials fluctuated by 1 IT at the interface (the case ⟨1′⟩), 1 RD located 2 (the case ⟨2′⟩) and 4 (the case ⟨3′⟩) nm below the surface, the combined case of ⟨1′⟩ + ⟨2′⟩, and the case of ⟨2′⟩ + ⟨3′⟩, respectively. All surface potentials are extracted from the source end to the drain end, where the RDs and/or IT are locating at x = 5 nm.

from S to D and results in a repulsive barrier well around ITs, as shown in the areas of local spikes in Fig. 5b' and c'. The electron is forced to change its conducting path because it cannot transport from S to D directly depending on those ITs near S owing to locally weakened energy and altered velocity, as shown in the areas of low-level current densities in Fig. 5b" and c". Consequently, the cases of Fig. 5b and c have similar I_{off}, as shown in Fig. 5b' and c' but different I_{on}, as shown in Fig. 5b" and c". The nonlinear coupled capturing and obstructing effects induced by the "RD and ITs" have clearly shown in Fig. 3c. Similarly, Fig. 5c and d are two cases of the "RDs and ITs" with similar I_{on} but different I_{off}. These two cases have the same number of the "RDs and ITs" (they have 1 ITs and 6 RDs), but their I_{off} is different owing to random position of ITs. The device with ITs near the source end, as shown in Fig. 5c, has relatively stronger local spike of potential compared with the case shown in Fig. 5d. For the on-state current, the conducting areas are very similar, as shown in Fig. 5c" and d"; therefore, Fig. 5c and d have similar I_{on}. In summary, the random position effect of the "RDs and ITs" induces rather different fluctuation in spite of the same number of the "RDs and ITs". All plots of the off-state potential and the on-state current density are extracted at the channel

Table 2
Summary of V_{th} and potential difference induced by 1 IT at the interface (the case ⟨1′⟩), 1 RD located at 2 nm (the case ⟨2′⟩) and 4 nm (the case ⟨3′⟩) below the surface, the combined case of ⟨1′⟩ + ⟨2′⟩, and the case of ⟨2′⟩ + ⟨3′⟩, respectively.

	⟨1′⟩ 1 IT at the interface	⟨2′⟩ 1 RD at 2 nm below the surface	⟨3′⟩ 1 RD at 4 nm below the surface	⟨1′⟩ + ⟨2′⟩	⟨2′⟩ + ⟨3′⟩
V_{th} (V)	0.196	0.304	0.298	0.312	0.362
Potential difference (eV)	0.4332	0.3845	0.3522	0.5392	0.5433

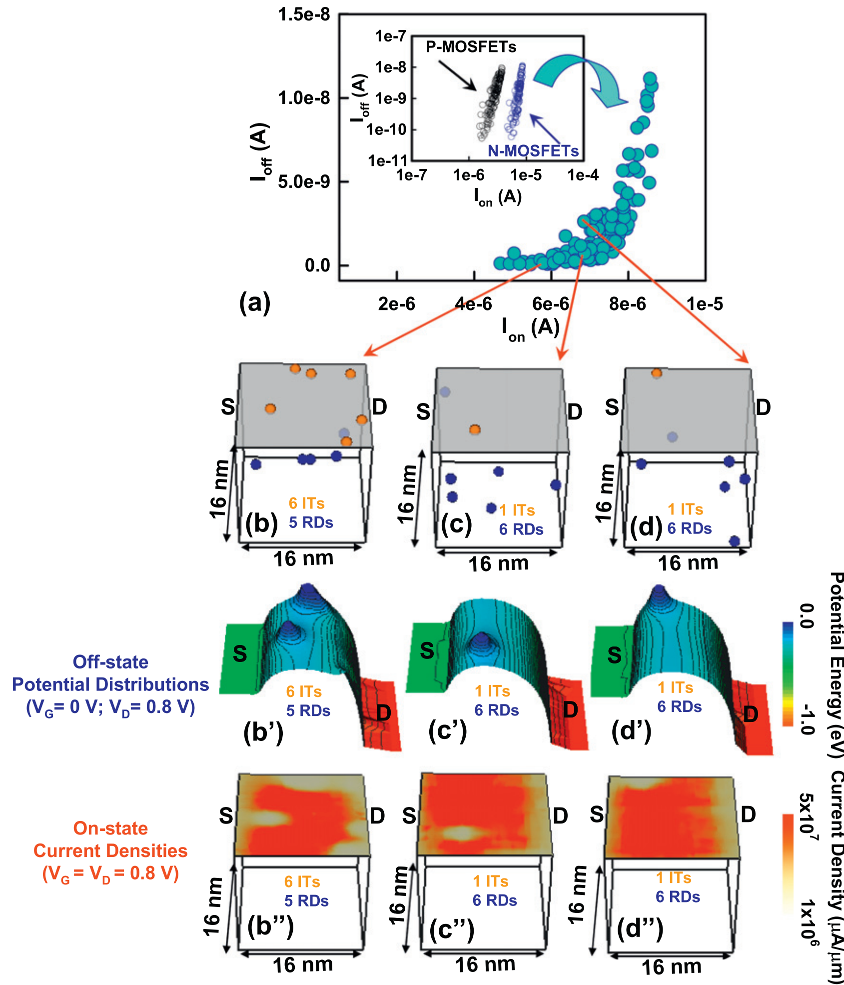


Fig. 5. (a) Plot of I_{off} versus I_{on} of the simulated N- and P-MOSFETs, where each symbol indicates the result induced by the combined RDs and ITs. The inset is the log–log plot to show the scatter relationship. Without loss of generality, we consider the N-MOSFETs in examining the random number and position effects, where orange dots are ITs and blue dots are RDs. (b) and (c) represent two cases of RDs and ITs with similar I_{off} but different I_{on}. (c) and (d) are two cases of RDs and ITs with similar I_{on} but different I_{off}. The corresponding off-state potentials and on-state current densities of (b), (c), and (d) are shown in (b'), (c'), (d') and (b'), (c'), (d'), respectively. All plots of the off-state potential and the on-state current density are extracted at the channel surface.

surface. The σI_{on} and σI_{off} of the N- and P-MOSFETs induced by the RDs, ITs and "RDs and ITs" are summarized in Table 1, respectively, including their statistical sums of variances.

For the AC characteristic fluctuation, the gate capacitance–voltage (C_G–V_G) of the RDs-, ITs-, and "RDs and ITs"-fluctuated 16-nm-gate N-MOSFETs are shown in Fig. 6a, d and g, where the red lines show the nominal capacitances, the gray dashed lines are the fluctuated results, and the solid lines with symbols are the averaged values of all fluctuated cases. For the RDs-induced C_G fluctuation, as shown in Fig. 6a, the lateral shift and the change of shape are observed for the C_G–V_G curves; the shape variation of the C_G curves is resulted from the placement of RDs in the channel depletion region. The lateral shift of the C_G curves is due to V_{th}'s variation. Fig. 6b and c shows the C_G curves and associated variations for the devices with the number of RDs less than or equal to the averaged number 6 and for the devices with the number of RDs more than 6. The RDs-induced C_G fluctuations are suppressed for the devices under high gate bias. As shown in Fig. 6c, the devices with the number of RDs more than 6 have significant C_G fluctuation in the linear region. For the impact of only ITF, the lateral shift of the C_G curves is owing to random number effect of ITs. The slight change of C_G's shape could be attributed to different position effect of ITs at HfO_2/silicon interface, as shown in Fig. 6d. Below the linear region, both the cases in Fig. 6e and f have minimized C_G's fluctuation which is different from the influence of RDs; however, the C_G's fluctuation appear when the devices enter strong inversion because the ITs capture the induced electrons, destroyed the formulated inversion layers, and weaken the screening effect, where the large number of ITs is severe, compared with the cases of ITs less than or equal to the averaged number 4. Not shown here, the asymmetric shape variation of C_G curves is owing to random ITs near the source or drain sides. For the local interaction effect

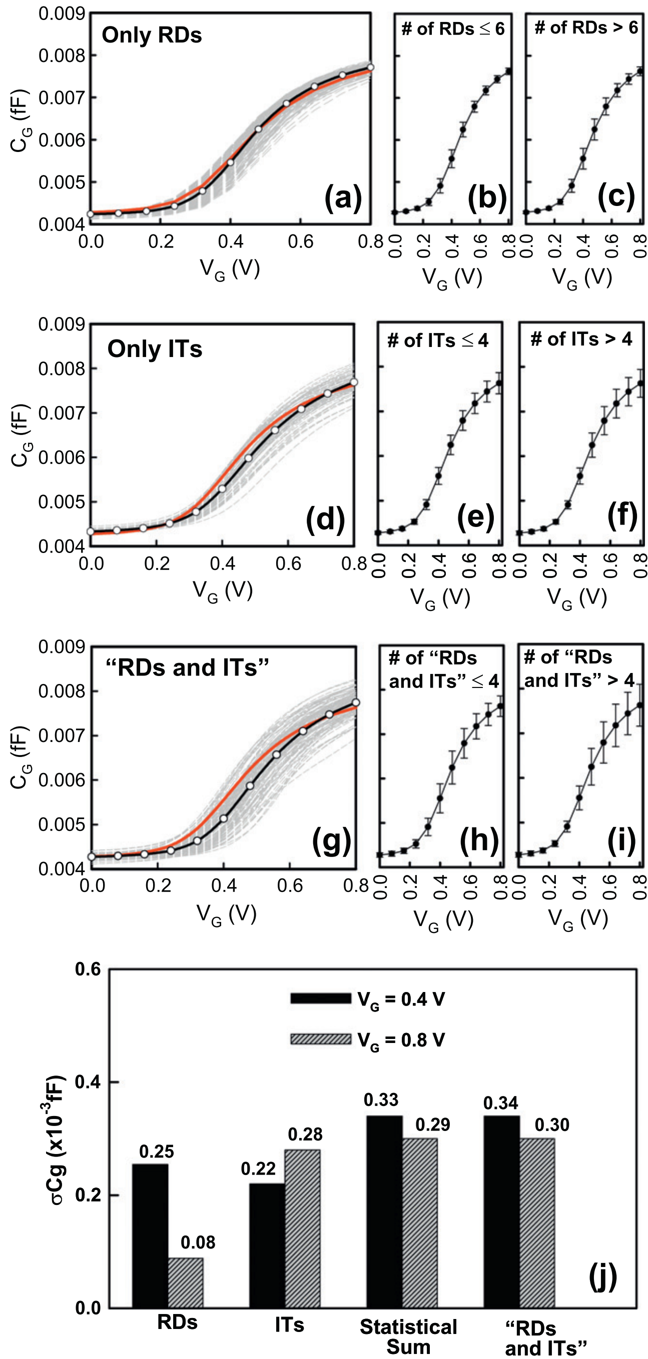


Fig. 6. Plots of gate capacitance–voltage (C_G–V_G) of the RDs-, ITs- and "RDs and ITs"-fluctuated 16-nm N-MOSFETs are shown in (a), (d), and (g), respectively, where the red lines are the nominal cases with respect to different settings and the black lines are the averaged results accordingly. (b) is the plot for the cases with the number of RDs is less than or equal to the average number 4 and (c) is the plot for the number of RDs is more than the average number 4. Similarly, (e) and (f) are for ITs, and (h) and (i) are for the combined RDs and ITs. (j) plot of the gate capacitance fluctuation of the simulated N-MOSFETs induced by RDs, ITs and combined RDs and ITs under V_G = 0.4 V and 0.8 V. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

of the combined RDs and ITs, the significantly lateral shift and change of shape for the curves of C_G–V_G are shown in Fig. 6g. The combined RDs and ITs affect the C_G curves nonlinearly, as shown in Fig. 6h and i, which should be modeled for nano-CMOS circuit simulation. The various fluctuations of gate capacitance obtained from Fig. 6a–i with respect to different gate bias are listed in Fig. 6j. Result shows that the device operates under the saturation region may suffer from the less gate capacitance fluctuation, where the screening effect of inversion layer of device screens the fluctuation of gate capacitance for the cases of RDF. However, for the cases of ITF, the σC_G keeps similar values in both the low and high fields which can not be screened due to ITs are right at the HfO_2/silicon interface. The σC_G induced by the "RDs and ITs" is obviously dominated by ITs under the saturation operation.

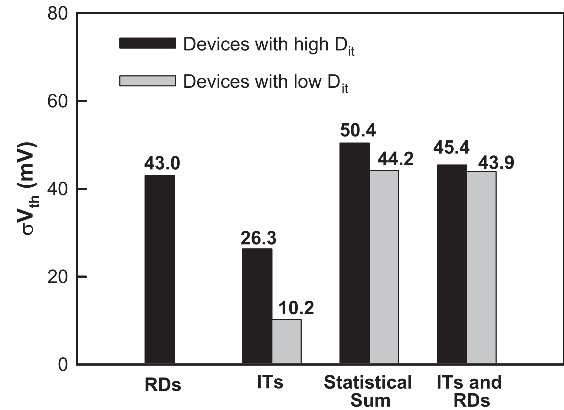


Fig. 7. The σV_{th} induced by the combined ITs and RDs, where the interface traps have high and low D_{it}.

Both the DC and AC characteristic fluctuations indicate the impact of ITs on device variability is significant. In order to study the fluctuation of devices with low D_{it}, a tenth of originally studied D_{it} is performed. Fig. 7 shows the σV_{th} induced by the RDs, ITs, and the combined RDs and ITs, where the interface traps have high (the originally studied one) and low D_{it}. This preliminary study shows that the magnitude of fluctuation is mainly dominated by RDs, even devices are with low D_{it}. Therefore, reducing channel doping level plays a crucial role for device's fluctuation suppression in the studied 16-nm-gate CMOS devices.

4. Conclusions

In summary, we have explored the local interaction of surface potentials between the combined RDs and ITs for the 16-nm-gate CMOS devices. Due to randomly positioned charges resulting from the RDs and ITs in the 16-nm-gate CMOS devices, the "RDs and ITs" has an enlarged peak of localized spikes compared with the results of individual RDs and ITs, respectively. It implies that the interaction and coupling effects should be considered simultaneously for the RDF and ITF in emerging HKMG CMOS devices. Notably, fluctuations among RDs, ITs, and random work function of nanosized metal grains are currently under examination.

Acknowledgements

This work was supported in part by National Science Council (NSC), Taiwan under Contract Nos. NSC-99-2221-E-009-175 and NSC-100-2221-E-009-018 and by tsmc, Hsinchu, Taiwan under a 2011–2012 grant.

References

[1] Moore G. Progress in digital integrated electronics. In: Proceeding of IEEE international electron devices meeting technical digest. USA: 1975. p. 11–13.
[2] Kuhn KJ, Giles MD, Becher D, Kolar P, Kornfeld A, Kotlyar R, et al. Process technology variation. IEEE Trans Electron Dev 2011;58(8):2197–208.
[3] Li Y, Hwang C-H, Li T-Y, Han M-H. Process–variation effect, metal-gate workfunction fluctuation, and random-dopant fluctuation in emerging CMOS technologies. IEEE Trans Electron Dev 2010;57(2):437–47.

[4] Li Y, Yu S-M, Hwang J-R, Yang F-L. Discrete dopant fluctuations in 20-nm/15-nm-gate Planar CMOS. IEEE Trans Electron Dev 2008;55(6):1449–55.
[5] Li Y, Hwang C-H, Han M-H. Simulation of characteristic variation in 16-nm-gate finFET devices due to intrinsic parameter fluctuations. Nanotechnology 2010;21(9):095203.
[6] Li Y, Hwang C-H, Huang H-M. Large-scale atomistic approach to discrete-dopant-induced characteristic fluctuations in silicon nanowire transistors. Phys Status Solidi A 2008;205(6):1505–10.
[7] Li Y, Hwang C-H. Discrete-dopant-induced characteristic fluctuations in 16 nm multiple-gate silicon-on-insulator devices. J Appl Phys 2007;102:084509.
[8] Bukhori MF, Roy S, Asenov A. Simulation of statistical aspects of charge trapping and related degradation in bulk MOSFETs in the presence of random discrete dopants. IEEE Trans Electr Device 2010;57(4):795–803.
[9] Li Y, Hwang C-H. High-frequency characteristic fluctuations of nano-MOSFET circuit induced by random dopants. IEEE Trans Microw Theory Tech 2008;56(12):2726–33.
[10] Li Y, Hwang C-H, Li T-Y. Random-dopant-induced device variability in nano-CMOS and digital circuits. IEEE Trans Electron Dev 2009;56(8):1588–97.
[11] Li Y, Hwang C-H, Li T-Y. Discrete-dopant-induced timing fluctuation and suppression in nanoscale CMOS circuit. IEEE Trans Circuits Syst Part II: Express Briefs 2009;56(5):379–83.
[12] Hurley PK, Cherkaoui K, McDonnell S, Hughes G, Groenland AW. Characterisation and passivation of interface defects in (100)-Si/SiO_2/HfO_2/TiN gate stacks. Microelectron Reliab 2007;47(8):1195–201.
[13] Cassé1 M, Tachi1 K, Thiele1 S, Ernst T. Spectroscopic charge pumping in Si nanowire transistors with a high-κ/metal gate. Appl Phys Lett 2010;96:123506.
[14] Appaswamy A, Chakraborty P, Cressler J. Influence of interface traps on the temperature sensitivity of MOSFET drain-current variations. IEEE Electr Device Lett 2010;31(5):387–9.
[15] Mahbub Satter Md, Haque A. Modeling effects of interface trap states on the gate C–V characteristics of MOS devices on alternative high-mobility substrates. Solid-State Electron 2010; 54(6): 621–627.
[16] Andricciola P, Tuinhout HP, De Vries B, Wils NAH, Scholten AJ, Klaassen DBM. Impact of interface states on MOS transistor mismatch. In: Proceeding of IEEE international electron devices meeting technical digest. USA: 2009. p. 711–714.
[17] Cheng H.-W, Li F.-H, Han M.-H, Yiu C.-Y, Yu C.-H, Lee K.-F, Li Y. 3D device simulation of work-function and interface trap fluctuations on high-κ/Metal gate devices. In: Proceeding of IEEE international electron devices meeting technical digest. USA: 2010. p. 379–382.
[18] Li Y, Cheng H-W, Chiu Y-Y. Interface traps and random dopants induced characteristic fluctuations in emerging MOSFETs. Microelectron Eng 2011;88(7):1269–71.
[19] Ashraf N, Vasileska D, Wirth G, Srinivasan P. Accurate model for the threshold voltage fluctuation estimation in 45-nm channel length MOSFET devices in the presence of random traps and random dopants. IEEE Electr Device Lett 2011;32(8):1044–6.
[20] Li Y, Sze SM, Chao T-S. A Practical implementation of parallel dynamic load balancing for adaptive computing in VLSI device simulation''. Eng Comput 2002;18(2):124–37.
[21] Tang T-W, Wang X, Li Y. Discretization scheme for the density-gradient equations and effect of boundary conditions. J Comput Electron 2002;1(3):389–93.
[22] International technology roadmap for semiconductors [Online]. <http://www.itrs.net/>.
[23] Engström O. Electron states in MOS systems. ECS Trans 2011;35(4):19–38.
[24] Sze SM. Physics of semiconductor devices. 2nd ed. New York: John Wiley and Sons; 1981.