Solid-State Electronics 77 (2012) 20–25

Contents lists available at SciVerse ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

# Characterizations of polycrystalline silicon nanowire thin-film transistors enhanced by metal-induced lateral crystallization

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ARTICLE INFO

*Article history:*
Available online 14 June 2012

*Keywords:*
Metal-induced lateral crystallization (MILC)
Nanowire (NW)
Poly-Si
Solid-phase crystallization (SPC)
Thin-film transistors (TFTs)

ABSTRACT

In this paper, we present a comprehensive study on the effects of layout design and re-crystallization temperature on the material and electrical characteristics of polycrystalline silicon thin-film transistors (poly-Si TFTs) with metal-induced lateral crystallized (MILC) nanowire (NW) channels. It is found that the off-state leakage current shows strong dependence on the arrangement of MILC seeding windows, while the number of smaller solid-phase-crystallized (SPC) grains in the channel is reduced by lowering the re-crystallization temperature, thus improving the on-state behavior. Moreover, owing to the spatial confinement for MILC fronts, small cross-section of the NW channel would result in little lateral crystallization, and thus retarding the enhancement in performance of MILC NW devices.

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## 1. Introduction

Field-effect transistors (FETs) constructed with polycrystalline silicon nanowire (poly-Si NW) channels recently have attracted enormous attentions for a number of promising applications, such as high-performance thin-film transistors (TFTs) [1,2], real-time detection biosensors [3,4], and flash memory devices [5,6]. This is mainly attributed to the inherent properties of NW's small body and high surface-to-volume ratio, and thus the electrostatic states in the NW channel are sensitive to the surface conditions exerted by conventional solid gates or biochemical gates. Besides, the amount of defects contained in the tiny poly-Si NW structure is comparatively reduced, leading to lower leakage current and higher carrier mobility [7]. Moreover, the mobility of carriers in poly-Si greatly depends on both grain size and intra-grain micro-structural defects. In view of this, metal-induced lateral crystallization (MILC) technique presents a low-cost and promising approach to grow large-area poly-Si films with enhanced crystallinity at lower temperatures (below 600 °C) by using metal silicides as the crystallization agent [8–10]. It has been reported that high-performance poly-Si TFTs can be realized owing to the MILC longitudinal grains largely parallel to the drain current, hence yielding higher mobility [11,12]. Lately, we have successfully developed a novel scheme for fabricating poly-Si NW TFTs by utilizing MILC technique to achieve superior crystalline properties and electrical behaviors [2,13]. The results evidently reveal that the NW channels enhanced by MILC approach are suitable for high-performance device applications. We believe this is because the large and needle-like MILC grains can be formed in parallel to the NW channel direction, and therefore it is feasible to obtain the NW with nearly monocrystalline structure [14]. However, in the implementation of MILC process, our preliminary data seemed to suggest that the arrangement of MILC seeding windows and NW dimensions play an important role in affecting the resulted film quality and device performance [2]. So in this study, several parameters including different MILC seeding window offset (i.e., spacing between the window and the channel region, as shown in Fig. 1), dimensions of NW channels and annealing conditions, were designed and thoroughly investigated for better comprehension of MILC mechanism in the NW regime.

## 2. Device structure and experiments

The proposed MILC NW device features the source/drain (S/D) regions and NW channels across and abutting against the side-gate, respectively, as illustrated in Fig. 1. Briefly, the fabrication process started with the formation of the $n^+$-poly-Si gate on an oxidized Si substrate. Then, a 40 nm-thick tetraethyl-orthosilicate (TEOS) oxide serving as the gate oxide was deposited in a low-pressure chemical vapor deposition (LPCVD) system, followed by the deposition of a 100 nm-thick amorphous Si (a-Si) layer. Afterwards, S/D dopants were implanted with $P^+_{31}$ ion beam with a dose of $1 \times 10^{15}$ cm$^{-2}$ at 15 keV. Subsequently, S/D photoresist

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http://dx.doi.org/10.1016/j.sse.2012.05.025

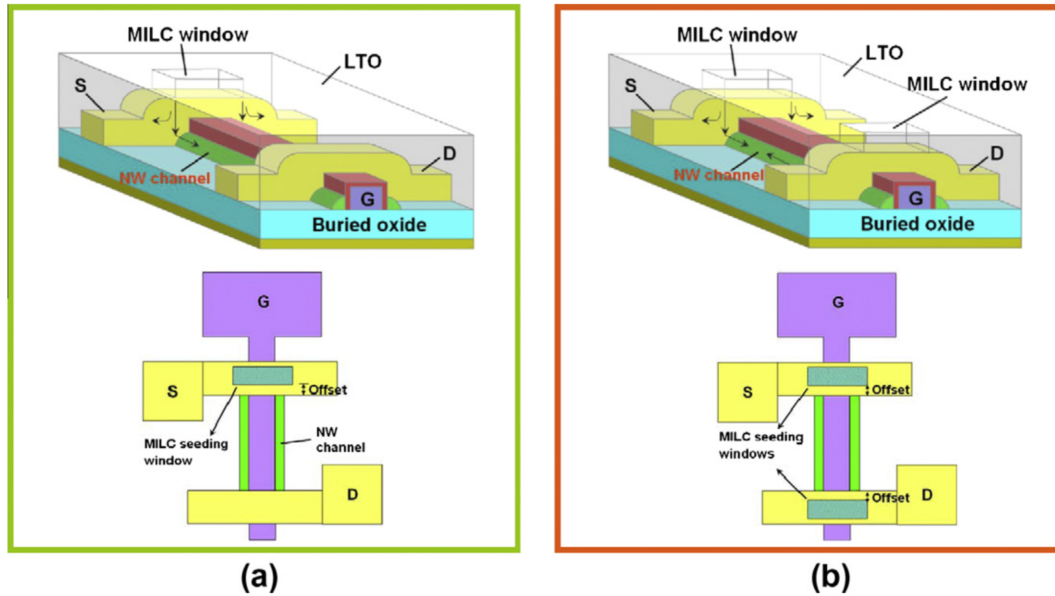


**Fig. 1.** Side and top views of the MILC devices with (a) MIUC and (b) MIBC configurations. Offset is defined as the spacing between the MILC seeding window and NW channel region.

patterns were generated using a g-line stepper and the regions were subsequently patterned by an anisotropic dry etching step using $HBr/Cl_2$ gases. During the etching process, the NW channels were simultaneously formed on the sidewalls of the gate structure, similar to the formation of sidewall spacers employed in standard CMOS manufacturing. Note that the NW channels were accomplished in a self-aligned manner with respect to the S/D and remained undoped because the aforementioned implant was done at a low energy so the implanted dopants do not reach the channel. A 100 nm-thick low-temperature oxide (LTO) was then deposited by a plasma-enhanced (PE) CVD. For MILC purpose, the seeding windows were opened in the LTO layer. In this work, two splits of samples were exploited, as illustrated in Fig. 1. In one split, denoted as the metal-induced unilateral crystallization (MIUC) split (Fig. 1a), only a single window was opened on the source region. Here the source region is defined as the terminal that serves as the grounded source during normal device characterization. In the other split, two windows symmetric to the channel center were opened on both the source and drain regions, and denoted as the metal-induced bilateral crystallization (MIBC) split (Fig. 1b). After opening the seeding windows, a 5 nm-thick Ni layer was deposited to serve as the seeding layer. The lateral crystallization was carried out at 550 °C in $N_2$ ambient for 21 h, unless mentioned otherwise. The arrows shown in Fig. 1 indicate the crystallization paths. Next, the unreacted Ni was disposed off in an $H_2SO_4/H_2O_2$ solution. Afterwards, an additional annealing step at 600 °C for 6 h was performed for the purpose of S/D dopant activation. After depositing a 200 nm passivation oxide layer and opening contact holes, a standard metallization step was performed to complete the device fabrication. It is worth noting that the overall process flow is quite simple and straightforward.

## 3. Results and discussion

### 3.1. Material properties of MILC NWs

Fig. 2 shows the top-view scanning electron microscopic (SEM) image of an MILC sample taken near the seeding window. It can be seen that the large needle-like Si grains protrude from the MILC seeding window, and the width of them reaches 90 nm. Generally,

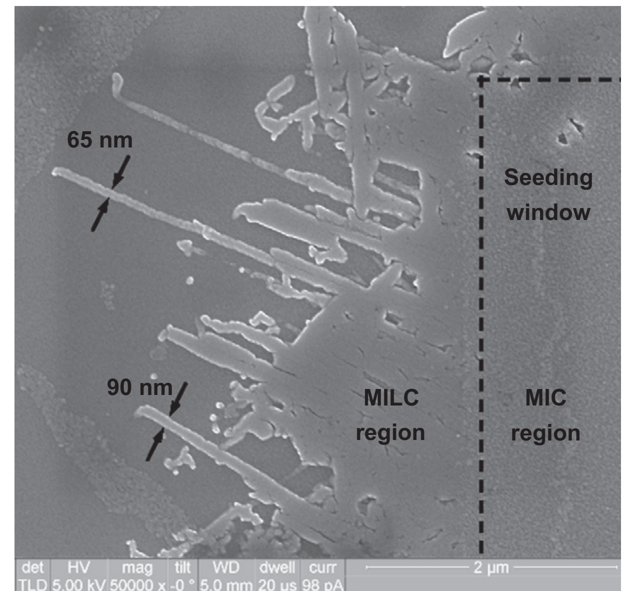


**Fig. 2.** Top-view SEM image of an MILC poly-Si sample near the seeding window. Secco etching was used to remove most of amorphous Si.

the size of NW fabricated in our study is deliberately controlled to be smaller than 50 nm in width as shown in Fig. 3. As a result, once the NW feature size is shrunk to less than the lateral size of the needle grain, it becomes feasible to achieve single-crystal NW structure. Fig. 4a shows the migration of a $NiSi_2$ precipitate with size of 50 nm by 10 nm in the NW, leaving behind the needle-like Si crystallite. In this case, single-crystalline Si property is thus obtained. For better understanding of detailed crystalline property in the NW, Fig. 4b displays the plan-view transmission electron microscopic (TEM) image of an MILC sample near the seeding window on the test structure. The NW shows long and large grains in it. Near the seeding window, the length of the single-crystal Si grain is found to be about 1 µm. The electron diffraction pattern at the circled region further verifies that this visible Si NW exhibits monocrystalline structure with $\langle 110 \rangle$ orientation. However, the

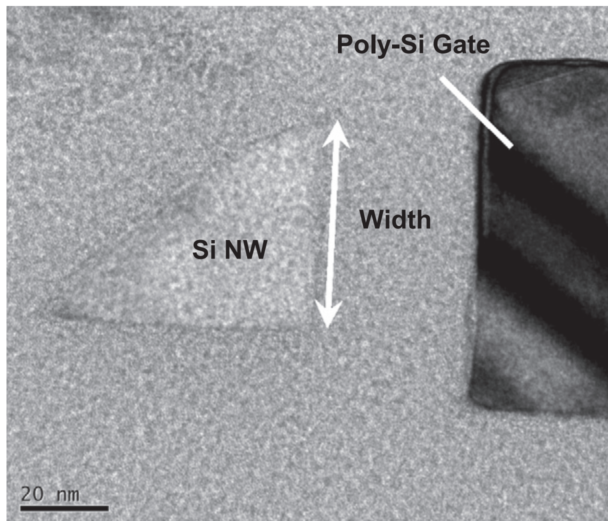


**Fig. 3.** Cross-sectional TEM image of the MILC NW device showing the NW channel abutting to the poly-Si gate.

grain size becomes smaller and the crystalline quality is worsened in the area located away from the seeding window. We ascribe this phenomenon to the fact that the grain growth due to heterogeneous nucleation of solid-phase crystallization (SPC) process is apt to compete with MILC grain growth as the annealing proceeds. SPC is a thermodynamic driven process and, typically, the crystallinity and orientation in SPC poly-Si are almost random. Hence, the grain size is small and there are a number of microdefects contained, which can be the scattering centers for carrier transport [15–17]. On the other hand, it should be also noted that much smaller grains and more defects are observed in the MIC region as shown in Fig. 2. Besides, it is reported that higher Ni concentration stays in the MIC region [18]. Hence, the device active region is usually constructed in the MILC region rather than the MIC area.

On the other hand, in the course of developing our MILC NW devices, we found that the sequence of NW formation and MILC treatment affects the device performance as depicted in Fig. 5. For MILC process executed after the NW formation, the needle-like grain growth can be deliberately confined in a designated space and direction. This implies only few $NiSi_2$ fronts could proceed in the NW structure and accordingly leave few Si grains and Ni traces in the channel. However, for MILC before the NW channel formation, lateral growth would radially spread from the seeding window. There is no NW serving as a filter to suppress the number of $NiSi_2$ fronts from proceeding, and more dendritic grains would exist in the channel region as depicted in Fig. 2, rather than merely aligning in parallel to the channel. Also, the $NiSi_2$ fronts have been found to contain higher Ni concentration [18]. Therefore, the more dendrite structures in the NW channel, the more Ni residues in it. These factors aggravate leakage behavior, and worsen on-state and subthreshold characteristics for devices with MILC performed before the NW formation, as obviously presented in Fig. 5. Hence, by taking advantage of this preliminary and important finding, the fabrication of MILC NW devices follows the procedure of NW formation prior to MILC treatment.

### 3.2. MILC seeding window arrangement

To study the effect of trace amount of Ni in the channel and keep the defective MIC/MILC intersection region away from the channel, various offset lengths were designed. The split parameters are 0.5, 1.5, 2.5, 4 and 5.5 μm. All electrical characterizations were performed under both forward (denoted as “F”) and reverse (denoted as “R”) modes of operations, based on the assignment of the source and drain biases, where the source terminal is grounded while a positive voltage is applied to the drain terminal. The off-state currents as a function of offset length for MIUC and MIBC devices under both forward and reverse modes of operations are shown in Fig. 6. It is apparent that for the MIUC device, the leakage current under reverse mode of operation is at least two orders of magnitude larger and with much larger variation, compared with those under forward mode of operation. This is mainly attributed to the defective MIC/MILC interface (as shown in Fig. 2) and residual Ni species causing additional trap-assisted leakage paths if the seeding window resides on the drain side [18]. Particularly, this

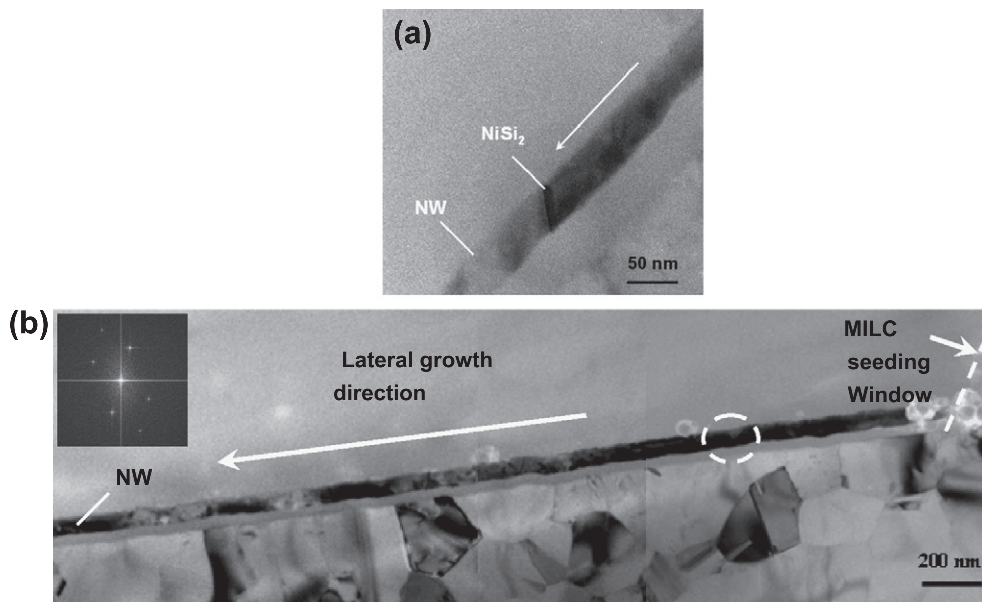


**Fig. 4.** (a) The migration of a $NiSi_2$ crystallite leaving behind the needle-like Si grain. The arrow indicates the crystallite proceeding direction. (b) Plan-view TEM picture of the MILC NW structure. The diffraction pattern in the inset was obtained from the circled region, implying monocrystalline property of the Si NW.

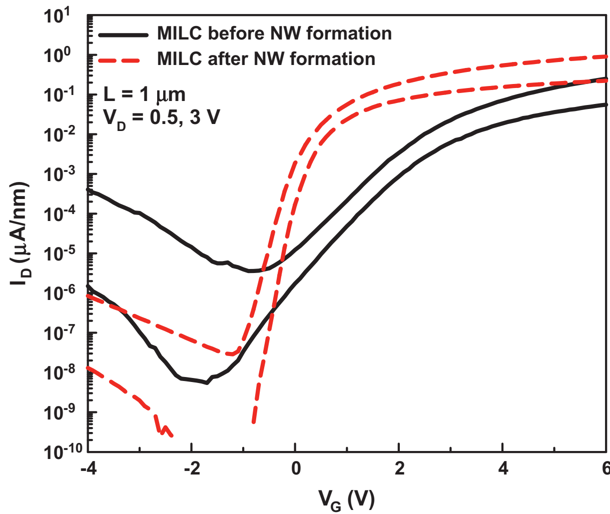


**Fig. 5.** Transfer characteristics of poly-Si NW devices for MILC process executed before and after NW formation.

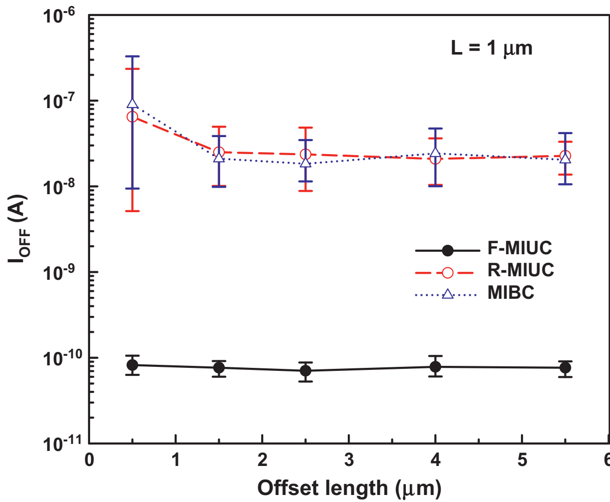


**Fig. 6.** Comparison of the off-state leakage currents, extracted at $V_D/V_G$ = 3 V/−5 V, for MIUC and MIBC devices operated under forward and reverse modes with different offset lengths.

phenomenon becomes more serious as the offset is smaller than 1 μm. However, the leakage current is almost independent of the offset length in the F-MIUC scheme, which can be explained by the fact that the drain terminal is possibly free from the highly defective trap states. It also reveals that the leakage current of the F-MIUC scheme could be decreased by about three orders of magnitude over that of the R-MIUC case when the offset is 0.5 μm. Moreover, almost comparable trend and variation as well as magnitude of the leakage currents are revealed in the splits of R-MIUC and MIBC, implying that the severe leakage current is greatly dependent on the amount of defect densities existing at the drain terminal, rather than the source side. These findings are important to obtain optimal MILC NW device structure.

### 3.3. Length effects on MILC NWs

In Fig. 4, the region near the seeding window exhibits good crystallinity, but deteriorated crystalline quality is found in the area located away from the seeding window. The location dependence in material quality reflects on the device characteristics. Fig. 7a compares the transfer characteristics between the MIUC and MIBC devices with $L$ = 1 μm. It is seen that the performance is better for the MIUC device. In the MIBC device, the fronts of crystallization from opposite sides confront with each other at the central region of the channel. Trace amount of Ni species may be left inside the channel and leads to the degraded on-state performance as compared with the MIUC device. However, the trend is reversed in the case of devices with $L$ = 5 μm, as shown in Fig. 7b. When the channel is long, small-grain structures of SPC mechanism will most probably take place during the later stage of the MILC annealing in the region near the drain. Thus, the on-state current of the MIUC device would be worse than that of the MIBC one, which could be attributed to the fact that needle-like grains growing from opposite sides of the channel comparatively retrain SPC process in the MIBC configuration. Therefore, in order to suppress SPC grains in the MILC channels especially in long NWs, the MIBC scheme turns out to be a better choice of device structure.

Furthermore, for the sake of addressing the length issue, two main strategies could be adopted. One is to increase the MILC rate; the other is to suppress the SPC growth. Based on our experiment (data not shown) and the literature [19], MILC rate is faster in p-type poly-Si films. In this regard, if NW channels are doped with p-type dopants, MILC rate will increase. However, dopant distribution in NWs and threshold voltage adjustment of the device will remain an issue. The other approach is by lowering the annealing temperature, thus suppressing the SPC process. It is known that the activation energy is about 3.2 eV for SPC, while 1.85 eV for MILC [20]. Fig. 8 displays the on-current behaviors as a function of the channel length for devices annealed at 525 °C and 550 °C, respectively. The on-currents for the 525 °C-annealed devices are indeed found to be larger than those for the 550 °C-annealed counterparts. Fig. 9 shows the schematic illustrations for the crystalline properties of MILC NW channels at lower and higher annealing temperatures, inferring that fewer small-size SPC grains are present to retard MILC grain growth at lower annealing temperature, and thus enhancing the crystallinity of NW channels as well as the on-currents.

### 3.4. Width effects on MILC NWs

In this part, we will further discuss the impact of NW's cross-section on device performance. Fig. 10 shows the transfer characteristics of 22 nm-wide MILC and SPC NWs as compared with those of 50 nm-wide MILC and SPC NWs devices. For fair comparisons, all currents are expressed as current density by dividing the current by the cross-sectional conduction width of NW. The SPC samples characterized here were fabricated with the MILC devices on the same wafers but without any MILC seeding window on them. So during the MILC treatment, the channel re-crystallization of these SPC devices is only related to the thermal annealing. Apparently, the 50 nm-wide MILC NW device shows distinct MILC effect and superior performance in the subthreshold and on-state regions. However, MILC effect is found to be nearly on a par with SPC for the narrow-channel (i.e., 22 nm) devices, implying similar crystallinity in the NW channels which mostly comprise of SPC grains. This phenomenon is also observed in the previous research [14]: NWs with width smaller than 30 nm would result in little lateral crystallization. Such NW width effect should be due to the spatial confinement for $NiSi_2$ precipitate to proceed in the small NW channel. In addition, the competing heterogeneous SPC growth is also believed to be more pronounced in a smaller space. Therefore, MILC process in an aggressively scaled NW volume becomes much more complicated to analyze. Such effect certainly needs a plethora of samples and careful TEM analysis for full investigation.

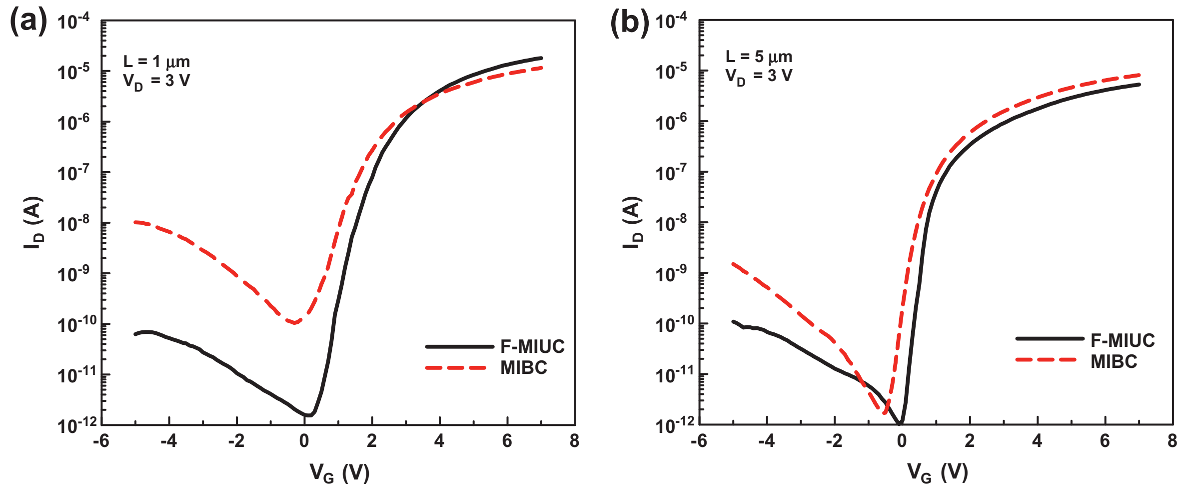


**Fig. 7.** Comparison of the transfer characteristics for the F-MIUC and MIBC NW devices with channel length of (a) 1 μm and (b) 5 μm.

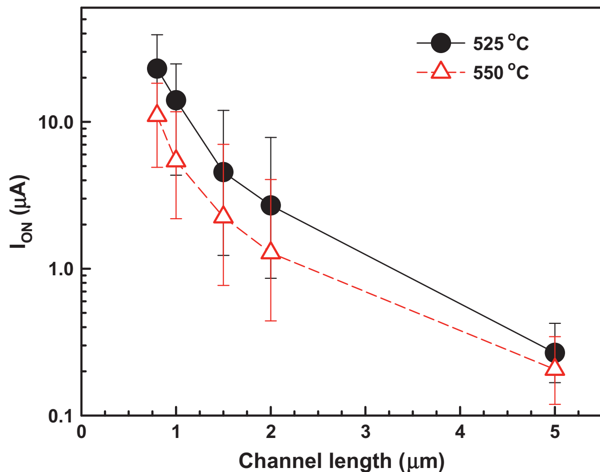


**Fig. 8.** On-currents, extracted at $V_D/V_G = 3\ V/10\ V$, as a function of the channel length for MILC devices anneal at 525 °C and 550 °C, respectively. The devices are with offset of 2.5 μm and operated under F-MIUC scheme.

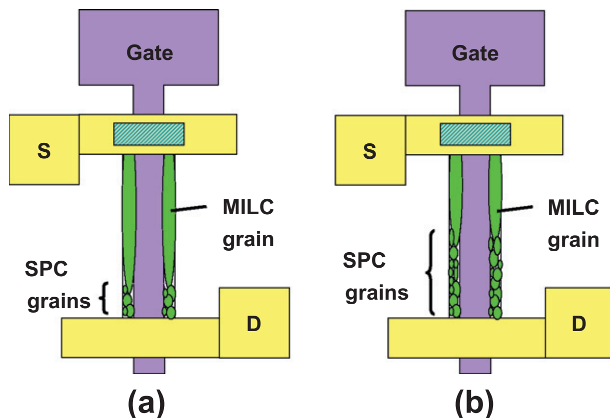


**Fig. 9.** Schematic illustration of the crystallinity of NW channels performed at (a) low and (b) high annealing temperatures during MILC process.

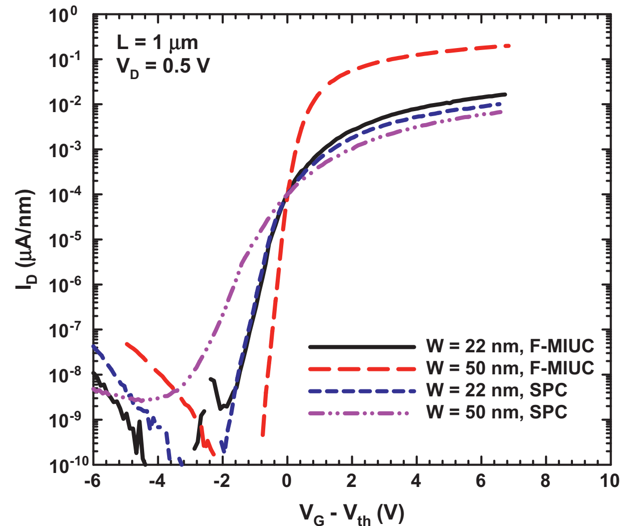


**Fig. 10.** Transfer characteristics of NW devices with various NW widths and crystallization approaches.

## 4. Conclusion

In this work, we have addressed the influences of seeding window arrangement and annealing temperatures on the performance of the MILC NW devices. Our results indicate that as the seeding window is located only on the source side and away from the drain/channel junction, the off-state currents could be greatly reduced. Moreover, the SPC growth in the NW structure can be suppressed by using a lower MILC temperature, resulting in enhanced on-state characteristics. In addition, the dimensions of NW channels also impact on MILC behaviors and device electrical properties. We believe these findings provide useful guidelines for process and circuit designers in the design and fabrication of high-performance poly-Si NW FETs.

## Acknowledgments

The authors would like to thank National Nano Device Laboratories (NDL) and Nano Facility Center (NFC) of National Chiao Tung University for assistance in device fabrication. This work was supported in part by the Ministry of Education in Taiwan under ATU

Program, and the National Science Council of the Republic of China under Contract No. 99-2221-E-009-167-MY3.

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