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High-performance vertically stacked bottom-gate and top-gate polycrystalline silicon thin-film transistors for three-dimensional integrated circuits

I-Che Lee *, Tsung-Che Tsai, Chun-Chien Tsai, Po-Yu Yang, Chao-Lung Wang, Huang-Chung Cheng

Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, ROC

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ABSTRACT

The three-dimensional CMOS inverter with top-gate (TG) poly-Si thin film transistors (TFTs) vertically stacked on the bottom-gate (BG) poly-Si TFTs have been proposed to achieve high-performance characteristics via excimer laser crystallization (ELC) for the first time. Under an appropriate laser irradiation energy density, the silicon grain growth could be controlled from the sidewalls of the bottom-gate structure and thus the high-quality laterally grown poly-Si film with single perpendicular grain boundary in the channel would be formed for the BG TFTs. In addition, a simple ELC method was also utilized to the top-layered poly-Si film for TG TFTs as compared with solid-state-crystallized (SPC) ones. As a result, the field-effect mobilities of the proposed n-type BG and p-type TG TFTs could be significantly increased to be 390 and 131 cm^2/V s, respectively, in contrast to 32.3 and 14.7 cm^2/V s for the SPC ones, accordingly. Furthermore, such three-dimensional (3-D) TFT have also been employed to demonstrate the inverter devices and is suitable for future 3-D ICs as well as system-on-panel applications.

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1. Introduction

In the past years, shrinkage of the device dimension was one of the technologies to increase transistor density and improve circuit performance on integrated circuits [1,2]. However, the device dimension might not be shrunk infinitely. Therefore, the scaling-down technologies to increase the transistor density might approach the scaling limitation [3,4]. Moreover, with decreasing the feature size, the importance of interconnect delay increases [5].

Owing to the scaling limit and the increasing domination of the interconnects, a further increase of device density and reduction of delay would depend on the three-dimensional integration technology [6–8]. Vertically stacked multifloor structure has been considered as one of the ultimate three-dimensional integrated circuits (3-D ICs) in future [9]. From the viewpoint of reduction of interconnect delay, the connection of the function blocks could be replaced by the shorter and vertical interconnects for 2-layer devices. Therefore, the interconnect delay of 3-D ICs would be reduced as compared with 2-D ICs [6]. In the perspective of reduction of chip area, it has reported that a 50% area reduction could be attained by employing two stacked device layers over the standard 2-D IC structure [10]. Furthermore, the process could be simplified by means of fabricating only one type of device instead of complementary ones on each layer [11].

One of the main challenges to implement 3-D stacked transistors was the thermal budget. The high temperature processing of second layer of devices and beyond might be a threat to cause dopant diffusion in the lower layers of devices [12]. Another obstacles of developing 3-D stacked device layer technology was to obtain high quality silicon layer for the multi-level purpose [13], for example, solid-phase crystallization [14], selective epitaxial growth and epitaxial lateral growth of silicon [15], crystallization of amorphous silicon using Ge [16], metal induced lateral crystallization [12], etc. Some of these methods might cause poor film quality and metal contamination as well as suffer from complicated process and high thermal budget [17,18].

One promising approach for achieving high-quality silicon grains with low thermal budget was to utilize ELC [19]. Under the laser annealing conditions near the super lateral growth (SLG) regime, the large grains can be obtained for high-performance poly-Si TFTs. In addition, various poly-Si grain enhancement technologies with ELC have been proposed to further improve the uniformity and performance of poly-Si TFTs, including the a-Si spacer [20], recessed-channel structure [21], and so on [22–29]. However, some of them might need complex process or requiring complicated laser annealing systems.

A simple structure of bottom-gate (BG) TFTs vertically stacked with top-gate (TG) TFTs possessing low thermal budget and easy fabrication procedure was proposed to attain high-performance 3-D ICs via ELC. Consequently, the bottom-layered BG poly-Si TFTs with single perpendicular grain boundary in the channel would demonstrate high-performance electrical characteristics.

* Corresponding author. Tel.: +886 3 5712121x54218; fax: +886 3 5738343.
E-mail address: iclee.ee95g@nctu.edu.tw (I.C. Lee).

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Furthermore, the complementary 3-D poly-Si invertors with p-type top-gate (TG) TFTs stacked on the n-type bottom-gate (BG) ones were also demonstrated with good characteristics for the system-on-panel and 3-D integrated CMOS applications.

2. Device fabrication

Fig. 1 displays the key fabrication steps for the proposed 3-D CMOS inverter with BG and TG poly-Si TFTs crystallized via ELC. At first, an 100-nm-thick phosphorus-doped polysilicon layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C on oxidized silicon wafers. After definition the bottom-layer bottom gate electrode, an 100-nm-thick tetraethyl orthosilicate (TEOS) gate oxide layer and an 100-nm-thick a-Si layer were deposited by LPCVD. Then, the samples were performed by a KrF excimer laser irradiation (λ = 248 nm) at room temperature and the number of laser shots per area was 20 (i.e., 95% overlapping). After ELC, the poly-Si active layers were etched to define the bottom-layered active channel region. Next, a phosphorus ion implantation with a dose of 5×10^{15} cm^{-2} was carried out to form the n-type bottom-layered source and drain regions. After the deposition of a TEOS separation oxide, an 100-nm-thick a-Si layer were deposited by LPCVD and irradiated by the KrF excimer laser. Next, the poly-Si active layers were etched to define the top-layered active channel region. After that, an 100-nm-thick TEOS gate oxide layer and an 100-nm-thick in situ doped phosphorus poly-Si layer were deposited. The poly-Si gate and gate oxide were etched to form top-layered top-gate region. Then, a boron ion implantation with a dose of 5×10^{15} cm^{-2} was carried out to form the p-type top-layered source and drain regions. Afterwards, a TEOS passivation oxide layer was deposited, and the dopant activation was performed by thermal annealing at 600 °C for 10 h. Finally, contact hole opening, metallization, and sintering process were carried out to complete the fabrication of the 3-D BG and TG TFTs. For the comparison, the conventional SPC TG poly-Si TFTs were also fabricated.

3. Results and discussion

The plane-view scanning electron microscopy (SEM) photographs, as shown in Figs. 2 and 3, verify the grain boundaries in the channels for the bottom-layered and top-layered devices. For the bottom-layered ELC BG poly-Si thin film, Fig. 2a and b show the SEM images of the films without and with optimum laser irradiation energy density after Secco etching, respectively. It was observed that the silicon grains uniformly existed in the channel region and only one perpendicular grain boundary was formed in the center of the channel under optimum laser irradiation energy density of 460 mJ/cm^2, as illustrated in Fig. 2b. However, Fig. 2a displays the poly-Si thin film having many small grains without optimum laser irradiation energy density of 420 mJ/cm^2. When the excimer laser irradiation is irradiated on the a-Si thin film, the optimum laser energy density is controlled to completely melt the thin channel region of a-Si film and partially melt the thick region of a-Si near the sidewalls of the bottom gate. A lot of un-melting solid seeds remain near the sidewalls of bottom-gate electrode. Consequently, a lateral temperature gradient can be produced between the thin channel and thick sidewalls of a-Si thin film, and the grains will grow laterally from the sidewalls to towards the channel region. Therefore, the lateral growth can be artificially

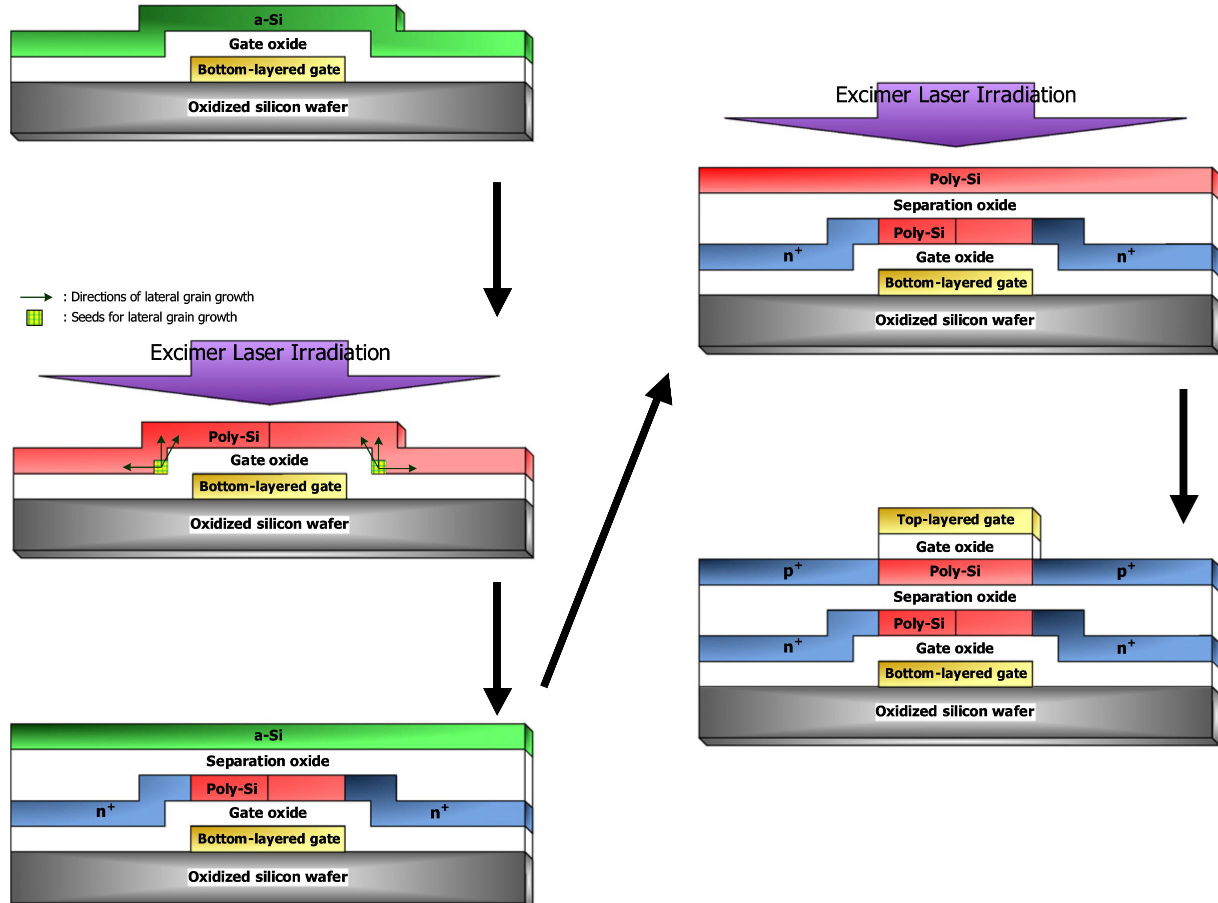

Fig. 1. Schematic diagrams of the key-process procedures of the proposed 3-D bottom-gate (BG) and top-gate (TG) poly-Si TFTs crystallized with ELC.

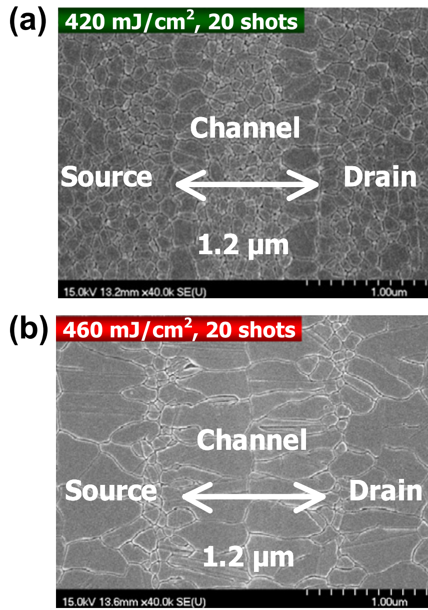

Fig. 2. The plane-view scanning electron microscopy (SEM) photographs of bottom-layer poly-Si thin film (a) without and (b) with optimum laser irradiation energy density after Secco etching.

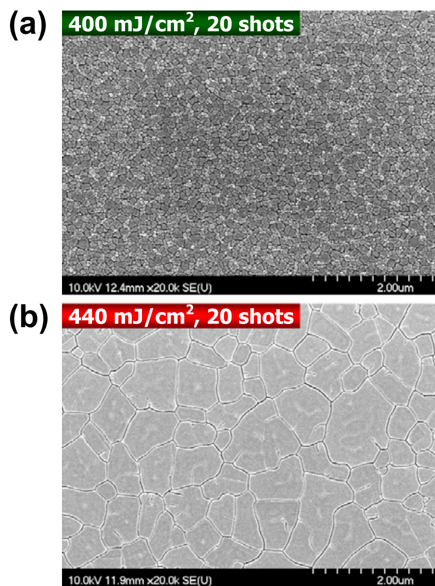

Fig. 3. The plane-view scanning electron microscopy (SEM) photographs of top-layer poly-Si thin film (a) without and (b) with optimum laser irradiation energy density after Secco etching.

controlled in the channel region of the bottom-layered ELC BG TFTs and only one grain boundary perpendicular to the direction of current flow is uniformly formed in the center of the channel region. Moreover, the optimum laser irradiation energy density process window for the bottom-layered poly-Si thin film could be easier widened from 460 mJ/cm^2 to 540 mJ/cm^2.

The plane-view SEM photographs of top-layer poly-Si thin film without and with optimum laser irradiation energy density after Secco etching were displayed in Fig. 3a and b, accordingly. Under the laser irradiation energy density of 400 mJ/cm^2, the small grains and a large amount of grain boundaries were observed in the poly-Si thin film, as shown in Fig. 3a. On the contrary, the large poly-Si grains existed in the poly-Si thin film with the optimum laser irradiation energy density of 440 mJ/cm^2, as presented in Fig. 3b. When the applied excimer laser energy density on the a-Si thin film is too small to cause complete melting the a-Si thin film in the channel region, vertical solidification occurs and the un-melted solid layer remains to be a-Si. Thus, the melted Si layer transform into poly-Si with small grain size. On the other, when the energy density of excimer laser irradiation on the a-Si thin film is controlled to near complete melting the a-Si thin film, very few residues exist as seeds. Therefore, the large grain size poly-Si thin film was formed in the channel due to the so-called super lateral growth phenomenon.

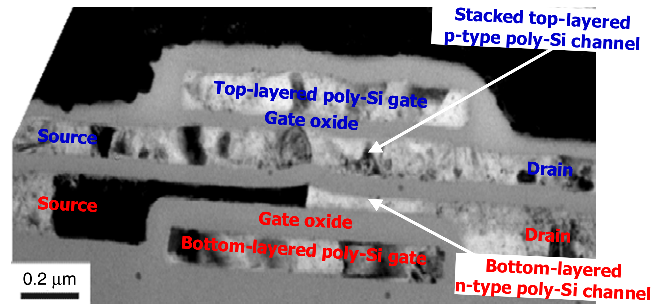

Fig. 4. The focus-ion-beam prepared cross-sectional TEM image of excimer-laser-crystallized 3-D BG and TG TFT with a gate length of 1.2 µm.

Fig. 4 demonstrated the cross-sectional transmission electron microscopy photograph to analyze the microstructure of excimer-laser-crystallized 3-D CMOS TFTs with a gate length of

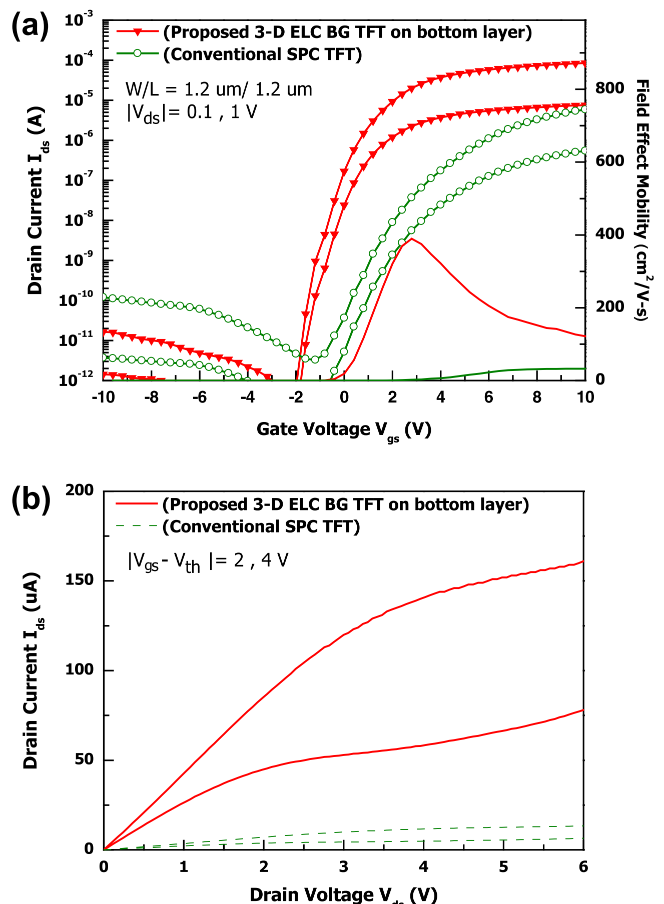

Fig. 5. The typical (a) transfer characteristics and (b) output characteristics of the proposed 3-D ELC BG TFT on bottom layer and conventional SPC TFT.

Table 1
Measured electrical characteristics of 3-D ELC BG TFTs on bottom layer and conventional SPC ones.

TFT structures ($L = W = 1.2$ μm)	Field-effect mobility μ_{FE} (cm^2/V s)	Subthreshold swing S.S. (V/dec)	Threshold voltage V_{th} (V)	On/off current ratio
Conventional SPC TFT	32.3	1.148	3.23	1.84×10^6
Proposed 3-D ELC BG TFT on bottom layer	390	0.512	−0.23	1.76×10^8

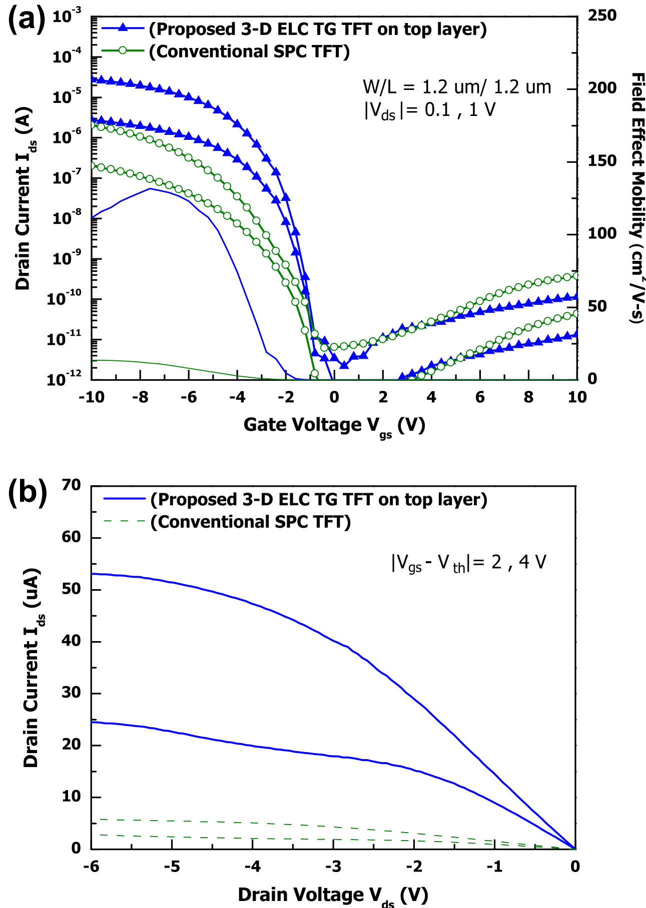

Fig. 6. The typical (a) transfer characteristics and (b) output characteristics of the proposed 3-D ELC TG TFT on top layer and conventional SPC TFT.

1.2 μm. It is clearly shown the gate-stacked structure of the TFTs with the p-type top-layered ELC TG TFTs stacked on the n-type bottom-layered ELC BG ones. The poly-Si grains were observed in the top-layer p-type channel. Moreover, two spatially controlled silicon grains with a longitudinal size of about 0.60 μm were formed in the bottom n-channel owing to the BG structure. This phenomenon is attributed to that the 100-nm-thick poly-Si thin film with the thicker sidewall intrinsically caused by the BG structure was complete melted and the thin film located near the sidewalls was partial melted under appropriate laser irradiation conditions. Then the poly-Si thin film would start solidification from the BG sidewalls and extend toward the complete melted silicon film in the channel until the solid–melt interface impinged from the opposite directions. In addition, it was worthy to notice that the bottom channel maintained the single grain boundary perpendicular to the current flow after laser irradiation of the top-layered devices. Therefore, most of the laser irradiation energy of top-layered devices was absorbed in the top-layered silicon film and the optimized laser energy would not damage the underlayer.

Because of the high-quality bottom-layered poly-Si film, the n-type ELC BG TFTs demonstrated superior electrical performance, as shown in Fig. 5a and b for the transfer and output characteristics, correspondingly. It was observed that the higher field-effect mobility of 390 cm^2/V s for the proposed 3-D ELC BG TFT on the bottom layer was attained as compared with the lower one of 32.3 cm^2/V s for the conventional SPC TFT. The proposed 3-D ELC BG TFT also showed a steeper subthreshold swing and high on/off current ratio of 0.512 V/dec and 1.76×10^8 as compared with the conventional SPC one having those of 1.148 V/dec and 1.84×10^6, respectively. Table 1 presents some important electrical parameters. Those great improvements were attributed to the high-quality large and uniform poly-Si grains as well as the only one perpendicular grain boundary artificially controlled growth in the channel region owing to the bottom-gate structure under optimum laser energy condition.

The TG poly-Si TFT on top layer shows good electrical characteristics as compared with the conventional one. Fig. 6a and b exhibit the typical transfer and output characteristics, respectively. As can be seen, an obvious improvement in device characteristics is obtained from the SPC TFT to the proposed 3-D ELC TG one, such as the field-effect-mobility increasing from 14.7 to 131 cm^2/V s and the subthreshold swing decreasing from 1.337 to 0.531 V/dec. Some important electrical parameters were listed in Table 2. It is also demonstrated that the proposed 3-D ELC TG TFTs exhibit higher driving capability due to the high-quality silicon grains in the channel. Take the $|V_{gs} - V_{th}| = 4$ V as an example, the current drivability of proposed 3-D ELC TG TFT is about ten times as large as that of an SPC TFT under the same bias condition. It was contributed to the high-quality poly-Si thin film under optimum laser irradiation energy density for the proposed scheme. In summary, the better electrical characteristics and driving capability imply that the proposed 3-D ELC BG and TG TFT structure is more suitable for high-resolution AMLCDs, AMOLEDs, and 3-D IC applications.

To demonstrate the feasibility in 3-D IC applications, the inverter property, voltage transfer characteristics, of the proposed CMOS with vertically stacked BG and TG poly-Si TFTs was exhibited in Fig. 7. The 3-D configuration was the p-type TG TFTs stacked on the n-type BG TFTs with the common gate structure. The power supply was $V_{DD} = 1$, 2, or 3 V, and the input signal swings from −2 to 2 V as well as the output voltage were from 1 to 3 V near the V_{DD}. In addition, the high noise margin NM_H was 1.79 V and the low noise margin NM_L was 0.11 V for $V_{DD} = 3$ V. The definitions of the noise margin were: $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$. Where V_{IH} and V_{IL} are defined as the points at which the slope of

Table 2
Measured electrical characteristics of 3-D ELC TG TFTs on top layer and conventional SPC ones.

TFT structures ($L = W = 1.2$ μm)	Field-effect mobility μ_{FE} (cm^2/V s)	Subthreshold swing S.S. (V/dec)	Threshold voltage V_{th} (V)	On/off current ratio
Conventional SPC TFT	14.7	1.337	−4.25	1.11×10^6
Proposed 3-D ELC TG TFT on top layer	131	0.531	−2.04	2.32×10^7

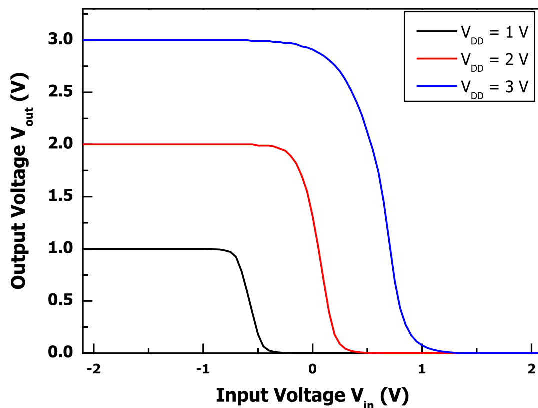

Fig. 7. Transfer characteristics of 3-D TFT inverter with p-type TG TFTs on the top layer and the n-type BG TFTs on the bottom layer. The power supply is V_{DD} = 1, 2, or 3 V.

the transfer characteristics is −1. The output voltages are V_{OH} and V_{OL}. Indeed, the proposed 3-D BG and TG poly-Si TFTs showed good inverter properties.

4. Conclusions

A novel high-performance 3-D CMOS inverter, which is composed of one BG poly-Si TFT with single one perpendicular grain boundary in the channel and one stacked TG poly-Si TFT, has been fabricated by ELC. The proposed top-layered p-type TG and bottom-layered n-type BG poly-Si TFTs exhibit high field-effect mobilities of 131 and 390 cm^2/V s, respectively, as compared with the conventional p-type and n-type SPC TFTs having the mobilities of 14.7 and 32.3 cm^2/V s, correspondingly. It is attributed to the only one grain boundary perpendicular to the channel for the bottom layer and the high-quality poly-Si film for the top layer. Moreover, the inverter with the stacked p-type TFTs on the n-type ones was demonstrated with good characteristics. Therefore, the vertically stacked BG and TG poly-Si TFTs are compatible with current CMOS process procedures as well as suitable for the future 3-D ICs and system-on-panel applications.

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