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A novel thermal switch and variable capacitance implement by CMOS MEMS process approaching in micro electrostatic converter

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ABSTRACT

This paper focuses on implementing a novel thermal switch and variable capacitance design by using commercially available CMOS MEMS process which can approach in a micro electrostatic converter system. In this system, there are two major parts. First is the variable capacitance, and the second is the thermal switch. In the variable capacitance, it implement by UMC 0.18 μm one-poly seven-metal (1P7M) CMOS MEMS process. In the post process, the silicon-oxidation has been released and the gap between two metal layers filled with PDMS (Polydimethylsiloxane). Filling with PDMS is to significantly increase C_{max}.

In the thermal switch design, there are two novel designs in this switch: first, the soft contact structure and post-processing fabrication; second, using residual stress to achieve large structural deformation and a new design of thermal switch. To create the soft contact structure, residual stress effect has been utilized to make different bending curvatures. According to the experiments, the layer metal 1 has the largest residual stress [1] effect that can achieve the largest deflection in *z*-axis. Because the residual stress of the layer metal 1 is negative, the structure will bend down after release, the largest contact area which has been set up to get the lowest contact miss ability. In the post-processing fabrication, 0.3 μm thickness gold will be patterned on the contact tips. Due to gold, rather than Aluminum, has no oxidation issue, it has more reliability on preventing the problem of oxidation than Aluminum. In the new thermal actuator design, we design a novel folded-flexure [2,3] with the electro-thermal excitation to turn the switch on or off. In the prototype, the device size is 500 μm × 400 μm and the gap between two contact pads is 9 μm in off-state.

Depending on the experimental results, the C_{max} is 19.22 nF, and the C_{min} is 10.65 nF in variable capacitance. The switch can work stably at 3 V, and the working temperature and operating bandwidth are individually 20–200 °C. The natural frequency of the switch is 42.9 kHz and the response time is 14.28 Hz.

1. Introduction & system

Micro-Electro-Mechanical System (MEMS) is the integration of mechanical elements, sensors, actuators, and electronics on a common substrate through micromachining processes compatible with conventional integrated circuit (IC) fabrication. By combining silicon based micro-machines with microelectronics, MEMS technology has revolutionary impact on all categories of applications, making possible the realization of the complete system on chip (SOC) concept. Current MEMS research and development has already been applied in fields such as micro-optical systems, sensors and actuators, micro fluidic elements, and even biomedical applications, all with fruitful results. Such continuous improvement of microsystem technology promotes the development of smart micro transducer networks, such as RFID (Radio Frequency Identification) and wireless sensor network. These highly integrated portable devices have received increasing interest in recent years. Nevertheless, power consumption has become a severe limitation on the development due to the limited energy capacity of the small volume energy storage devices. Traditional storage devices include batteries, micro batteries, micro fuel cells, ultra capacitors, micro heat engines, and radioactive materials. Researchers attempt to increase the energy density in these storage devices, but the solutions still have finite lifetime and high maintenance costs. Fortunately, the advance in low power VLSI (Very Large Scale Integrated circuit) technology, along with the low duty cycles of the wireless sensor networks, have reduced power requirements to tens to hundreds of micro watts. It becomes possible to power these portable devices by scavenging ambient energy from the environment, thus providing a self renewable or even self

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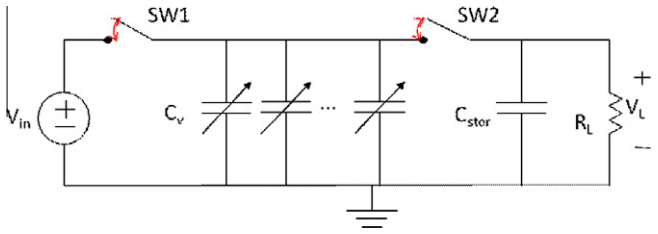

Fig. 1. Micro electrostatic energy converter system.

sustainable energy source which can replenish part or all of the consumed power. This concept has received attention along with the development of wireless sensor networks, and research on various ambient energy scavenging technologies are being conducted.

Electrostatic capacitive energy conversion utilizes a variable capacitor to convert vibration energy into electric energy. The electrical energy W stored in a capacitor with capacitance C and voltage V is $W = \frac{1}{2}CV^2 = \frac{1}{2}\frac{Q^2}{C}$. If the capacitance of a pre-charged capacitor with constant charge Q is decreased due to vibration, the stored electrical energy in the capacitor will increase, thus converting the kinetic energy into electrical energy. The main concern of the capacitive energy conversion is how to extract the stored electrical energy in a properly controlled timing scheme. Capacitive energy conversion is more suitable for the steady frequency moderate amplitude vibration source mentioned before.

Fig. 1 is the micro electrostatic energy converter system. The converter is composed of an auxiliary battery supply V_{in}, a vibration driven variable capacitor C_v and an output storage capacitor C_{stor}, which is connected to the load R_L. Two switches, SW1 and SW2, are used to connect these components and control the charge–discharge conversion timing. The variable capacitor serves as the conversion transducer and the auxiliary battery supply is used to pre-charge the capacitor. A basic operation cycle begins

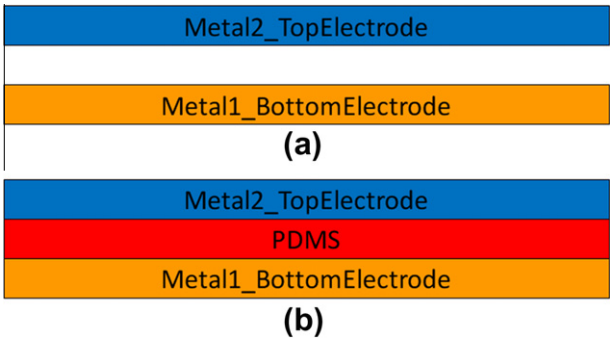

Fig. 3. (a) Remove SiO_2 by HF vapor. (b) The gap filled with PDMS.

Table 1
Eight combinations of CMOS metal/oxide stacked structures.

No.	Metal 1	Metal 2	Metal 3	Metal 4
1	●	●	●	●
2		●	●	●
3	●		●	●
4	●	●		●
5			●	●
6		●		●
7	●			●
8				●

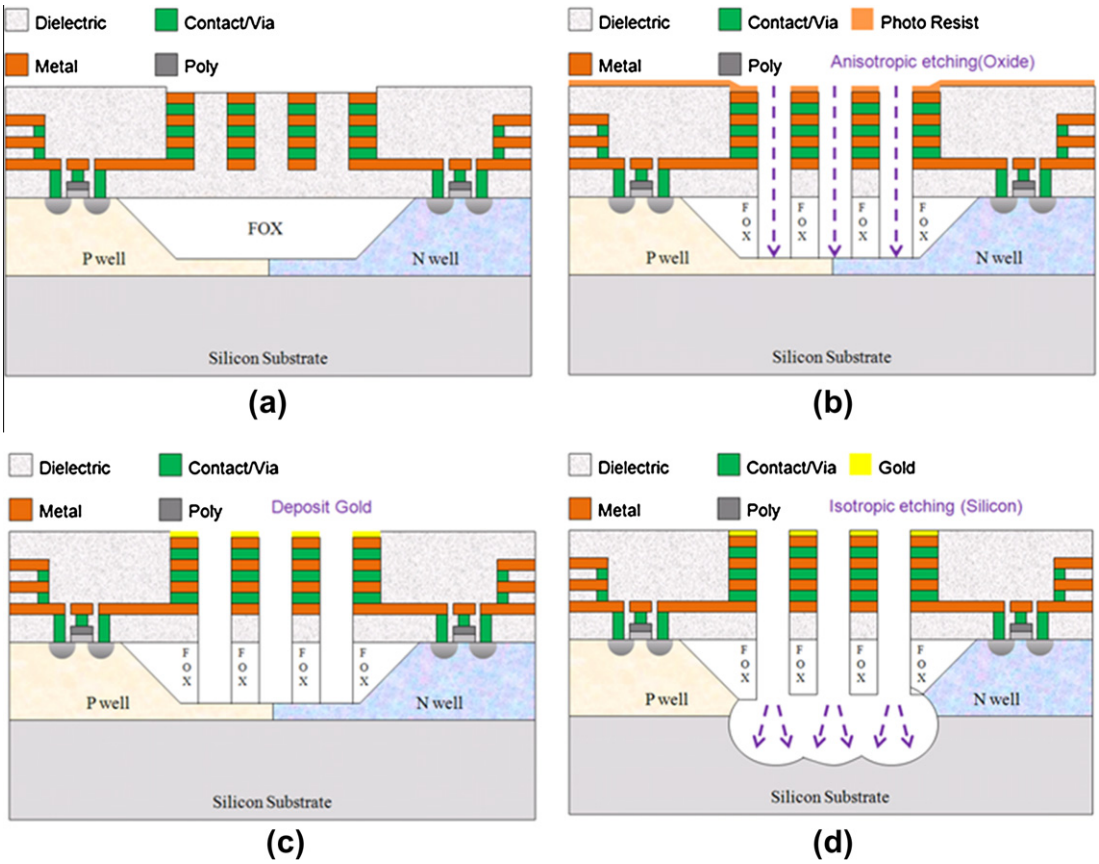

Fig. 2. CMOS MEMS process.

Table 2
Average values and standard deviations (STD) of effective residual stress property.

No.	Stress gradient (MPa/μm)	STD
1	4.35	3.83
2	21.92	7.48
3	2.90	3.84
4	−3.05	3.03
5	20.48	7.83
6	12.45	6.00
7	−5.42	3.90
8	10.39	4.85

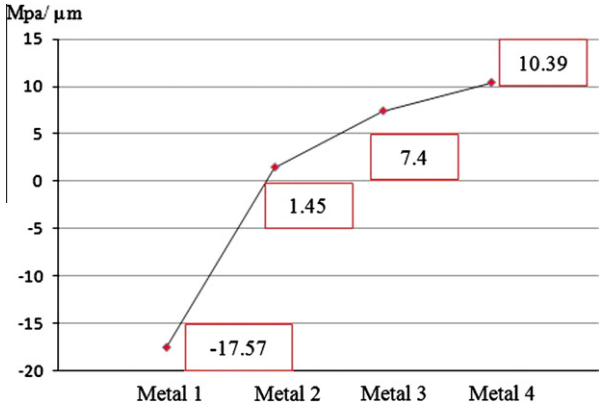

Fig. 4. Effective gradient stress vs. metal layer.

when the variable capacitor C_v is charged by the auxiliary voltage supply V_{in} through SW1 at its maximum C_{max}. After C_v is charged to V_{in}, SW1 is opened and the capacitance changes from C_{max} to C_{min} due to vibration driven displacement. In this process, the charge Q on the capacitor remains constant (SW1 and SW2 both open). Therefore, the terminal voltage on the capacitor is increased, converting the kinetic energy of vibration into electrical energy stored in C_v. When the capacitance reaches C_{min} and terminal voltage reaches V_{max}, SW2 closes and allows C_{stor} to be charged by C_v through charge redistribution, transfer the energy to the output port. SW2 is then opened and C_v varies back to C_{max}, preparing for the next conversion cycle.

2. Fabrication

CMOS MEMS utilizes the CMOS stacked layers to form the micro-sensors and the micro-actuators. It has great potential for commercial production. However, stacked CMOS layers are composed of compound materials like metal, via, poly-silicon, and oxide layers. There is stress in and between these layers. The extraction for individual layer in CMOS spends large chip area. And the simulation time for microstructure with the complicated multi-layers is much longer by using this method. The efficient method is to extract the effective mechanical properties of some basic metal/oxide combination structures. It not only costs less testing area and simulation time but also includes the stress of interlays. This paper used the effective mechanical properties extracted from eight combinations of CMOS metal/oxide stacked structures to simulate and predict the static and dynamic behavior of MEMS device. The problem of the lateral contact switch has been solved in this study by depositing gold on the Aluminum layer.

The CMOS MEMS multi-project wafer (MPW) was fabricated by TSMC 0.35 μm two-poly four-metal (2P4M) CMOS process and CIC micromachining post process. The major materials of metallization and dielectric layer in this CMOS process are respectively aluminum and silicon oxide. Fig. 2 shows the cross-section views of the MPW with post-CMOS micromachining steps. By the way, in this study we use Bio CMOS MEMS process, a gold layer is deposited on top layer.

For alleviating the dry etching process on dielectric layers, as Fig. 2a shows, the CMOS passivation layers on etching selective regions are removed during the CMOS process. Before the anisotropic dry etching, an additional photo-resist layer is spun and lithographed on the wafer for the post process. This lithography enables the definition of the protective region of photo-resist layer over the metal of the inductor. The thickness of the photo-resist requests at least 5 μm to avoid the RIE etching directly on the top meal. The anisotropic RIE etching with CF4, CHF3 and O2 is subsequently used to remove the exposed dielectric oxide in Fig. 2b. In this step, most photo-resist layers would exhaust with the RIE gas. When all metal layers are done, a gold layer is deposited on the top layer, as shown in Fig. 5. As Fig. 2d indicates, the following isotropic dry etching with SF6 and O2 is then included to remove the underlying silicon substrate and release the microstructures.

3. Device design

3.1. Variable capacitance design

In the variable capacitance design, a out-plane gap-closing comb structure is used for the variable capacitor. It is implemented by UMC 0.18 μm 1P7M CMOS process. In the post process, the silicon dioxide layer removed by HF vapor, thus there are seven metal layers can be used in variable capacitor. It means that there are up

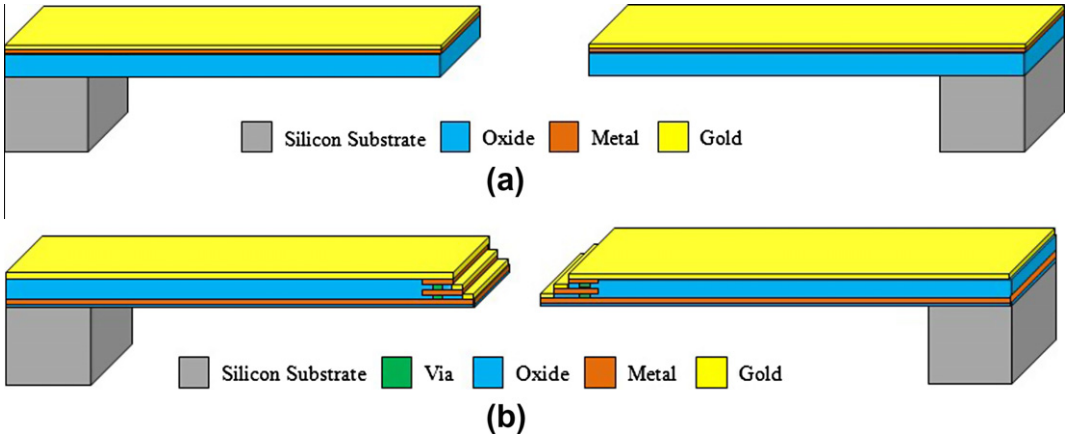

Fig. 5. (a) Cross-section view of normal contact tip. (b) Cross-section view of proposed contact tip.

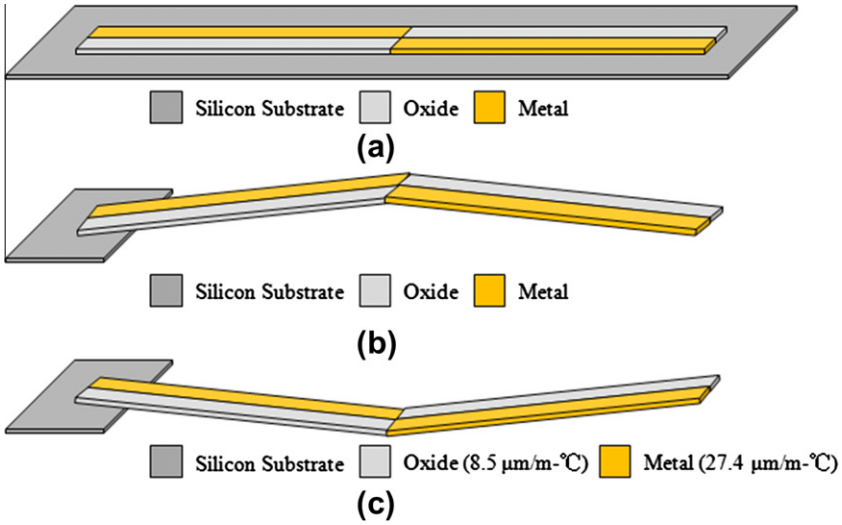

Fig. 6. (a) is the top view of micro-cantilever beam before release. (b) is the structure after release at 293 K (20 °C). (c) Due to different thermal coefficient, the structure will pull back with temperature increase to 473 K (200 °C).

Table 3
Average values and standard deviations (STD) of effective gradient stress property.

No.	Stress gradient (MPa/μm)	STD
1	64.27	4.43
2	27.79	4.74
3	40.45	7.33
4	38.88	4.79
5	13.23	1.26
6	7.97	2.67
7	20.35	1.45
8	-20.96	3.07

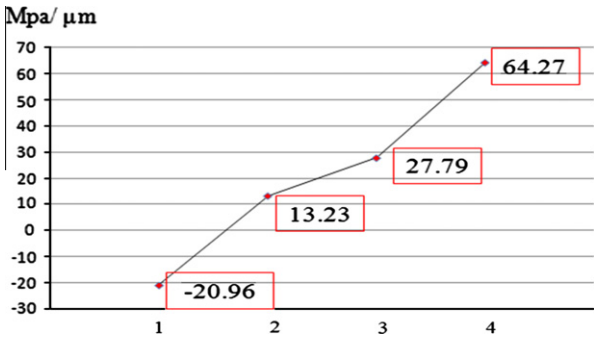

Fig. 7. Effective residual stress vs. numbers of metal layer.

to 6 available variable capacitors in one block. In order to increase the capacitance value, the gap of the metal layer is filled with PDMS (polydimethylsiloxane), as shown in Fig 3. The relative permittivity of PDMS is 10. For fill the PDMS into the gap of the variable capacitance, about 0.05 ml PDSM had drop at the etch-hole. Stand for 1 h the PDSM will fill the gap of the capacitance.

3.2. Mechanical switch design

The switches SW1 and SW2 are realized as lateral contact mechanical switches. Conventional design of the charge–discharge timing control switches utilize diodes or clocked active switches. In order to prevent charge leakage out of C_v and C_{stor}, the switches must have a reverse leakage current lower than a few nA. This is not common in commercially available diodes and other switching circuitry. Capacitive coupling is another problem, in which the capacitance of the switch contributes to parasitic capacitance. Our design of SW1 and SW2 has barely zero charge leakage and very low capacitance coupling effect. Other advantages are the low energy consumption, the synchronous operation to the variable capacitor, and the monolithic integration with the whole device structure.

SW1 is designed to contact simultaneously when or merely after the metal layer has touched. SW2 is designed by a thermal type. SW2 is turn on at initial time, and there are current through pass the switch. The temperature of the switch will increase caused by the current. And it will pull-back, thus the SW2 will turn off. To design the thermal switch, there are two parts should discuss. First is the soft contact structure, and second is new design of thermal actuator.

3.3. The soft contact structure

In a normal switch design, the contact area is too small to make a poor contact. To solve this problem, a new design of the contact profile which used negative residual stress effect and the different configurations of the contact tip has proposed in this study. Every metal used in the TSMC 0.35 μm 2P4M CMOS process has its own effective residual stress. Combine different metal layer also can get different residual stress [1]. Table 1 shows eight combinations of CMOS metal/oxide stacked structures.

By comparing Table 2, only the layer Metal 1 has the negative and residual stress (Table 2 and Fig. 4). Thus the contact profile will bend down after release. With this profile, it provides lager contact area than the normal design.

This study also designs different configurations of the tip with different contact profile which can get more contact area (Fig. 5a and b).

In the post-processing, 0.3 μm thickness gold will be deposited on the surface of the element. Since gold is non-active, it has more reliability on avoiding the problem of oxidation and on increasing the conductivity at contact area.

3.4. A novel design of thermal switch

In the novel thermal switch design, this paper proposed a novel folded-flexure with the electro-thermal excitation to control the

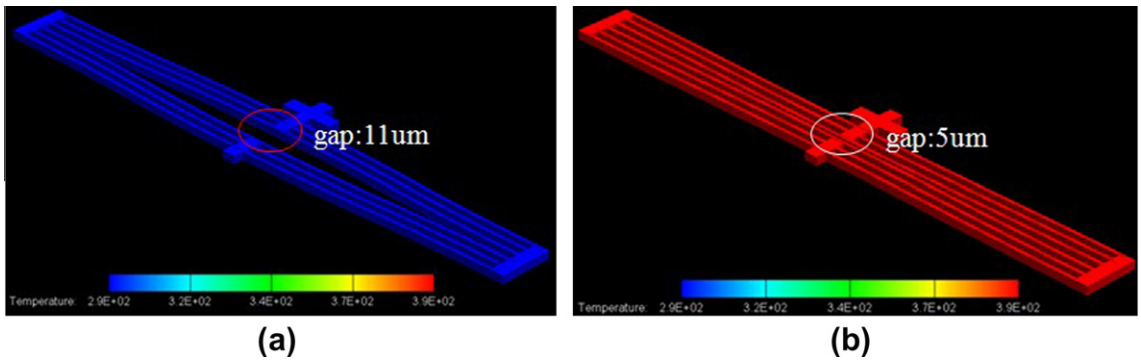

Fig. 8. (a) Thermal switch at 20 °C in Coventor-Ware. (b) Thermal switch at 200 °C in Coventor-Ware.

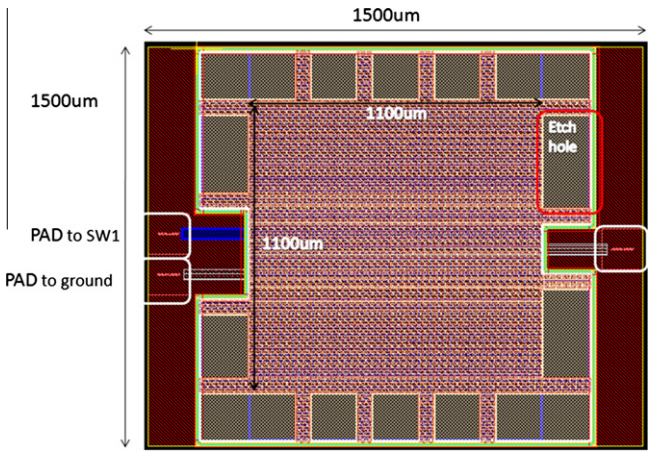

Fig. 9. Layout of the variable capacitor.

switch on or off, as shown in Fig. 6. In the normal design [2,3], the numbers of the layers used are metal 1, metal 2 and metal 3. In this proposed design, the different numbers of layers are used.

In this design, effective gradient stress and thermal coefficient are used finite-element-method software in simulation. By comparing Table 3, the stress increases with the numbers of metal layers, as shown in Fig. 7. It indicated that oxide layer in CMOS process has compressive stress and the metal layer has tensile stress before post-processing release, as illustrated in Fig. 6a. Due to the isotropic dry silicon etch and structural release. The oxide layer has tensile stress and the metal layer has compressive stress after release, as shown in Fig. 6b.

When the switch turn on, there are current pass by the switch and let the temperature of the switch rise up. Because oxide layer (8.5 μm/K) and metal layer (27.4 μm/K) [4] have different thermal coefficient. The folded-flexure of the switch will pull back and the switch will turn off, as shown in Fig. 6c. So we can use this folded-flexure structure to control the switch turn on or turn off.

4. Simulation and experimental result

The simulation software (Coventor-Ware) also used to verify the switch and capacitance design. By the simulation result, the initial gap is 11 μm at 293 K (20 °C). Due to temperature increase, the gap pulling back and the displacement of the contact-tip is 6 μm at 473 K (200 °C), as shown in Fig. 8.

Fig. 9 is the layout of the variable capacitance, and it has implemented by UMC 0.18 μm CMOS MEMS process, as shown in Fig. 10a and b the SiO_2 layers of the capacitance have been etched by HF and filled with the PDMS. The size of the capacitor is 1100 μm × 1100 μm. Fig. 11 is the thermal switch implement by TSMC 0.35 μm 2P4M CMOS process and CIC micromachining post process. The width of the device is 500 μm, and length is 400 μm.

The switch and variable capacitor were first tested by a probe station to see if they were properly released. The switch was measured by the MEMS Motion Analyzer (MMA G2, Umech Technologies, USA) system at the National Chip Implementation Center (CIC). The MMA system utilizes image processing technique and measures the periodic relative motion between the movable and the still structures of the device. The photograph of the MMA measurement setup provided by CIC is shown in Fig. 12. The MMA measurement results are plotted in Fig. 13a. The resonant frequency is about 42.9 kHz with a corresponding −90° phase shift

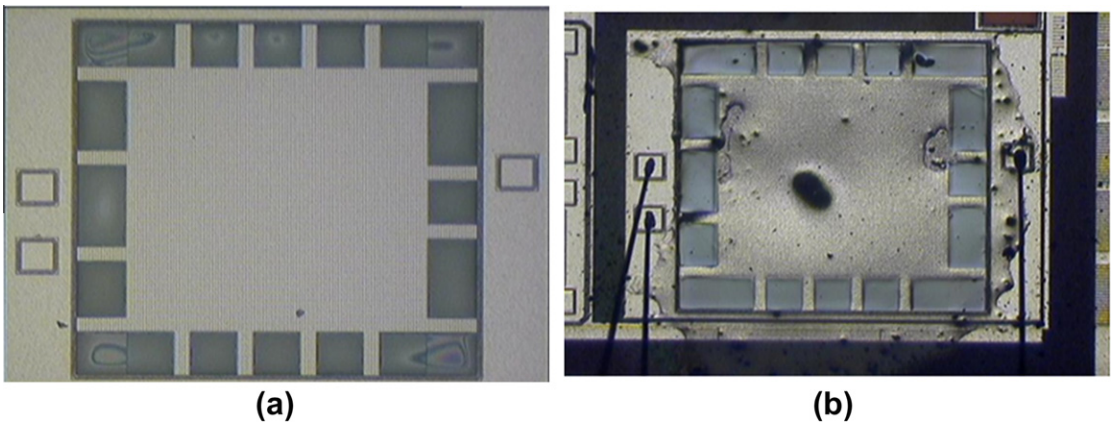

Fig. 10. (a) Device implemented by UMC 0.18 μm process and remove the SiO_2 layer. (b) The gap filled with PDMS.

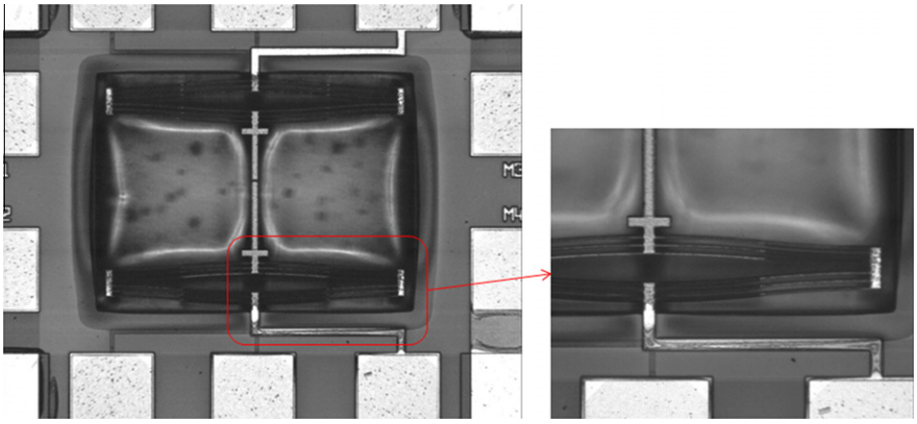

Fig. 11. Device implemented by TSMC 0.35 μm process.

Fig. 12. MEMS Motion Analyzer (MMA).

at resonance. From the measured amplitude response curve, it is seen that the 3 dB bandwidth is about $\Delta f_{3dB} = 250$ Hz in Fig. 13b. The response time of the switch is 14.28 Hz, as shown in Fig. 14. The system is used into bio-medical environment. The operation frequency is about 1–2 Hz, so the response time of the switch is suitable for the system.

In the static state of the switch, we use probes to control the voltage given and signal analysis. Fig. 15a is the photo by Optical Microscope (OM) and Fig. 15b is the measurement result by optical profiler. The gap is 19.86 μm at initial time (0 V and 300 K). Fig. 16a is the switch in 20 °C, and Fig. 16b is the switch in 200 °C by using MMA.

5. Conclusion

In this study, a MEMS-based variable capacitor and a new thermal switch was proposed and implemented by using CMOS MEMS process and CIC micromachining post process has been developed. In the prototype, the device size of the variable capacitor is 1100 μm × 1100 μm, and the thermal switch size is 500 μm × 400 μm. The gap between two contact pads of the switch is 9 μm in off-state. According to the measurement result and the photo by OM, the switch can work stably at 3 V, and the working temperature and operating bandwidth are individually 20–200 °C. The natural frequency of the switch is 42.9 kHz and the response time is 14.28 Hz.

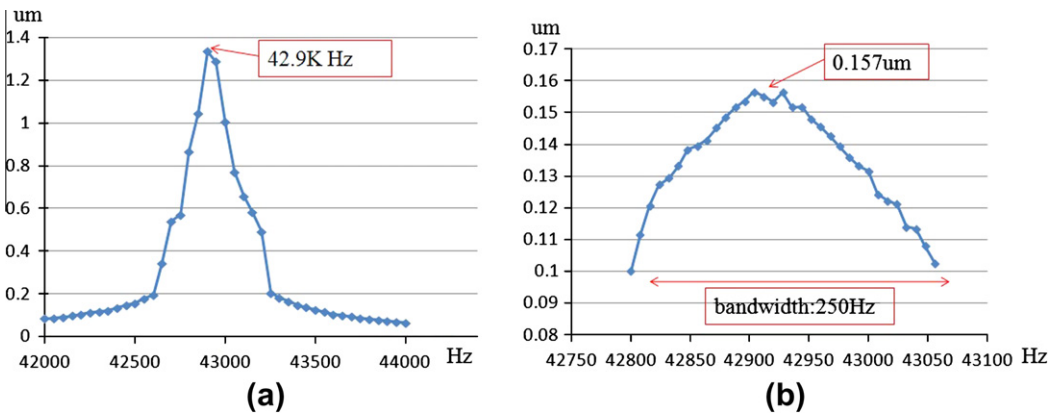

Fig. 13. (a) Natural frequency. (b) Bandwidth of the switch.

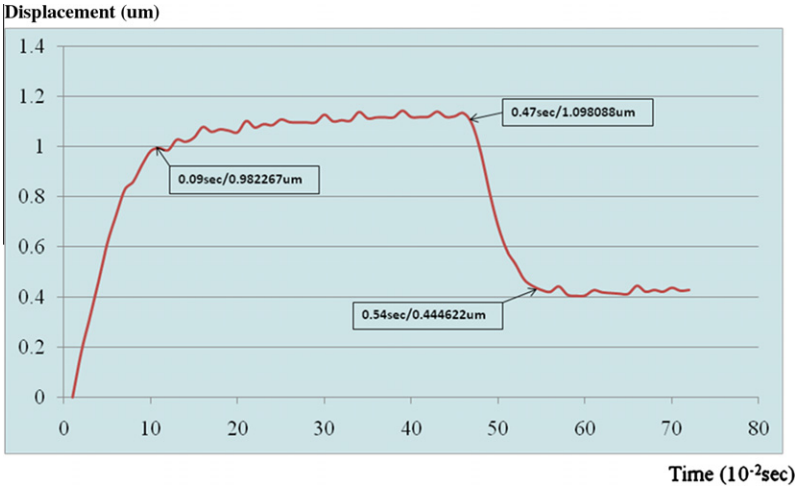

Fig. 14. Response time of the switch.

Fig. 15. (a) One side of the switch. (b) Measurement result by optical profiler.

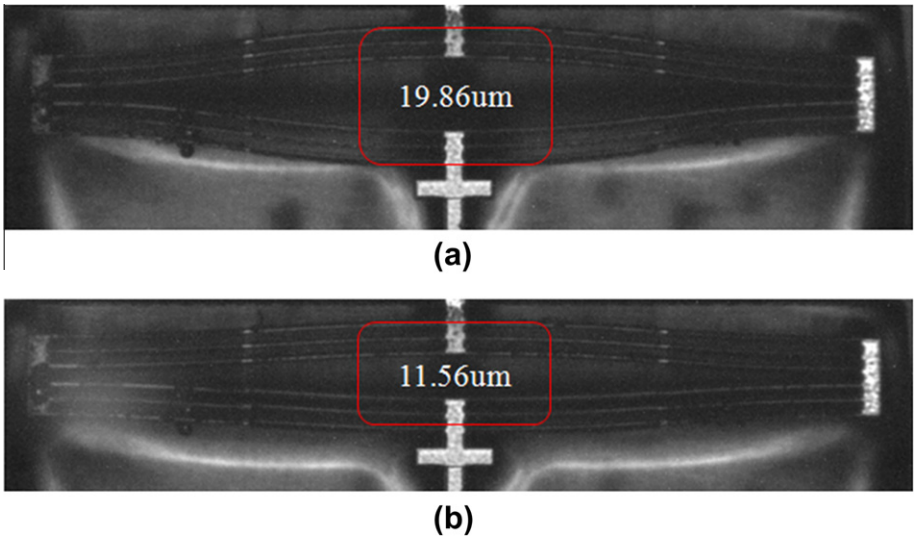

Fig. 16. (a) Thermal switch at 20 °C. (b) Thermal switch at 200 °C.

Acknowledgments

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