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Experimental Results of Testing a BIST Σ–Δ ADC on the HOY Wireless Test Platform

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Abstract High pin count packaging and 3D IC technology make testing such advanced ICs more and more difficult and expensive. The HOY wireless test platform provides an alternative and cost-effective test solution to address the poor accessibility and high test cost issues. The key idea is implementing a low-cost and short-distance wireless transceiver on chip so that all test instructions and data can be transmitted without physical access. Due to the limited wireless bandwidth, all modules in the device under test (DUT) are preferred to have some built-in self-test (BIST) features. Prior works successfully demonstrated that DUTs with memory and digital circuits can be tested on the low-cost wireless test platform. However, there is no example to show if it is also possible to test the DUT embedded with analog circuits on the HOY test platform. This paper demonstrates the first system-level integration including hardware and software for testing a fully-integrated BIST ADC on the HOY wireless test platform. The DUT chip fabricated in 0.18-μm CMOS consists of a second-order Σ–Δ ADC under test (AUT) and the BIST circuitry. The AUT design employs the decorrelating design-for-digital-testability (D^3T) scheme to make itself digitally testable. The BIST design is based on the modified controlled sine wave fitting (CSWF) method. The required BIST circuits are purely digital and as small as 9.9k gates. The gate count of the HOY test wrapper is less than 1k. Experimental results obtained by the HOY wireless test platform show that the AUT achieves a dynamic range of 85.1 dB and a peak SNDR of 78.6 dB. The wireless test results show good agreement with those acquired by conventional analog tests.

Keywords Analog-to-digital converter (ADC) · Built-in self-test (BIST) · Design-for-testability (DfT) · Sigma–Delta modulation · Analog and mixed-signal test · Wireless test

1 Introduction

Testing advanced system-on-chip (SoC) IC becomes more and more difficult and costly because of the increasing pin count and transistor count of the IC. For example, conventional wafer tests request high density (with more than 1000 pins) probe cards with a very fine pitch (smaller than 50 μm). Such probe cards suffer from implementation difficulty, high cost, and low reliability. Testing a device with a small pin count like a three-dimension (3D) IC is even harder. The 3D IC assembles several chips together by through-silicon-vias. The intermediate bare dies therefore may have very few accessible pins which make their tests extremely difficult after packaging. In addition to the accessibility issue, the requirement of bulky and expensive automatic test equipment (ATE) due to more complex

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chip functions is another root cause of the increasing test cost.

Wu et al. [30] defined a next-generation wireless test system named HOY. The HOY wireless test platform provides an alternative to cope with the difficulty and the high cost of testing advanced SoC devices [12, 30]. The key idea is implementing a low-cost and short-distance wireless transceiver [17] on chip so that all test instructions and data can be transmitted wirelessly. Adopting wireless communication eliminates the need of physical contacts of the tester and the device under test (DUT) and thus directly addresses the accessibility issues. The platform also allows using a low-cost laptop as the test host to replace the expensive ATE without loss of the capability of programming the test procedure and automatically conducting the tests. An FPGA prototype of the HOY wireless test platform has been proposed for the purpose of demonstration in [18].

An intrinsic limitation of the HOY platform is the finite wireless communication bandwidth. To tackle this problem, the circuits under test (CUTs) are preferred to have some design-for-testability (DfT) or built-in self-test (BIST) features. For memory and digital circuits, lots of DfT and BIST methods have been proposed [1, 2, 4, 16, 21, 29]. Chi et al. [5] successfully demonstrated an example DUT which integrated memory and digital circuits with BIST circuits and the HOY RF communication module that can be tested on the HOY wireless test platform. On the other hand, the development of the BIST and DfT methods for analog and mixed-signal (AMS) circuits are less mature [3]. Several state-of-the-art BIST techniques for data converters can be found in [6, 13, 22, 24–26].

Analog-to-digital converters (ADCs) are fundamental AMS building blocks of modern SoC devices whose tests are very challenging even in the traditional way, not to mention conducting their tests wirelessly. The requirements of transmitting high-precision analog stimuli to the DUT and acquiring a huge amount of output samples for analyzing the responses by fast Fourier transform (FFT) are the major difficulties of testing ADCs on the HOY wireless test platform. To address these issues, the ADC design should incorporate with some BIST scheme so as to minimize the data volume exchanging between the tester and the DUT and to provide the DUT with high-precision analog stimuli.

This work demonstrates the experimental results of a new fully-integrated BIST Σ–Δ ADC in 0.18um tested on the HOY wireless test platform. We show the system integration of not only the hardware, but also the software to make testing Σ–Δ ADC wirelessly and cost-effectively possible. The new modulator core of the ADC under test (AUT) adopted the D^3T input structure proposed in [10] to enhance the test accuracy.

The BIST design is based on the modified controlled sine wave fitting (CSWF) method [11, 20] which conducts single-tone functional tests without the need of CPU/DSP and bulky memory. The BIST design can test for the signal-to-noise-and-distortion ratio (SNDR), the dynamic range (DR), the offset, and the gain error of the AUT. The required BIST circuits are purely digital and we implemented the cost-effective CSWF output response analyzer (ORA) proposed in [15] to make the total gate count of the BIST circuitry less than 10 k. Comparing with the BIST techniques requiring critical analog circuits, the proposed BIST design benefits from less yield loss caused by parametric defects since digital circuits are more robust against the parametric defects than analog circuits are. In addition, the yield loss due to hard defects in a circuit is proportional to its area. Because the gate count of the added BIST circuitry is less than 10 k, the yield loss resulted from the hard defects of the BIST circuitry would be not significant. The experimental results shows good agreement between the wireless test results and those reported by conventional functional tests.

The paper is organized as what follows. Section 2 reviews the HOY wireless test platform. Section 3 describes the design of the DUT, the fully integrated BIST Σ–Δ ADC, and explains how the BIST design operates. Section 4 demonstrates the system-level integration of the BIST ADC and the HOY wireless test platform and the experimental results. Finally, we draw our conclusions in Section 5.

2 Review of the HOY Wireless Test Platform

The HOY wireless test platform aims at providing a simplified test interface and test flow to address the high cost and the difficulty of testing advanced SOC devices [30]. Wireless communication directly solves the test problem of too many or too few physical pin/pad count and simplifies the test interface. However, it also leads to a limited communication bandwidth. To bear up the finite data bandwidth, the CUTs being wirelessly tested favor embedding some kinds of DfT and/or BIST techniques.

Figure 1 shows the general architecture of the HOY wireless test platform proposed in [12, 30]. The HOY wireless test platform is composed of the tester, constituted by the test host and the wireless test head, and the DUT. The test host is as simple as a laptop and thus saves the costly ATE. The test instructions and

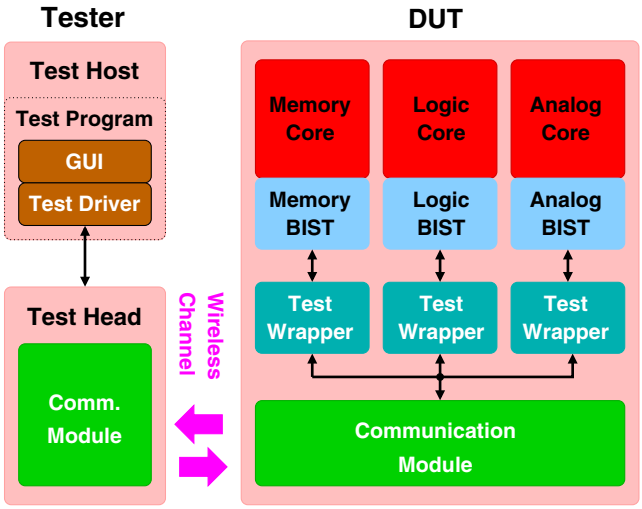

Fig. 1 The HOY wireless test platform

the test results are wirelessly communicated between the tester and the DUT to address the pin accessibility issue. The HOY platform defines the wireless communication as a short-distance (around 1 cm) one so that the on-chip wireless communication module can be made very simple and leaves all the design burdens to that of the wireless test head of the tester [17].

Generally speaking, the DUT is an SoC chip containing different kinds of CUTs such as memory, logic, and analog circuits. All the CUTs on chip share the same communication module to achieve a small hardware overhead. The communication module itself can be made as a hardware intellectual property (IP) so that it can be plug-and-play in any IC design. The design details of the communication module including the short-range RF transceivers, the baseband processor, the media access control (MAC), and the data exchange unit (DEU) can be found in [17, 18].

On the contrary, each CUT has a customized test wrapper to synchronize different clock domains and to exchange the test data between the CUT and the communication module. It also interprets the test instructions for the CUT [31].

The HOY wireless test platform not only defines the hardware interfaces but also provides software supports. For example, an automatic test driver generator has been developed to automatically generate the test drivers for the test host and the test wrappers for the CUTs [31]. With the test driver generator, circuit designers no longer have to worry about how to integrate their circuits on the wireless test platform.

In addition to the test driver generator, the platform also provides a test program that integrates the test drivers with a graphic user interface (GUI). It allows users to setup their desired test procedures easily. The tester automatically issues the test instructions, sends test data to the DUT, and then receives the test data from the DUT according to the preset test procedure. The test results can be immediately shown on the GUI of the test program. By integrating the hardware with the software, the HOY test platform facilitates convenient SoC tests like conventional ATE does.

Another major advantage of adopting the HOY wireless test platform is making the tests cost-effective because it does not need high-end ATE but a linux-based laptop. An economical model has been built to prove that the test cost can be drastically reduced if the HOY wireless test platform is applied instead of conventional ATE, especially in advanced technology [12].

In this work, we adopted the automatic test wrapper and test driver generator proposed in [31] to generate the hardware test wrapper and the software test driver of the DUT. We also integrated the generated test driver into the HOY test program so that the whole test procedure was fully automatic.

3 Implementation of the DUT

The core of the DUT is an high-resolution Σ–Δ ADC composed of an analog second-order switched-capacitor (SC) Σ–Δ modulator and a digital decimation filter. The Σ–Δ ADC operates at an oversampling ratio (OSR) of 128 and an oversampling frequency of 6.144 MHz for audio applications. The decimation filter removes the out-of-band shaped noise, equalizes the passband responses, and decimates the output sampling rate to 48 kHz.

To support the wireless tests, additional BIST circuits were added to the DUT. Ideally, a successful BIST ADC design should be able to test for the standard performance parameters that conventional functional tests provide, and to achieve high test accuracy and a small silicon overhead. Besides, the added BIST circuitry itself should achieve a high yield which may be an issue when the BIST circuitry consists of critical analog circuits [28]. Functional-test-alike BIST schemes [11, 23, 27] conform to most of the requirements and thus are preferred for this application.

Figure 2 shows the block diagram of the DUT. The two shaded blocks indicate the original Σ–Δ AUT. The rest blocks are the purely digital circuits for conducting the BISTs. In the following, we will depict the details of the implementation.

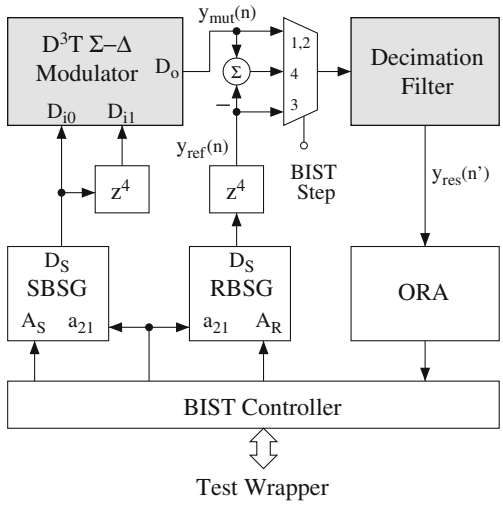

Fig. 2 Block diagram of the proposed fully integrated BIST Σ–Δ ADC

3.1 Σ–Δ ADC Under Test

Transmitting high-precision analog stimuli through a wireless channel is much difficult than transmitting digital ones; therefore, our first approach to make the DUT built-in self-testable is making the Σ–Δ modulator digitally testable. Several appealing design-for-digital-testability (DfDT) schemes for Σ–Δ ADCs have been proposed for this purpose [7, 8, 10, 23]. They have the similar idea: using one or more 1-bit digital-to-charge converters (DCCs) embedded in the AUT to generate the analog stimuli on-chip. The required stimulus is first modulated by a software 1-bit Σ–Δ modulator. The resulted Σ–Δ modulated bit-stream is then applied to the embedded 1-bit DCC to generate the discrete-time analog stimulus. The single-bit DCC achieves a very small silicon area and is inherently linear. Both features are substantial for the success of the BIST design. Among these schemes, the decorrelating design-for-digital-testability (D^{3}T) scheme proposed in [10] is superior to the others in test accuracy. Thus, we adopted it in our SC Σ–Δ modulator design.

Figure 3 illustrates the schematic of the D^{3}T second-order Σ–Δ modulator [10]. It's output $D_o \in \{0, 1\}$ is a pulse-density-modulated (PDM) bit-stream, and Φ_1 and Φ_2 are two non-overlapped clock phases.

The shaded area of Fig. 3 indicates the D^{3}T structure which consists of two identical design-for-digital-testability (DfDT) SC networks. Each DfDT SC network is reconfigured as a 1-bit DCC during digital tests. The test-mode control pin T switches the operation mode of the D^{3}T Σ–Δ modulator between the normal mode or the digital test mode. By setting T to 0 and fixing the digital stimulus input pins D_{ij}, $j \in \{0, 1\}$ at 1, the D^{3}T modulator operates in the normal mode. The switches $S1_j$ to $S5_j$ are turned off due to the setup. Hence, the D^{3}T Σ–Δ modulator samples the analog inputs and converts them to a PDM bit-stream as a convectional second-order SC Σ–Δ modulator does.

Setting T to 1 turns off the switches SA_j, SB_j, and SE_j and makes the D^{3}T modulator operate in the digital test mode. The sampling capacitors C_{S0+}, C_{S0-}, C_{S1+}, and C_{S1-} now sample either V_{REF} or V_{CM} instead of the primary analog inputs during Φ_1. In Φ_2, the stored charges on the capacitors are transferred to either the integration capacitor C_{I1+} or C_{I1-} according to the values of the digital stimuli D_{i0} and D_{i1} and provide the desired discrete-time analog stimuli.

In our design, the sampling capacitors C_{S0+}, C_{S0-}, C_{S1+}, and C_{S1-} have the same size and the two digital stimuli D_{i0} and D_{i1} are the same bit-stream but with a relative delay of 4 clock cycles. It has been shown that an additional finite-impulse-response (FIR) term $\left(1 + z^{-4}\right)/2$ that provides low-pass filtering (LPF) capability is introduced to the signal transfer function (STF) of the D^{3}T Σ–Δ modulator [10] in the digital test mode.

This LPF term of the STF is a unique and the most important feature of the D^{3}T scheme. It effectively attenuates the shaped noise power of the digital stimuli that does not exist in their analog counterparts. Consequently, the loss of the test accuracy due to the shaped-noise correlation and the premature overload is substantially improved [10]. In addition to high test accuracy, the D^{3}T structure also provides the advantages such as a small silicon overhead since only several switches are added, high fault observability because most components are activated in both modes, and the capability of conducting at-speed tests thanks to the reconfiguration does not change the loads of the operational amplifiers.

The design of the decimation filter does not affect the BIST functions as long as it does not fold significant out-of-band noise back to the baseband after decimation and does not introduce significant passband ripples. The decimation filter used in this work consists of a three-stage comb filter followed by an amplitude equalizer and provides passband ripples less than ±0.05 dB. It is the same as what the conventional second-order Σ–Δ ADC would use, though adopting a four-stage comb filter would enhance the test accuracy [23].

3.2 BIST Design of the AUT

Though the input and the output of the D^{3}T Σ–Δ modulator are all bit-streams that already can be transmit-

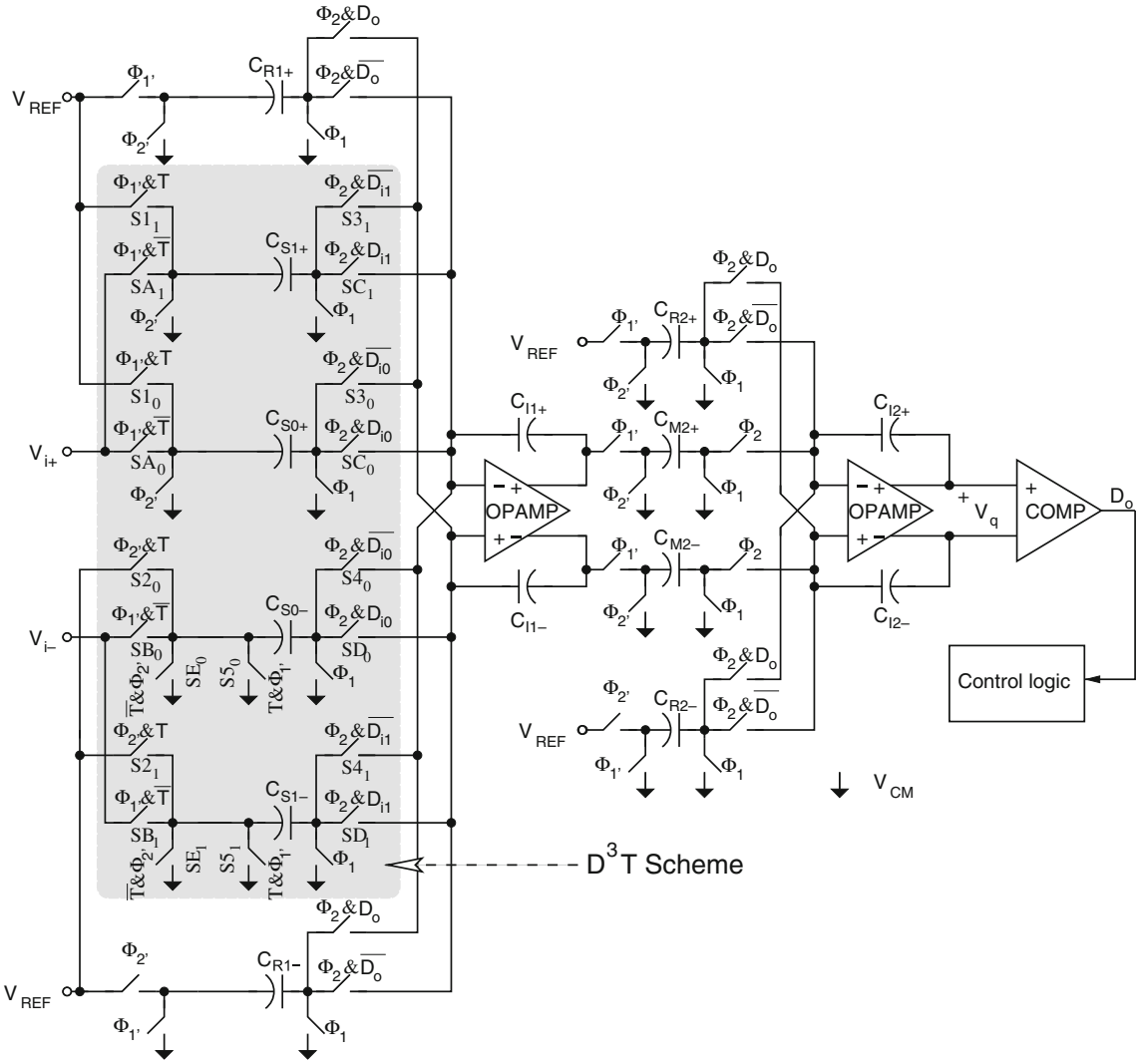

Fig. 3 Schematic of the D³T Σ–Δ modulator [10]

ted through the wireless channel without loss of SNDR accuracy, however, the real-time communication and the high data rate requirements make the design of the on-chip communication module too complicated to be cost-effective. Hence, it is necessary to adopt some BIST method incorporated with the D³T Σ–Δ modulator to further reduce the required test data rate.

One of the major issues of implementing the functional-test-alike BIST circuitry is how to make it cost-effective. For instance, conventional functional tests need to acquire many output samples of the AUT and then use FFT to derive the output spectrum. The measurement results such as the SNDR, the DR, the offset, and the gain error are calculated according to the derived spectral data. Directly adopting the FFT analysis method obviously suffers from the needs of a complex CPU/DSP and huge on-chip memory. The silicon overhead of the BIST circuitry is too large to be acceptable.

Mattes et al. [20] proposed the controlled sine wave fitting (CSWF) method that can test for the AUTs' SNDRs without FFT analysis. The main idea of the CSWF method is that the signal power and the THD+N power can be derived independently at different time. Recall that the output spectrum of an AUT of a standard single-tone test comprises the offset, the stimulus tone, and the total-harmonic-distortion-and-noise (THD+N) signal. Hence, we can derive the THD+N signal by removing the offset and the stimulus tone from the ADC's output in digital domain. Then, a simple power estimator can be used to accept the resulted THD+N signal and to output the THD+N power for calculating the SNDR of the AUT.

Based on the similar idea, reference [11] demonstrated a fully-integrated BIST Σ–Δ ADC in which the Σ–Δ modulator under test (MUT) was equipped with the DfDT SC structure proposed in [8]. The design proposed a modified CSWF BIST procedure that saved a lot of hardware overhead. The experimental results showed that the BIST design did achieve a low cost without significant compromise of the test accuracy [11].

In this work, the BIST design of the DUT follows the modified CSWF BIST procedure in [11], but the Σ–Δ MUT is the D^3T one to prove that the modified CSWF BIST procedure is also suitable for the D^3T Σ–Δ modulator. In addition, design efforts are made to further reduce the hardware overhead.

Figure 2 depicts the block diagram of the DUT. The BIST circuitry can be divided into the stimulus generation part, the ORA, and the BIST controller which communicates with the HOY test wrapper.

Two identical bit-stream generators (BSGs) generate the required Σ–Δ modulated bit-streams for the modified CSWF BIST procedure. The first one is the stimulus BSG (SBSG) which is in charge of generating the stimulus bit-stream for the analog D^3T modulator. The second one is the reference BSG (RBSG) that generates the digital reference signal for removing the the signal tone part of the MUT's responses according to the CSWF method. Both stimulus and reference signals are the 1-bit Σ–Δ modulated single-tone sinusoidal signals. They have the same frequency controlled by the parameter a_{21}, and their tone amplitudes are set by the parameters A_S and A_R, respectively. All these control parameters are transferred from the tester.

3.2.1 BIST Procedure

The modified CSWF BIST procedure comprises four steps [11]. Every BIST step conducts a coherent single-tone test and acquires N decimated outputs for analysis, where N is selected to be 2^{11}, a power of two, to simplify the hardware implementation.

Let A_T, f_T, and f_{clk} be the amplitude and the frequency of the desired single-tone stimulus and the oversampling frequency of the MUT, respectively. The following detail the BIST procedure.

Step 1: Calculating the Offset During the first BIST step, the SBSG generates a single-tone stimulus with an amplitude of $A_S = A_T\pi/4$ for the AUT. The ORA calculates the average of N decimated samples of the AUT which contain integer cycles of the stimulus tone. Because it is a coherent test, the average of the N samples is equal to the DC offset OS of the AUT.

Step 2: Calculating the Amplitude of the AUT's Response In the second step, the same stimulus is applied to the AUT again but the function of the ORA is changed. The ORA first removes the estimated offset in the previous step from the responses. Then, it accumulates twice the absolute values of the N offset-free samples. Mathematically, we have

$$A_{R4} = A_T \left| H_{DEC}\left(e^{\frac{j2\pi f_T}{f_{clk}}}\right)\right| \left| STF_{MUT}\left(e^{\frac{j2\pi f_T}{f_{clk}}}\right)\right|, \quad (1)$$

where $H_{DEC}(z)$ represents the transfer function of the decimation filter and $STF_{MUT}(z)$ is the STF of the Σ–Δ MUT. The final result of this step, A_{R4}, is the stimulus-tone amplitude of the decimated response which will be used to calculate the signal power of the test.

Step 3: Calculating the Amplitude of the Reference Signal The RBSG receives the setup of $A_R = A_T\pi/4$ and generates a purely digital reference stimulus in this step. The reference stimulus directly inputs the decimation filter and the ORA calculates the stimulus-tone amplitude of the decimated response. The final result, A_{S4}, can be expressed as

$$A_{S4} = A_T \left| H_{DEC}\left(e^{\frac{j2\pi f_T}{f_{clk}}}\right)\right|. \quad (2)$$

Notice that A_{S4} does not contain any information of the MUT, but the gain of the decimation filter.

Step 4: Calculating the THD+N Power The final step is to calculate the THD+N power. By setting A_S to A_{S4} and A_R to A_{R4}, the stimulus tone level of the output bit-stream of the MUT is

$$A_{S4}\left|STF_{MUT}\left(e^{\frac{j2\pi f_T}{f_{clk}}}\right)\right| = A_T \left|STF_{MUT}\left(e^{\frac{j2\pi f_T}{f_{clk}}}\right)\right| \left|H_{DEC}\left(e^{\frac{j2\pi f_T}{f_{clk}}}\right)\right|, \quad (3)$$

which is the same as A_{R4} according to Eq. 1. Since the STF of the analog Σ–Δ modulator has a gain very close to 1 within the rated passband and the passband ripples of the decimation filter are less than ±0.05 dB, the stimulus level of the fourth BIST step A_{R4} is close to the desired value A_T. An additional delay of 4 clock cycles is added to the path of the reference signal to compensate for the phase delay introduced by the D^3T MUT so that the tones of the MUT's output and the reference signal are not only of the same amplitude but also in phase.

The ORA first eliminates the stimulus tone part of the response by subtracting the reference signal $y_{ref}(n)$ from the MUT's response $y_{mut}(n)$. Then, it further

Table 1 Summary of the BIST procedure

	A_S	A_R	BIST functions
Step 1	$\frac{A_T\pi}{4}$	N/A	$OS = \frac{1}{N}\sum_{n'=1}^{N} y_{res}(n')$
Step 2	$\frac{A_T\pi}{4}$	N/A	$A_{R4} = \frac{2}{N}\sum_{n'=1}^{N} \lvert y_{res}(n') - OS\rvert$
Step 3	N/A	$\frac{A_T\pi}{4}$	$A_{S4} = \frac{2}{N}\sum_{n'=1}^{N} \lvert y_{res}(n')\rvert$
Step 4	A_{S4}	A_{R4}	$P_{THDN} = \frac{1}{N}\sum_{n'=1}^{N} \lvert y_{res}(n') - OS\rvert^2$, $SNDR = \frac{A_{R4}^2}{2P_{THDN}}$

removes the offset from the decimated response and results in the desired THD+N signal. Finally, the ORA calculates the THD+N power, P_{THDN}, by accumulating the squares of the N THD+N samples and taking the average of the result. The final SNDR result is obtained as the ratio of the $A_{R4}^2/2$ and the calculated THD+N power.

Table 1 summarizes the BIST procedure including the corresponding test setup and ORA functions where n' represents the sample index after decimation.

3.2.2 Implementation of the Bit-Stream Generators

As explained above, the modified CSWF BIST procedure requires two BSGs to generate the Σ–Δ modulated bit-streams. A low-cost BSG that can generate single-tone outputs for the purpose of on-chip tests has been proposed in [19]. Figure 4 shows the block diagram of the BSG which is structurally a digital resonator. It generates a multi-bit sinusoidal wave at D_{OSC}. By embedding a digital Σ–Δ modulator with an

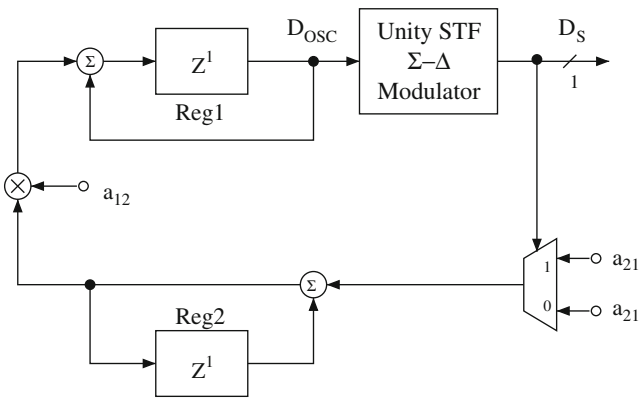

Fig. 4 The low-cost BSG embedded with a unity-STF Σ–Δ modulator

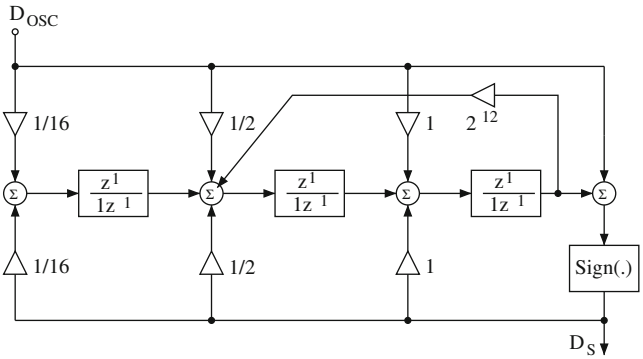

Fig. 5 The third-order Σ–Δ modulator adopted in the BSG

STF of unity and fixing the parameter a_{12} at a value of a power of 2, this implementation eliminates the need of multipliers so as to achieve a small hardware overhead.

For our BIST application, the BSG also can generate the required Σ–Δ modulated bit-stream. The frequency of the test tone is mainly controlled by the value of the frequency parameter a_{21} which must be carefully designed to follow the coherent test criteria [3]. Meanwhile, the amplitude of the test tone can be set by the initial values of the registers 1 and 2 [19].

In order to provide higher resolution stimuli, we adopted the digital third-order modulator shown in Fig. 5 as the required unity-STF Σ–Δ modulator in Fig. 4 [11]. The third-order Σ–Δ modulator has better noise shaping capability and thus the generated digital stimuli have less noise power left in the rated passband. By properly truncating the digital signals in the third-order Σ–Δ modulator, the final gate count of the BSG is only 3.05k [11].

3.2.3 Implementation of the Output Response Analyzer

The ORA is designed to implement the BIST functions listed in Table 1 for calculates the test results in real time. Keeping the hardware overhead as low as possible is the main concern for the ORA design. After reexamining the ORA equations of the four BIST steps, it is found that they perform similar arithmetic operations.

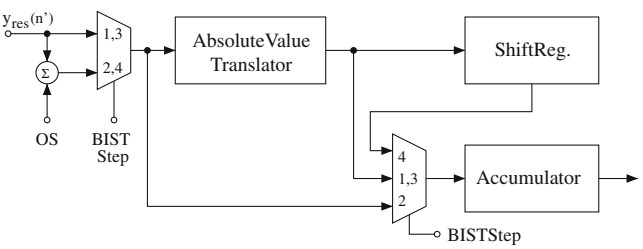

Fig. 6 Implementation of the ORA

It implies they can share the same circuits such as the accumulator and the absolute-value translator. Figure 6 shows the implementation of the ORA. Thanks to the hardware sharing, the ORA consists of only 2.0k gates [15].

3.2.4 Test Time

Each BIST totally consumes 292 ms including 22 ms for initializing the analog Sigma–Delta modulator, 170 ms for the four BIST steps, and 100 ms for exchanging data with the test host. On the other hand, a conventional analog test has a negligible communication time and consumes about one seventh of the test time. A longer test time for the BIST would not increase the test cost because conducting the BIST does not require high-end mixed-signal ATE but a low-cost laptop.

4 Experimental Results

The DUT composed of the fully-integrated BIST Σ–Δ ADC has been fabricated in 0.18-μm CMOS. Figure 7 shows the micrograph of the test chip. The analog core, the D^3T Σ–Δ modulator, occupies 0.42 mm^2 and the active area of the digital decimation filter is 0.199 mm^2. The active area of the whole ADC without the BIST circuitry is 0.619 mm^2. The additional BIST circuitry consists of 9.9 k digital gates and occupies 0.131 mm^2. The overall hardware overhead is around 17.5%. The silicon overhead of the all-digital BIST circuitry would be much smaller when the design is ported to advanced technology. Table 2 summarizes the test chip.

The test chips were tested on the HOY wireless test platform. Figures 8 and 9 illustrate the photography and the test setup of the complete HOY wireless test platform for the following BIST experiments, respectively.

Table 2 Summary of the test chip

Process	0.18-μm CMOS	
Test chip area	1.54 mm by 1.18 mm	
Block	**Gate count**	**Area**
D^3T Σ–Δ modulator	n/a	0.42 mm^2
Decimation filter	15.0k	0.199 mm^2
Whole ADC		0.619 mm^2
Whole BIST circuitry	9.9k	0.131 mm^2
BSG	3.05k ×2	0.081 mm^2
ORA	2.0k	0.026 mm^2
BIST controller and I/O	1.8k	0.024 mm^2

For the tester shown in Figs. 1 and 9, we used a laptop as the test host, an FPGA board to implement the test head functions, and an RF circuit board for wireless communication. The DUT consists of a load board on which the BIST D^3T Σ–Δ ADC chip is mounted, an FPGA board to implement the communication module and the test wrapper, and an RF circuit board for wireless communication. The wireless test head and the DUT are integrated into two 15 cm-by-15 cm boxes, respectively.

The whole test procedure was fully automatic with the help of the HOY test program mentioned in Section 2. We used the test program running on the test host to set up the test suits and to receive the test results. Each test suit consists of several tests with different stimulus amplitudes or frequencies. By just clicking a button, the tester delivers the test instructions to the DUT, receives the BIST results from the DUT, and displays them on the GUI of the tester like conventional ATE does. Two example snapshots of the test results on the GUI are shown in Figs. 10

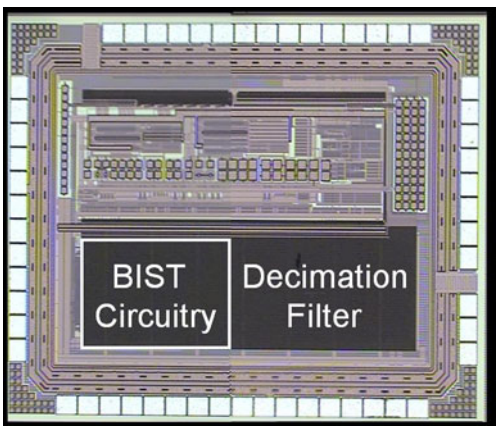

Fig. 7 Micrograph of the BIST Σ–Δ ADC chip

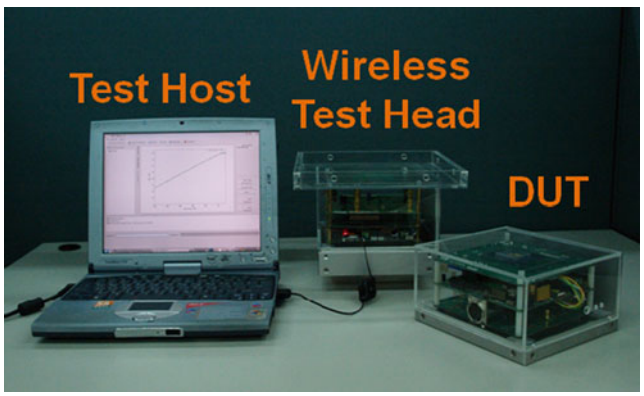

Fig. 8 Photograph of the HOY wireless test platform for testing the fully integrated BIST ADC chip

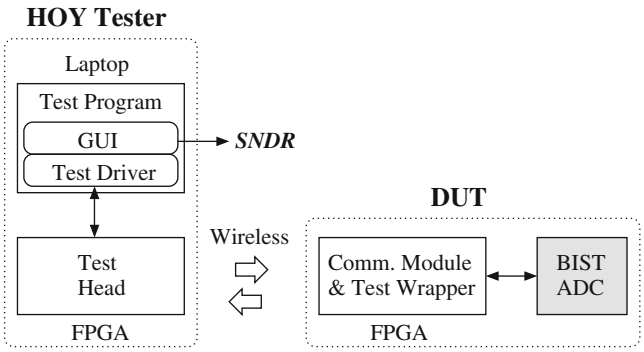

Fig. 9 Test setup of the wireless tests

and 11. They show how convenient the HOY wireless test platform is.

4.1 Wireless Test Results

Two test suits were conducted on the HOY wireless test platform. One is for testing the DR performance of the AUT and the other is for testing the frequency responses of the AUT.

Figure 10 shows the snapshot of the GUI which displays the test results at 1 kHz stimulus frequency. The stimulus amplitude was swept from −60 dBFS to −3 dBFS with a 2-dB step till −8 dB. Then, the step was reduced to 1 dB. The wireless test results reported a peak SNDR of 78.6 dB which occurs at a stimulus level of −6 dBFS. Figure 10 also indicates that the AUT achieves a DR of 85.1 dB.

Figure 11 illustrates the screen snapshot of the test host which displays the tested SNDR results vs. stimulus frequencies. The amplitudes of the stimuli were kept at the same −6 dBFS. The measured SNDR values vary by less than 3 dB for the stimulus frequencies lower than 17 kHz. In other words, the tested passband with the CSWF BIST method is 17 kHz which is pretty close to the rated 20-kHz passband of the AUT.

4.2 Conventional Analog Test Results

To verify the test accuracy, we also performed the corresponding analog tests of the AUT in the conventional way. Figure 12 depicts the test setup used to conduct the conventional analog tests. Since a low-noise environment is essential for high test accuracy, a customized evaluation board was implemented. We used the Audio Precision system as the analog stimulus generator and a logic analyzer with a memory depth of 2M bits per channel to capture the outputs. The acquired output samples were analyzed in the test host

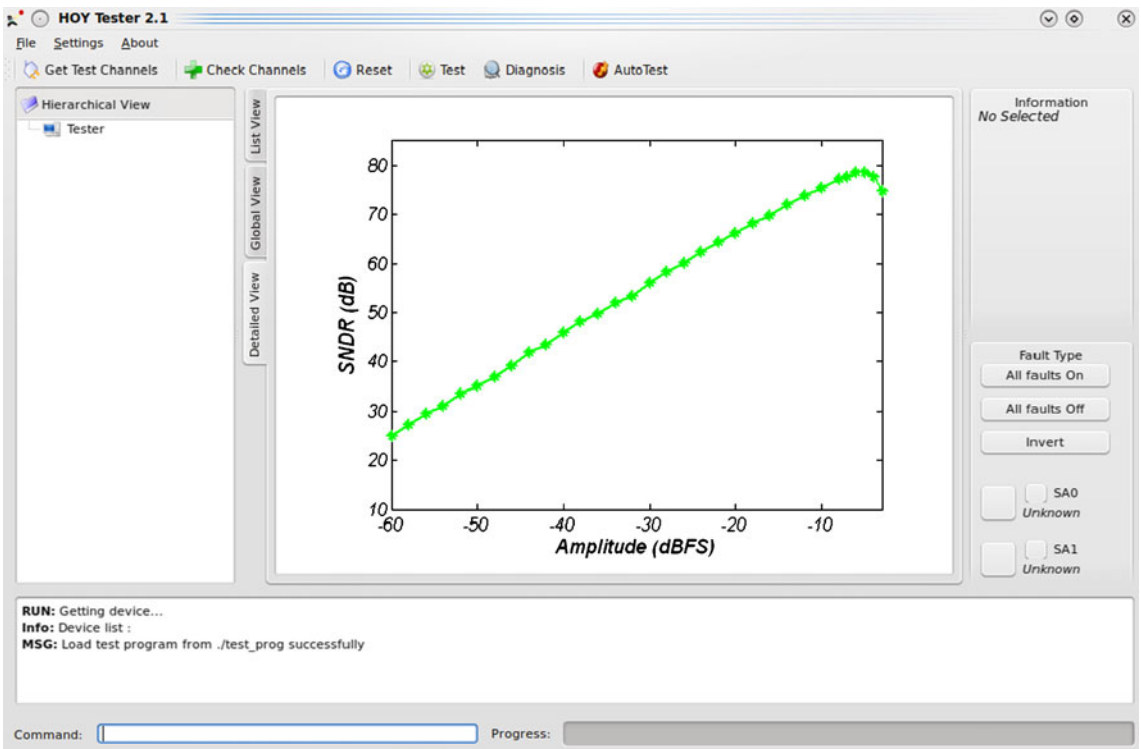

Fig. 10 GUI snapshot of the wireless BIST results of stimulus level vs. SNDR

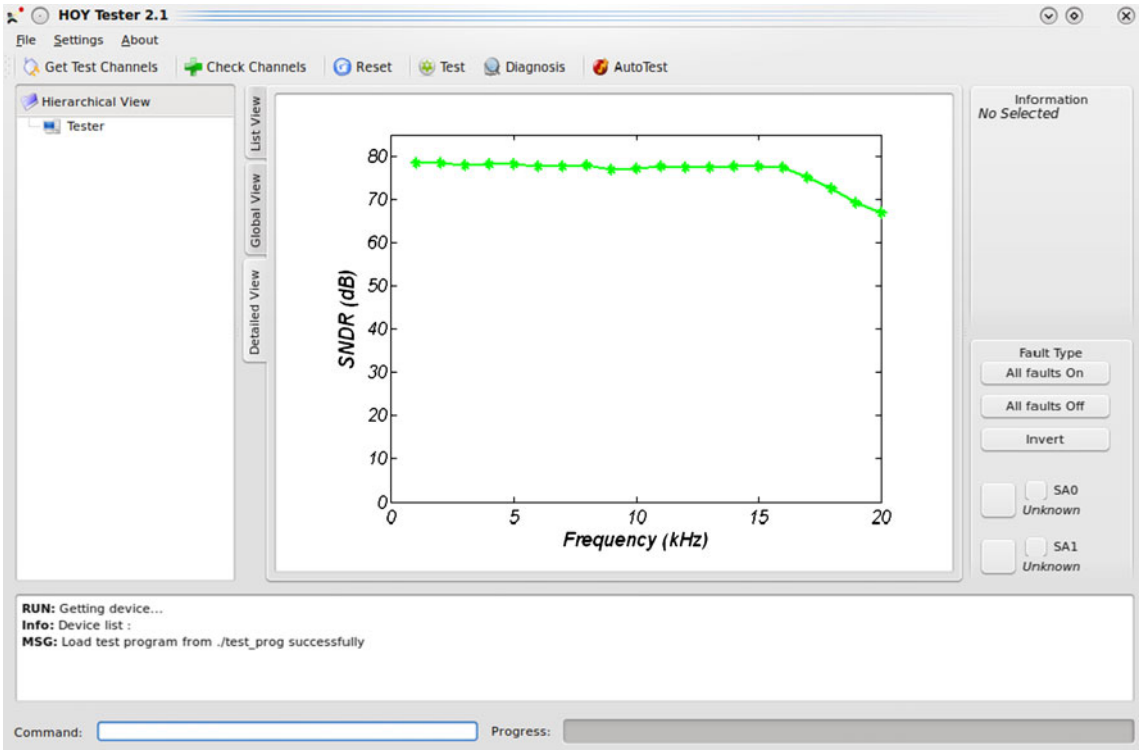

Fig. 11 GUI snapshot of the wireless BIST results of the frequency responses

using FFT analysis provided by Matlab. Comparing with the wireless test platform, lots of setup efforts are necessary for the analog tests.

Figure 13 plots the wireless test results by BIST and the corresponding analog test results. They shows good agreement in most tests. The peak SNDR and the DR reported by the conventional analog tests are 81.5 dB and 86.7 dB respectively.

Figure 14 shows the SNDR differences between the analog test results and those of the corresponding wireless tests. The SNDR differences are less than 2 dB for the stimulus levels smaller than −6 dBFS.

4.3 Digital Test Results with FFT

Although the BIST results already show good test accuracy, it is interesting to examine why the BIST SNDR results degrade when the stimulus level is higher than −5 dBFS. Recall the major differences between the BIST and conventional analog test are the analog stimulus generation and the output response analysis methods. Both of them may cause the differences.

We conducted the digital tests to check if the CSWF ORA was the root cause of the tested SNDR degradation. Figure 15 shows the test setup of the digital tests

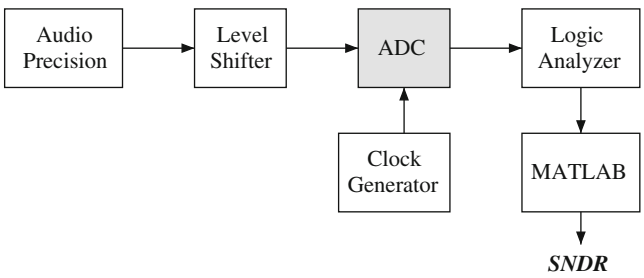

Fig. 12 Test setup of the conventional analog tests

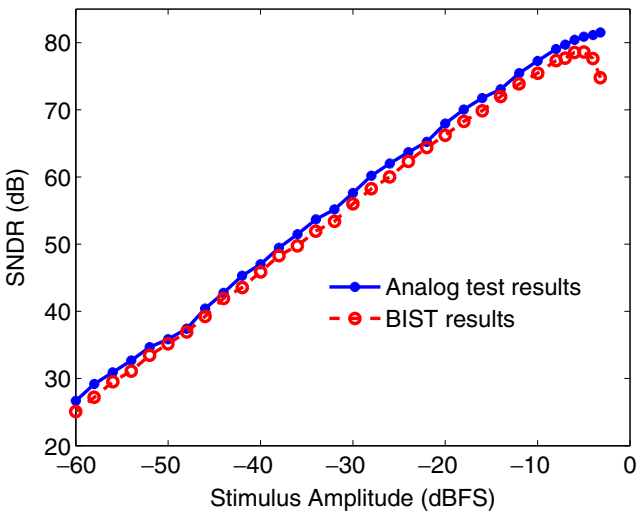

Fig. 13 Wireless BIST results and the corresponding analog test results

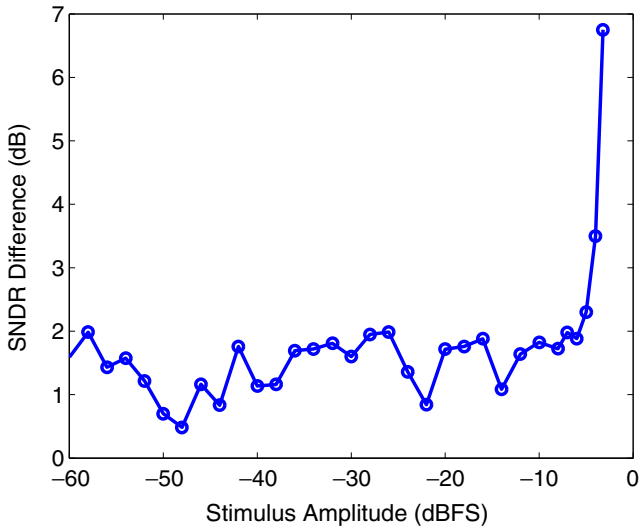

Fig. 14 SNDR differences between the analog test results and the corresponding BIST results

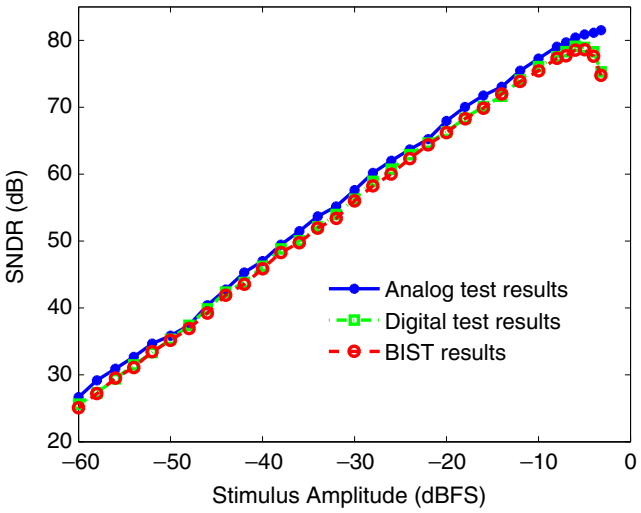

Fig. 16 Test results of stimulus level vs. SNDR of the three test methods

which is similar to that of the BIST. The digital stimulus is also generated by the same embedded SBSG, but the AUT's responses are captured by a logic analyzer to be analyzed by FFT. Figures 16 and 17 illustrate the test results and the corresponding SNDR differences of the three test methods.

According to Fig. 17, the SNDR differences between the test results of the two test methods using the same digital stimuli are in the range of −0.3 dB to 0.7 dB. Such tiny SNDR differences are already within the inherent uncertainty of the ADC tests. It implies the ORA of the CSWF BIST circuitry is not the root cause of the SNDR degradation.

To provide an additional proof about the correctness of the CSWF ORA, we conducted behavioral simulations with the FSLB+N model proposed in [9] to check if the CSWF procedure works correctly for the D^{3}T Σ–Δ AUT. Figure 18 shows the simulated output spectra of the $y_{mut}(n)$ after being decimated and $y_{res}(n')$ of the fourth BIST step and their cumulative THD+N power plots. The two spectra were derived by FFT analysis. The plots show both the offset and the stimulus tone of $y_{res}(n')$ successfully vanish to the noise floor as desired. In addition, the noise floors of the two spectra are almost the same. The experimental results show the BIST results are as accurate as their digital test counterparts. Consequently, we suspected the root cause of the SNDR accuracy degradation of the BIST is due to the stimulus generation part.

To verify our deduction, Fig. 19 plots the measured output spectra of the 1-kHz, −6-dBFS analog test and digital test. The plots show that the noise floor of the digital test is higher than that of the corresponding

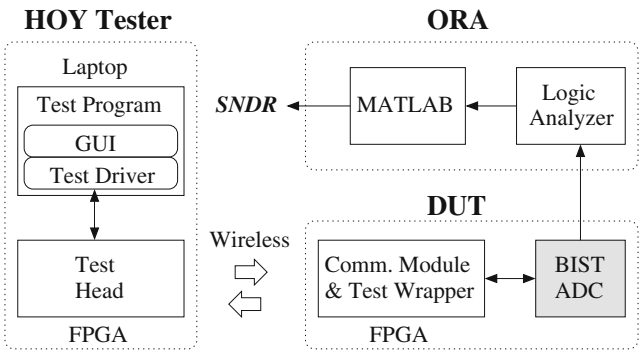

Fig. 15 Test setup of the digital tests

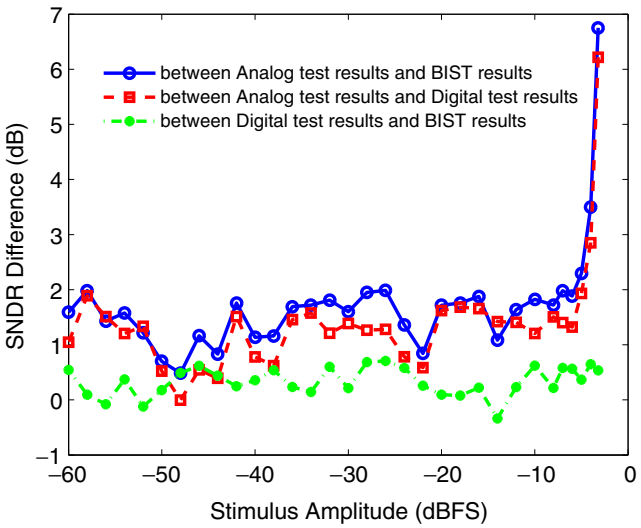

Fig. 17 SNDR differences among the three test methods

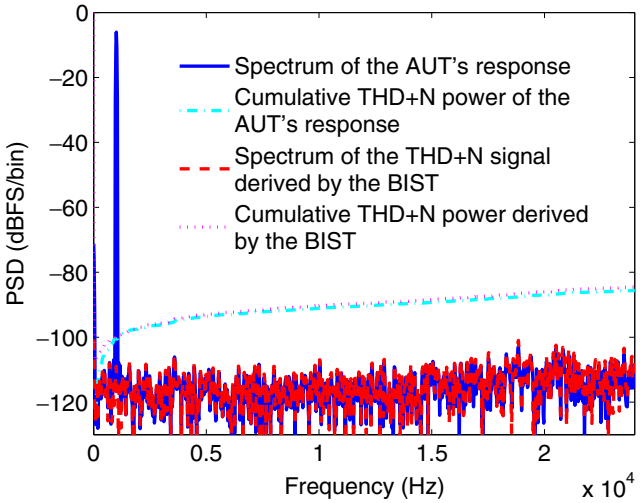

Fig. 18 Simulated output spectra of the 1-kHz, −6-dBFS digital test and the corresponding BIST with the FSLB+N model

analog one leading to the SNDR difference. Recall the stimulus of the digital test consists of some shaped noise while that of the analog test does not. Although the D^3T structure provides some LPF capability to reduce the shaped noise of the digital stimulus, the remained shaped noise power still makes the MUT suffering from the shaped noise correlation and modulator premature overloaded effects [8, 10]. Both effects degrade the tested SNDR at high stimulus levels. Table 3 summarizes the test results.

The proposed BIST design could be used to test the AUTs achieving higher SNDR values. Hung and Hong [14] depicted the simulation results of a third-order Σ–Δ AUT and showed the digital tests could measure a peak SNDR of 85.5 dB. However, the aforementioned intrinsic nonidealities of the digital tests still limit the measured peak SNDR.

Table 3 Summary of the test results

	Analog test	Digital test	CSWF BIST
Stimulus type	Analog stimulus	Σ–Δ modulated bit-stream	Σ–Δ modulated bit-stream
Analytic method	FFT Analysis	FFT Analysis	BIST based on CSWF
Peak SNDR	81.5 dB @ −3 dBFS	79.1 dB @ −6 dBFS	78.6 dB @ −6 dBFS
DR	86.7 dB	85.6 dB	85.1 dB

4.4 Frequency Response Test Results

Figure 20 plots the tested frequency responses of the three kinds of tests. The stimulus amplitude was kept at −6 dBFS for all tests. The wireless BIST results are very close to those of the digital tests, but lower than those of the analog test. Note that the tested SNDR values by the wireless BIST are almost a constant for the stimulus frequencies no more than 16 kHz. The BIST SNDR result at 17 kHz drops less than 3 dB. In other words, the BIST circuitry can provide a 17-kHz test bandwidth which is pretty close to the rated 20-kHz passband of the AUT.

To realize why the BIST method presented lower SNDR values for the stimulus frequencies higher than 17 kHz, we conducted the behavioral simulations with the FSLB+N model again. Figure 21 plots the simulated output spectra of the 18-kHz, −6-dBFS tests. Comparing the two cumulative THD+N plots with

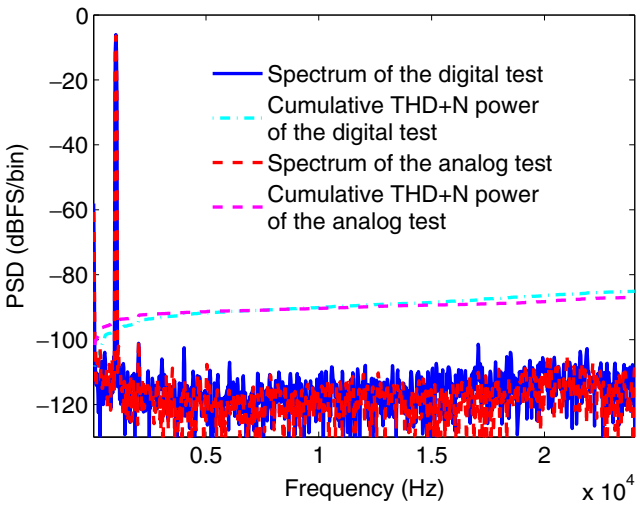

Fig. 19 Measured output spectra of the 1-kHz, −6-dBFS analog and digital tests

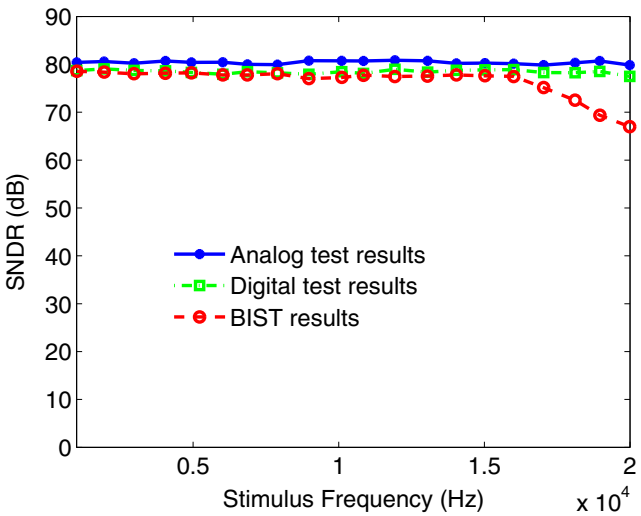

Fig. 20 Measured SNDR results vs. stimulus frequencies

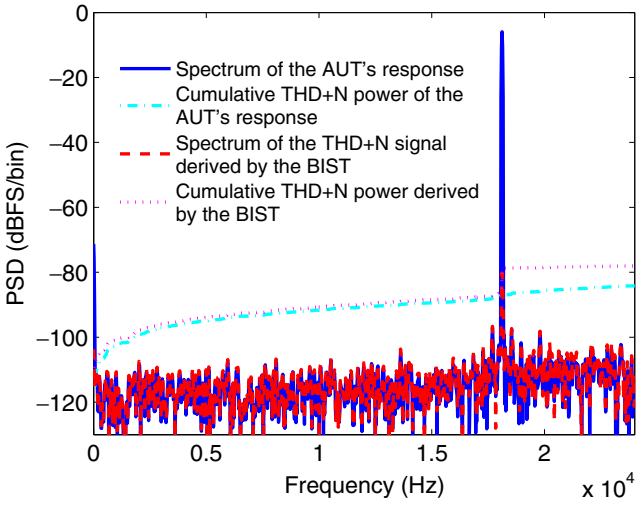

Fig. 21 Simulated output spectra of the 18-kHz, −6-dBFS digital test and BIST with the FSLB+N model

each other, it is clear that the residue stimulus tone leads to the SNDR degradation.

Actually, the raised residue tone level is the result of incomplete stimulus tone cancellation in the fourth BIST step. Ideally, we expect the output bit-stream of the MUT and the reference bit-stream in the fourth BIST step consisting of the same stimulus tone in both amplitude and phase. However, the phase shift between the output and the input of the MUT is stimulus frequency dependent in practice. Since the BIST implementation assumes the phase shift of the MUT is equal to two clock cycles regardless the stimulus frequency, the phase error increases when the stimulus frequency becomes higher. Note that a tiny phase error between the MUT's response and the reference signal could induce a significant residue tone to the THD+N signal. Hence, the BIST results are getting worse for higher frequencies. This is an intrinsic limitation of the CSWF BIST design [11].

5 Conclusion

This paper demonstrates the system-level integration including hardware and software of testing a fully-integrated BIST Σ–Δ AUT on the HOY wireless test platform. This is the first work to exhibit the possibility of testing AMS circuits on the HOY wireless test platform. The test chip consisting of the Σ–Δ AUT and the BIST circuits has been fabricated in 0.18-μm CMOS. The AUT employs the particular D^3T SC structure at its input stage which makes the AUT digitally testable. We adopted the modified CSWF BIST procedure to design the BIST circuitry to make the AUT built-in self-testable. The hardware overhead of the purely digital BIST circuits is only 9.9 k gates corresponding to an area overhead about 17.5% of the whole BIST AUT. The BIST AUT was successfully tested on the HOY wireless test platform without expensive AMS ATE and compromise of test accuracy. Experimental results of the wireless tests showed that the Σ–Δ AUT achieved a DR of 85.1 dB and a peak SNDR of 78.6 dB which are as accurate as those obtained by a bulky FFT analyzer.

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References

1. Alampally S, Venkatesh RT, Shanmugasundaram P, Parekhji RA, Agrawal VD (2011) An efficient test data reduction technique through dynamic pattern mixing across multiple fault models. In: Proc. IEEE VLSI test symp. (VTS), pp 285–290
2. Al-Yamani AA, McCluskey EJ (2010) Test set compression through alternation between deterministic and pseudorandom test patterns. J Electron Test (JETTA) 26(5):513–521
3. Burns M, Roberts G.W. (2001) An introduction to mixed-signal IC test and measurement. Oxford University Press, Oxford
4. Bushnell ML, Agrawal VD (2000) Essentials of electronics testing for digital, memory & mixed-signal VLSI circuits. Kluwer Academic, Norwell
5. Chi C-C, Lo C-Y, Ko T-W, Wu C-W (2009) Test integration for SOC supporting very low-cost tester. In: IEEE Asian test symp. (ATS), pp 287–292
6. Chouba N, Bouzaida L (2010) A BIST architecture for Sigma Delta ADC testing based on embedded NOEB self-test and CORDIC algorithm. In: Proc. IEEE int. conf. design and technology of integrated systems in nanoscale era (DTIS), pp 1–7
7. Hong H-C (2004) Design-for-digital-testability 30 MHz second-order Sigma–Delta modulator. In: Proc. IEEE custom integrated circuits conf. (CICC), pp 211–214
8. Hong H-C (2007) A design-for-digital-testability circuit structure for Σ–Δ modulators. IEEE Trans VLSI Syst 15(12):1341–1350
9. Hong H-C (2007) A fully-settled linear behavior plus noise model for evaluating the digital stimuli of the design-for-digital-testability Σ–Δ modulators. J Electron Test (JETTA) 23(6):527–538
10. Hong H-C, Liang S-C (2009) A decorrelating design-for-digital-testability scheme for Σ–Δ modulators. IEEE Trans Circuits Syst I, Reg Pap 56(1):60–73
11. Hong H-C, Su F-Y, Hung S-F (2010) A fully integrated built-in self-test Σ–Δ ADC based on the modified con-

trolled sine-wave fitting procedure. IEEE Trans Instrum Meas 59(9):2334–2344
12. Hsing Y-T, Denq L-M, Chen C-H, Wu C-W (2010) Economic analysis of the HOY wireless test methodology. IEEE Des Test Comput 27(3):20–30
13. Huang X-L, Kang P-Y, Yu Y-C, Huang J-L (2011) Histogram-based calibration of capacitor mismatch and comparator offset for 1-bit/stage pipelined ADCs. J Electron Test (JETTA) 27(4):441–453
14. Hung S-F, Hong H-C (2011) Design of a design-for-digital-testability third-order Σ–Δ modulator. In: Proc. IEEE 17th international mixed-signals, sensors and systems test workshop, pp 110–113
15. Hung S-F, Hong H-C, Liang S-C (2009) A low-cost output response analyzer for the built-in-self-test Σ–Δ modulator based on the controlled sine wave fitting method. In: IEEE Asian test symp. (ATS), pp 385–388
16. Kochte MA, Zoellin CG, Wunderlich H-J (2010) Efficient concurrent self-test with partially specified patterns. J Electron Test (JETTA) 26(5):581–594
17. Li C-F, Lee C-Y, et al (2011) A low-cost wireless interface with no external antenna and crystal oscillator for cm-range contactless testing. In: Proc. IEEE/ACM design automation conf. (DAC), pp 771–776
18. Liou J-J, Huang C-T, Wu C-W, Tien C-C, Wang C-H, Ma H-P, Chen Y-Y, Hsu Y-C, Deng L-M, Chiu C-J, Li Y-W, Chang C-M (2007) A prototype of a wireless-based test system. In: IEEE int. SOC conf. (SOCC), pp 225–228
19. Lu AK, Roberts GW (1994) A high-quality analog oscillator using oversampling D/A conversion techniques. IEEE Trans Circuits Syst II Analog Digit Signal Process 41(7):437–444
20. Mattes H, Sattler S, Dworski C (2004) Controlled sine wave fitting for ADC test. In: Proc. IEEE int. test conf. (ITC), pp 963–971
21. Mehta US, Dasgupta KS, Devashrayee NM (2010) Modified selective Huffman coding for optimization of test data compression, test application time and area overhead. J Electron Test (JETTA) 26(6):679–688
22. Mullane B, O'Brien V, MacNamee C, Fleischmann T (2009) A prototype platform for system-on-chip ADC test and measurement. In: IEEE int. SOC conf. (SOCC), pp 169–172
23. Rolindez L, Mir S, Bounceur A, Carbonero J-L (2006) A BIST scheme for SNDR testing of Σ–Δ ADCs using sine-wave fitting. J Electron Test (JETTA) 22(4–6):325–335
24. Rolindez L, Mir S, Carbonero J-L, Goguet D, Chouba N (2007) A stereo audio Σ–Δ ADC architecture with embedded SNDR self-test. In: Proc. IEEE int. test conf. (ITC), pp 1–10
25. Santin E, Oliveira L, Nowacki B, Goes J (2010) Fully integrated and reconfigurable architecture for coherent self-testing of IQ ADCs. In: Proc. IEEE int. symp. circuits and systems (ISCAS), pp 1927–1930
26. Ting H-W, Chang S-J, Huang S-L (2011) A design of linearity built-in self-test for current-steering DAC. J Electron Test (JETTA) 27(1):85–94
27. Toner MF, Roberts GW (1995) A BIST scheme for a SNR, gain tracking, and frequency response test of a Sigma–Delta ADC. IEEE Trans Circuits Syst II Analog Digit Signal Process 42(1):1–15
28. Vinnakota B (1998) Analog and mixed-signal test. Prentice-Hall, Englewoods Cliffs
29. Wang Z, Karpovsky M, Kulikowski KJ (2010) Design of memories with concurrent error detection and correction by nonlinear sec-ded codes. J Electron Test (JETTA) 26(5):559–580
30. Wu C-W, Huang C-T, Huang S-Y, Huang P-C, Chang T-Y, Hsing Y-T (2006) The HOY tester—can IC testing go wireless? In: Proc. IEEE int. symp. VLSI design, automation and test, pp 1–4
31. Yang C-Y, Chen Y-Y, Chen S-Y, Liou J-J (2010) Automatic test wrapper synthesis for a wireless ATE Platform. IEEE Des Test Comput 27(3):31–41

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