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PAPER

Cumulative Differential Nonlinearity Testing of ADCs

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SUMMARY This paper proposes a cumulative DNL (CDNL) test methodology for the BIST of ADCs. It analyzes the histogram of the DNL of a predetermined k LSBs distance to determine the DNL and gain error. The advantage of this method over others is that the numbers of required code bins and required samples are significantly reduced. The simulation and measurements of a 12-bit ADC show that the proposed CDNL has an error of less than 5% with only 2^{12} samples, which can only be achieved with 2^{22} samples using the conventional method. It only needs 16 registers to store code bins in this experiment.
key words: *cumulative differential nonlinearity, gain error, jitter calibration, analog-to-digital converters (ADCs)*

1. Introduction

In recent years, the improvement in the speed of wireless and wired line communications, and the reduction in cost have generated significant demand for the design and test of mixed-signal integrated circuits — especially *analog-to-digital and digital-to-analog converters* (ADC/DAC). Although *system-on-chip* (SoC) can reduce the cost of production and improve the performance, they raise great challenges for the test and verification of AD/DA converters, because the switching noise that is generated by the digital part greatly degrades the *signal-to-noise ratio* (SNR) of the analog signals and increases the jitter in the sampling clocks. As a result, the test and verification of on-chip AD/DA converters is critical.

Among the test items of AD/DA converters, the nonlinearities — both *integral nonlinearity* (INL) and *differential nonlinearity* (DNL) — are significantly affected by the SNR and jitters. The need for high accuracy, with a resolution of less than 0.5LSB (*least significant bit*), requires high-SNR test signals and low-jitter clocks. Hopefully, oversampling and averaging techniques can overcome the issues of noise and jitter. The resulting samples are then averaged for the resulting output data. However, because of the exponential complexity (2^n), the test consumes much time and resources when the bit length is large and the test conditions are not benign.

The tolerance and confidence levels in the ADC test methods are described in IEEE Std. 1057 [1] and IEEE Std. 1241 [2]. Histogram-based methods are commonly used for ADC testing [3]–[9]. They determine gain, offset, and nonlinearity error by checking the histograms. Methods to reduce the effects of noise [10]–[12] and jitter [13]–[15] improve accuracy.

To handle the complexity of testing under the influence of noise and jitter, a test methodology, called *cumulative differential nonlinearity* (CDNL), is proposed. Checking the DNL of a predetermined number of LSBs (k) at random enables the distribution function of the conventional DNL to be derived. The maximal DNL is thus known and whether the pass or fail can be determined. Therefore, whereas the conventional DNL test method requires 2^n code bins, the proposed method requires only a total of $2J$ code bins for storage, where J represents the combination of the clock jitter, noise, and DNL of the ADC in terms of LSB.

The rest of the paper is organized as follows. Section 2 elucidates the theoretical background of CDNL. Section 3 presents in detail the CDNL test procedures. Section 4 presents the simulation results. Section 5 shows the experimental results. Section 6 draws conclusions.

2. Proposed Cumulative DNL Method

Conventionally, the DNL of a code is defined as the difference between its code bin width and the average code bin width, divided by the average code bin width. For example, for a 10-bit ADC with 1 V conversion range, the average code bin width, or one LSB, is roughly 1 mV, $1\,V/2^{10}$. The width of code bin $\boldsymbol{i}$ in Fig. 1 is 1.5 mV or 1.5LSB. Hence, the DNL for code bin $\boldsymbol{i}$ is 0.5LSB.

The DNL test method, provided by IEEE Std. 1057 [1], is as follows. A ramp or sinusoidal waveform is sampled and the resulting codes are stored in their correspond-

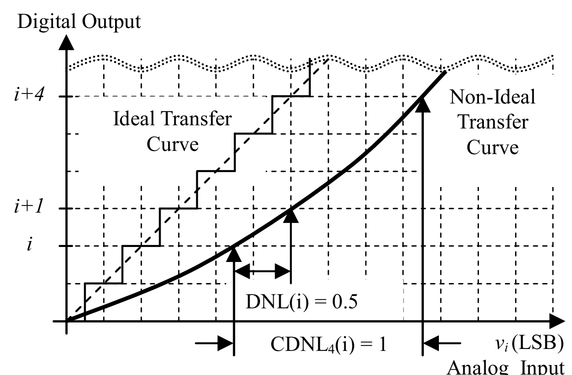

Fig. 1 DNL vs. CDNL.

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ing code bins. As a result, 2^n code bins are required to store the histogram. For a ramp input, the DNL is defined as *"the difference between a specified code bin width and the average code bin width divided by the average code bin width"* in [1]. Here, the DNL of every code is tested. The maximal one is selected to represent the characteristics of the circuit. The complexity of the determination of the DNL for every code is $O(2^n \times OSR)$, where OSR is the *oversampling rate* or average number of samples per code. The complexity is high, especially when n is large. It is a significant overhead for the *built-in self test* (BIST). Therefore, this study proposes a method that is suitable for use in the BIST.

2.1 Definition of CDNL

To overcome the resolution, noise, and jitter issue, the sample interval is chosen to be across multiple code widths. The cumulative DNL or CDNL is defined as,

$$CDNL_k(i) = v(i+k) - v(i) - k \times LSB. \tag{1}$$

$v(i)$ is the transition level for code $\boldsymbol{i}$ in LSB. In the example in Fig. 1, $CDNL_4(i) = 1LSB$, and can be represented as the sum of the DNLs for consecutive k codes,

$$CDNL_k(i) = \sum_{j=0}^{k-1} DNL(i+j). \tag{2}$$

Suppose that the DNL has a Gaussian distribution with a variance of σ^2_{DNL}. The variance of $CDNL_k$ without noise/jitter is

$$\sigma^2_{CDNL_k_ideal} = k \cdot \sigma^2_{DNL}. \tag{3}$$

The *standard deviation* (STD) of the CDNL is $\sqrt{k}$ times larger than that of the DNL. Therefore, it has a higher SNR in measurement. Notably, the conventional DNL is a special case of CDNL with $k = 1$.

The problems of jitter and noise are solved by a conventional oversampling technique. Suppose that the jitter is transformed into noise by

$$\sigma^2_{nj} = (\sigma_j \cdot l)^2. \tag{4}$$

$$\sigma^2_n = \sigma^2_{nj} + \sigma^2_{ni}. \tag{5}$$

Here, σ^2_j, σ^2_{ni}, and σ^2_n are the variances of jitter, noise, and the combination of jitter and noise and l is the slope of the transfer curve. According to (1), $CDNL_k$ is the difference between the two random variables, $v(i+k)$ and $v(i)$. Therefore, the effect of jitter and noise on $CDNL_k$ has a *probability density function* (PDF) of

$$f_n(x) = \frac{1}{\sqrt{2\pi}\sqrt{2}\sigma_n} \cdot e^{-\frac{1}{2}\left(\frac{x}{\sqrt{2}\sigma_n}\right)^2}. \tag{6}$$

With noise/jitter and DNL, $CDNL_k$ has a variance of

$$\sigma^2_{CDNL_k} = k \cdot \sigma^2_{DNL} + 2\sigma^2_n. \tag{7}$$

The number of code bins for store the histogram of CDNL is dependent on confidence level of measurement. Six σ_{CDNL_k} can cover 99.7% sample data. From the histogram of $CDNL_k$, $\sigma^2_{CDNL_k}$ can be obtained. If σ^2_n is known, then σ^2_{DNL} can be obtained by (7). The method for calibrating σ^2_n will be discussed later.

The above discussion is based on the independence of DNLs. There are some assumptions. First, that the model for the ADC is a quantizer with a Gaussian noise source added to the input of the device. The measurement will be somewhat erroneous if the dominant noise source is non-Gaussian. Second, the architecture of the device affects the measurements; but the technique is valid for the majority of high-speed, pipelined converters.

Flash ADCs (sometimes called parallel ADCs) are the fastest type of ADC and use large numbers of comparators. An n-bit flash ADC consists of 2^n resistors and $2^n - 1$ comparators arranged. The DNL distribution of ADC in the well-designed circuit is almost Gaussian. Because the process variation of resistors is Gaussian distribution and the offset of comparators in the flash ADC is also Gaussian distribution [16], [17]. It can be verified by Monte Carlo simulations.

Furthermore, in a multistage converter like pipelined ADCs [18], since the range of the second stage ADC is used over many times, the DNL pattern will repeat many times. In fact, the DNL repeat count will be 2^k where k is the number of bits in the first ADC. This logic is valid for any multistage converter as well as some flash ADCs that may have segmented resistive ladders. If the DNL of each stage is Gaussian distribution, the whole multistage ADC is also with Gaussian distribution.

For *sigma-delta ADC* ($\sum\Delta$ADC) [19], the DNL is likely to be random with a Gaussian distribution owing to its oversampling and the high-pass noise shaping effect.

Although the inherent DNL of the ADC will cause deviations from an ideal Gaussian distribution, it should be at least approximately Gaussian. If the code distribution is significantly non-Gaussian, as exemplified by large and distinct peaks and valleys, for instance — this could indicate either a poorly designed ADC or — more likely — a bad PC board layout, poor grounding techniques, or improper power supply decoupling.

However, DNL is due exclusively to the encoding process and may vary considerably dependent on the ADC encoding architecture. For some ADCs with calibration technique, the DNL may not be random. The error will affect a certain segment of the transfer curve or certain bits in the output code, potentially resulting in a non-ideal transfer curve.

2.2 CDNL with Gain Error

For an ADC with a gain error, the gain error must be calibrated and compensated for firstly. The ideal transfer curve has a slope of 1, $l = 1$. For a gain error of s, the slope is $1+s$. Without jitter, $CDNL_k$ is biased to $k \times s\,LSB$. Similarly, the σ_{CDNL_k} is enlarged by a factor of $1 + s$.

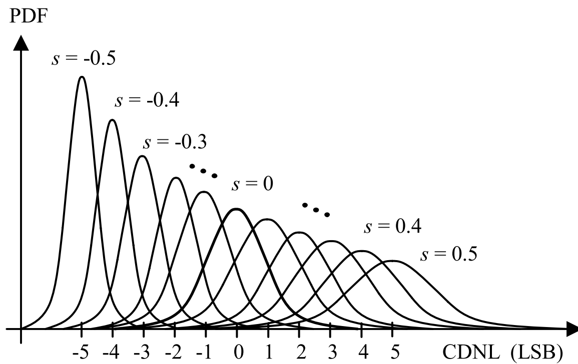


Fig. 2 Distribution functions for s (k=10).

$$\sigma_{CDNL_k} = (1 + s) \cdot \sqrt{k \cdot \sigma_{DNL}^2 + 2\sigma_n^2}. \tag{8}$$

$$\mu_{CDNL_k} = k \times s\, LSB. \tag{9}$$

Therefore, the PDF of $CDNL_k$ has a variance of $(1 + s)^2 \cdot (k \cdot \sigma_{DNL}^2 + 2\sigma_n^2)$ and a mean of $k \times s\, LSB$.

$$f_{sCDNL_k}(x, s) = \frac{1}{\sqrt{2\pi}\,\sqrt{2}(1 + s)\sigma_{CDNL_k}} \cdot e^{-\frac{1}{2}\left(\frac{x-k\cdot s}{\sqrt{2}(1+s)\sigma_{CDNK_k}}\right)^2}. \tag{10}$$

If a $CDNL_k$ histogram has a mean of μ_{CDNL_k} and a standard deviation of σ_{CDNL_k} and σ_n is known, then the gain error and σ_{DNL}^2 are given by

$$s = \mu_{CDNL_k}/k, \tag{11}$$

$$\sigma_{DNL}^2 = \left(\frac{\sigma_{CDNL_k}^2}{(1 + s)^2} - 2\sigma_n^2\right)\Bigg/ k. \tag{12}$$

Figure 2 shows the distribution functions for s from -0.5 to 0.5. For $s > 0$, the transfer curve is steeper, and the output codes have a wider distribution than the input, and vice versa for $s < 0$. Therefore, the histogram, shown in Fig. 2, can be used to determine the gain error (s), the noise and jitter (σ_n).

2.3 Derivative Maximum DNL

For estimation from σ_{DNL} to the maximum DNL, there is a well-known theory. If DNL is the maximum of 2^n independent random variables, its *cumulative distribution function* (CDF) becomes the power of original CDF $F(x)$.

$$F(x) = \frac{1}{2}\left[1 + erf\left(\frac{x - \mu}{\sqrt{2}\sigma_{DNL}}\right)\right]. \tag{13}$$

The PDF is the derivative of CDF. For Gaussian distribution of $\sigma_{DNL} = 1$ LSB. Peaks shift slightly depending on number of bits of ADC as follows: the maximum DNL is roughly 2.7 LSB, 3.1 LSB, and 3.5 LSB, for 8-bit, 10-bit, and 12-bit ADCs.

3. CDNL Test Procedure

The proposed CDNL test procedure comprises the following

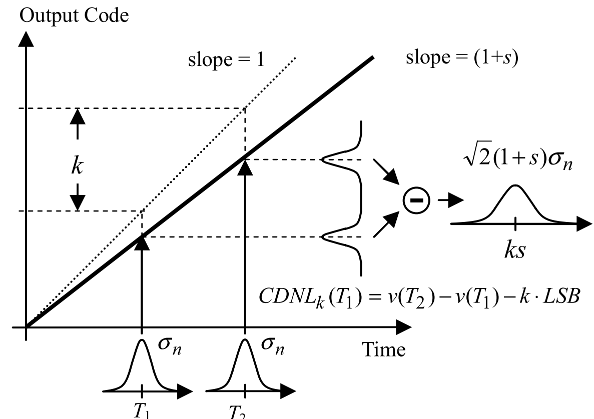


Fig. 3 Transfer curve with a local gain error of s.

five steps.

1. Apply a linear ramp test waveform.
2. Measure and calibrate noise and clock jitter $f_n(x)$.
3. Sample the waveform at a period of k LSBs $T_k = k \times T_{LSB}$.
4. Reconstruct the histogram of $f_{CDNL_k}(x)$.
5. Recover the PDF of the DNL.

Since the simulation by the ramp waveform and recording of the histogram are well defined by the chapter of full-scale triangle wave excitation in IEEE Std. 1057 [1], only the calibration of the noise and jitter are presented below.

The jitter and noise are crucial to ADC testing, in which the LSB is always below the noise level. The SNR must be known to determine the OSR and thus improve the confidence level. The calibration of the noise and jitter ($f_n(x)$) proceeds as follows.

Figure 3 shows a segment of the transfer curve that has a gain error of s. Suppose that the samples are repetitively taken at T_1 and T_2 and the histogram of CDNL for that code interval is recorded. According to (10), the CDNL will have an offset of $k \times s$ and an STD of $(1 + s)\sqrt{2}\sigma_n$. Since k is known, s can be obtained by dividing the offset by k. Then, σ_n is obtained by dividing the STD by $(1 + s)\sqrt{2}$.

The value of σ_n can be accurately obtained by two approaches. First, the number of samples is increased to increase the confidence level. Second, multiple tests can be conducted at various positions on the transfer curve. The final σ_n is the average of the value obtained at various positions. For example, if a total of 10^6 samples are sampled in the first instance, then ten tests can be conducted on 10^5 samples each.

In this study the latter one is preferred for the following reason. The transfer segment in the test interval may not be linear enough or the test interval may cover several transfer segments. A positive DNL shows that the code width is wide, which is called wide code. On the contrary, a negative DNL called narrow code presents the code width is narrow. If the code is wide, the noise measurement will be optimistic because the main bin will contain more hits. If a code is narrow, the noise measurement will tend to be on the

Table 1 Specifications of simulation environment.

Bit Number	12 Bits
Input Signal	$1V_{p\text{-}p}$ Sawtooth (0~1V)
1LSB	0.2442 mV
DNL Specification σ_{DNL}	0, 0.25, 0.5 LSB
Jitter and noise σ_n	1, 2, 4 LSB

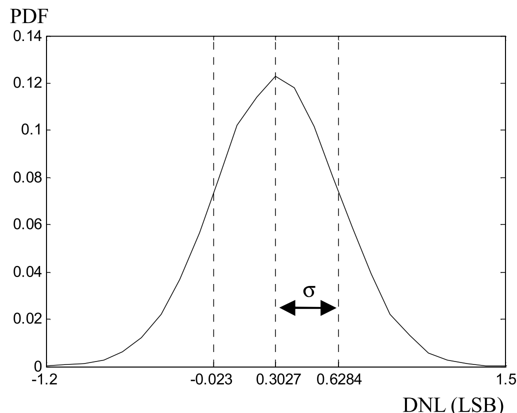
high side. If only one test is performed, then systematic errors will be present in the subsequent tests. The easiest way to circumvent this problem is to compute at several points along the transfer function avoiding major transitions, wide codes, and narrow codes-and then average the results. Multiple segments can be used to obtain the average gain error and the average σ_n.

4. Simulation Results

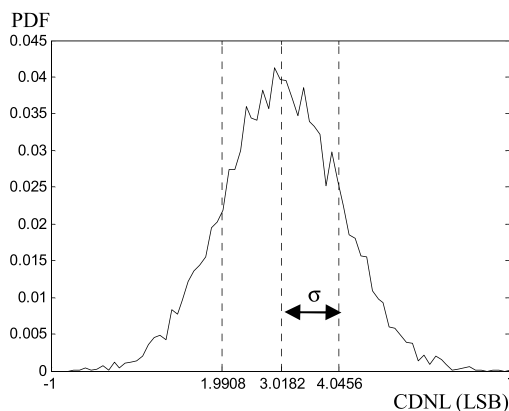
Before the experiment is conducted, a series of simulations are run to verify the concept. Table 1 presents the specifications of the simulation environment. The *device under test* (DUT) is a 12-bit ADC with $\sigma_{DNL} = 0.25\,LSB$ (STD of DNL) and $\sigma_n = 1, 2, 4\,LSB$ (STD of noise and jitter). The simulation results contain four parts. They are DNL and CDNL simulation, CDNL under various σ_n, CDNL under various numbers of sampling points, and CDNL under various value of k.

4.1 DNL and CDNL Simulations

Assume that the DNL of the DUT is Gaussian with $\sigma_{DNL} = 0.25\,LSB$. If the gain error is 0.3, then the slope of the transfer curve $l = 1.3$. According to (8) and (9), $\mu_{DNL} = s = 0.3\,LSB$ and $\sigma'_{DNL} = (1+s)\cdot\sigma_{DNL} = 0.325\,LSB$. Figure 4(a) shows the PDF of the DNL ($k = 1$) without noise or jitter. Figure 4(b) shows the PDF ofσ_{CDNL_10}. With $k = 10$, $\sigma_{CDNL_10} = (1+s)\cdot\sqrt{k}\cdot\sigma_{DNL} = 1.0277\,LSB$ and $\mu_{CDNL_10} = k\times s = 3\,LSB$. The sim ulated $\sigma_{CDNL_10} = 1.0283\,LSB$ has an error of only 0.5%. Figure 4(c) shows the results concerning noise and jitter ($\sigma_n = 2\,LSB$). Theoretically, $\sigma_{CDNL_k} = (1+s)\cdot\sqrt{k\cdot\sigma^2_{DNL} + 2\sigma^2_n} = 3.818\,LSB$. The simulated value is 3.812 LSB, from which $\sigma_{DNL} = 0.245\,LSB$ is obtained, yielding an error of 2% from $\sigma_{DNL} = 0.25\,LSB$, indicating that the proposed CDNL is able to recover σ_{DNL} from σ_{CDNL_k}. Here, the total number of samples in each case is 2^{17}.



(a)



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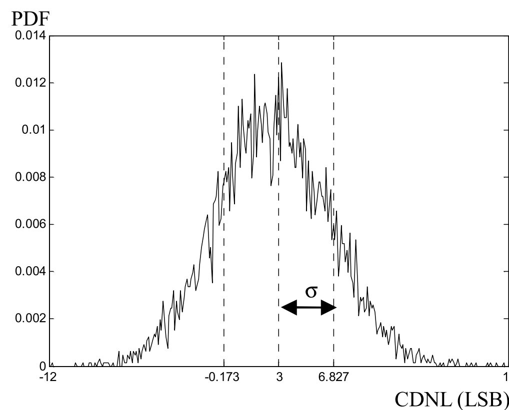


(c)

Fig. 4 (a) PDF of DNL with gain error (s=0.3). (b) PDF of $CDNL_{10}$ without noise or jitter. (c) PDF of $CDNL_{10}$ with noise and jitter.

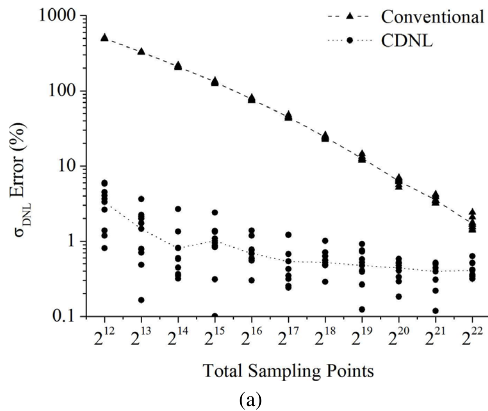
4.2 CDNL Simulations with Various σ_n

The effects of noise and jitter on the proposed CDNL and conventional methods are now simulated. Oversampling and averaging can improve the SNR. However, this will work only if the ADC noise can be approximated as white noise. If the input signal changes randomly from sample to sample, by amounts comparable to the code size (1 LSB), and the input signal has equal probability of being anywhere between two adjacent codes, then the noise can be modeled as approximating white noise. Measure a signal bandlimited to less than one-half the sampling rate, and then oversample that signal with an oversampling ratio (OSR). The resulting samples are then averaged for the resulting output data. For 6 dB of noise reduction, oversample by a factor of four. In this simulation, the injected σ_n values are 1, 2, and 4 LSBs and the total numbers of samples are 2^{17}, 2^{19}, and 2^{21} to meet the requirements of the oversampling theorem.

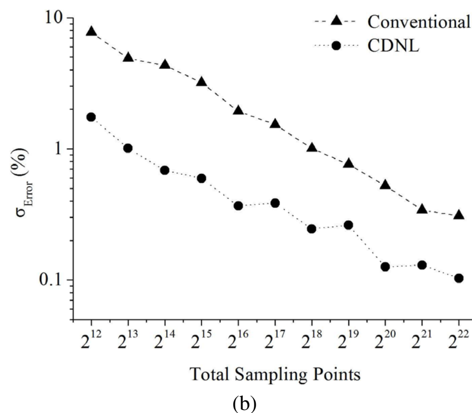
Table 2 presents the simulated results. It also presents the derived σ_{DNL} and the error of the proposed CDNL and

Table 2 Simulations of CDNL and conventional DNL with σ_n. ($\sigma_{DNL}/Error(\%)$)

σ_n	Samples	$\sigma_{DNL} = 0\,LSB$		$\sigma_{DNL} = 0.25\,LSB$		$\sigma_{DNL} = 0.5\,LSB$	
		CDNL	Conventional	CDNL	Conventional	CDNL	Conventional
1 LSB	2^{17}	0.028 / -	0.251 / -	0.248 / 0.72%	0.349 / 39.6%	0.507 / 1.46%	0.547 / 9.46%
2 LSB	2^{19}	0.037 / -	0.253 / -	0.246 / 1.44%	0.359 / 43.8%	0.495 / 0.96%	0.553 / 10.6%
4 LSB	2^{21}	0.056 / -	0.247 / -	0.244 / 2.36%	0.351 / 40.2%	0.511 / 2.16%	0.568 / 13.5%



(a)



(b)

Fig. 5 (a) σ_{DNL} errors with various numbers of samples. (b) σ_{Error} with various numbers of samples.

conventional methods. The proposed CDNL has errors of about 3% while the conventional method is seriously affected by the noise, because in the conventional method, the numbers of samples in each code bin are 32, 128, and 512.

4.3 CDNL Simulation with Various Numbers of Samples

Next, the effect of the number of samples on the accuracy is studied. Figure 5(a) shows the results of the simulation with various numbers of samples. The ADC under test has $\sigma_{DNL} = 0.25\,LSB$ and the jitter that is being injected has $\sigma_n = 1\,LSB$. The conventional method is consistent with the sampling theory. The accuracy is improved roughly 3 dB for every doubling of the oversampling. However, the proposed method has an error of less than 5% in all cases and 2% for 2^{17} samples, because the CDNL can be regarded as a one-bin test. A total of 2^{12} samples for a bin is enough to obtain high accuracy. Here, $DNL = 3 \cdot \sigma_{DNL}$ is assumed. In Fig. 5(a), each case is repeated ten times. Figure 5(b) shows the STD of the errors. The error has an STD less than 2% for 2^{12} samples and 0.3% for 2^{17} samples.

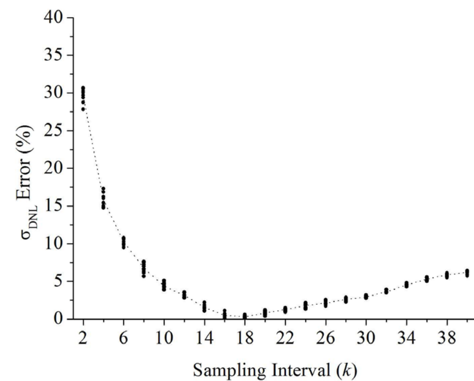


Fig. 6 σ_{DNL} errors as function of k.

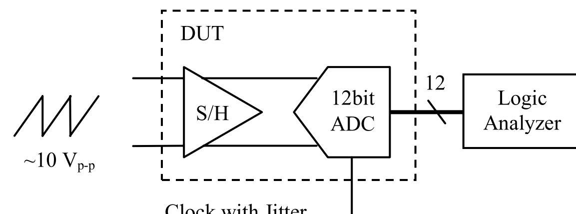


Fig. 7 Schematic diagram of ADC test.

4.4 CDNL Simulation with Various k

Figure 6 shows the measuring error with various CDNL intervals (k). The simulations are based on 2^{20} samples, $\sigma_{DNL} = 0.25\,LSB$, and $\sigma_n = 1\,LSB$. As suggested, for $14 < k < 24$ archives best results with an error less than 3%. For small k, the accuracy is greatly degraded owing to σ_n. For large k, it is known to be inaccurate theoretically.

5. Experimental Results

Not only was a computer simulation conducted, but also a commercial 12-bit ADC was tested. Figure 7 shows a schematic diagram of the test environment, and Fig. 8 shows a photograph. Here, a function generator is utilized to generate a clock with jitter and a logic analyzer for data acquisition. The DUT is AD574A with 10 kHz sampling rate. The period of a input ramp is 409.7 ms.

The first step is to calibrate clock jitter and noise (σ_n). Figure 9 shows σ_n measured at different codes. For each

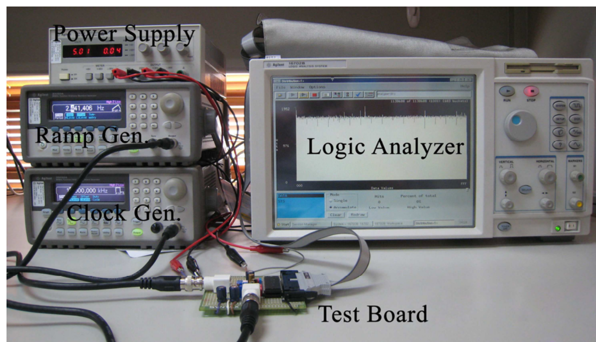


Fig. 8 Equipment for measuring.

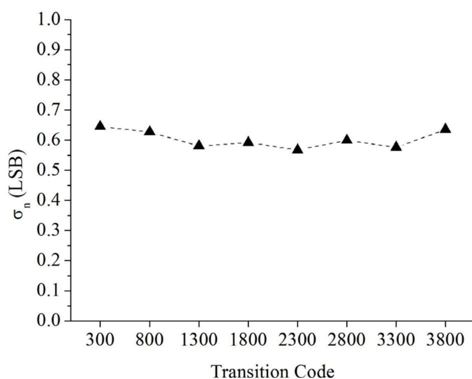


Fig. 9 σ_n at several transition codes.

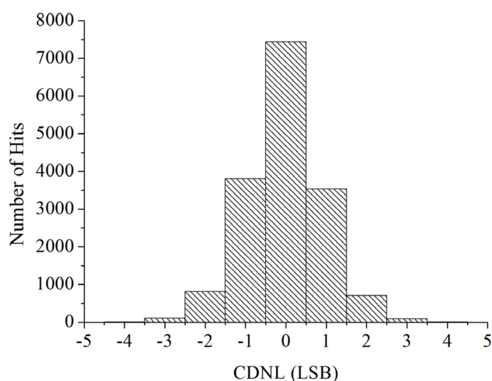


Fig. 10 Histogram of $f_{CDNL_16}(x)$.

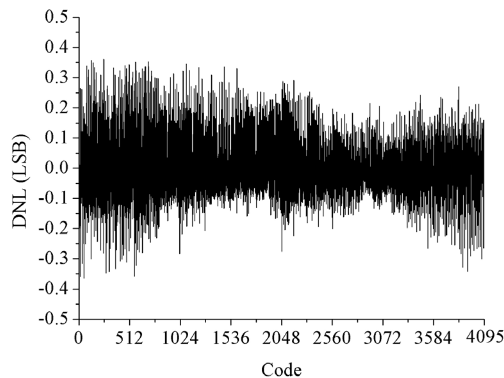


Fig. 11 Conventional measurement of DNL.

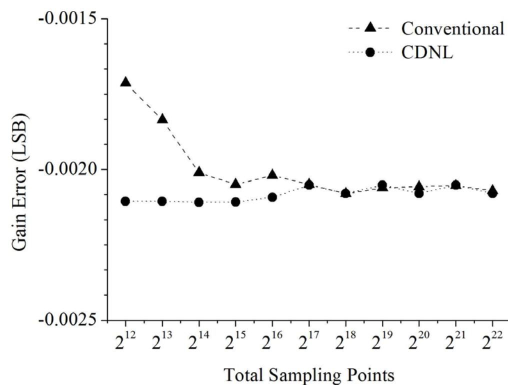


Fig. 12 Comparison of gain error.

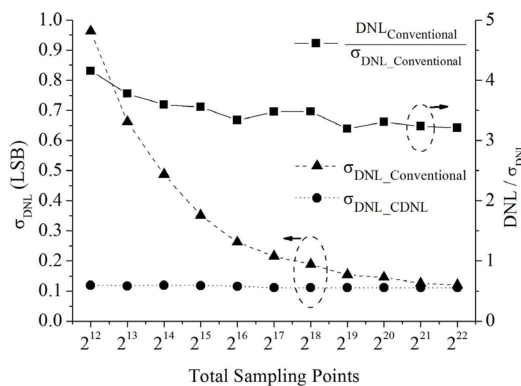


Fig. 13 Comparison of σ_{DNL}.

code, only 1024 samples are taken. The average σ_n is 0.60285 LSB.

Since $14 < k < 24$ was recommended above, k is set to 16 for the CDNL test. Figure 10 shows the histogram of f_{CDNL_16} for a total of 2^{14} samples, which implies that $\mu_{CDNL_16} = -0.0337\,LSB$ and $\sigma_{CDNL_16} = 0.9673\,LSB$.

Therefore, $s = \mu_{CDNL_16}/k = -0.00211\,LSB$, and σ_{DNL} $= \sqrt{\left(\frac{\sigma^2_{CDNL_16}}{(1+s)^2} - 2\sigma^2_n\right)\Big/16} = 0.1153\,LSB$.

For comparison, a conventional DNL test is conducted. Figure 11 shows the measured results made with 2^{22} samples. The gain error is $-0.00208LSB$ and σ_{DNL} = $0.1199\,LSB$. The maximal DNL is 0.3657 *LSB*, which is roughly $3\sigma_{DNL}$.

To compare thoroughly the proposed CDNL and the conventional DNL, measurements of the ADC were made with various numbers of sampling points. Figure 12 shows the comparison of gain errors. The proposed method achieves higher accuracy with fewer samples.

Figure 13 shows the comparison of σ_{DNL} values. It also plots the ratio of maximal DNL to σ_{DNL} using the conventional method. A total of 2^{12} samples with the proposed method yields the same accuracy as is achieved using more than 2^{22} samples with the conventional method. As that the suggestion is made based on the conventional method, the

Table 3 Efficiency & results comparison. (σ_n=0.6 LSB)

	Conventional Test	Proposed Test
Number of samples	4,194,304	4096 (+ 1024*8 for calibration)
Number of code bins	4,096	16
σ_{DNL}	0.1199 LSB	0.1153 LSB
Maximum DNL	0.3657 LSB	0.3689 LSB

maximal DNL is roughly $3.2 \times \sigma_{DNL}$ for 2^{22} samples. The test cost is significant reduce. It only needs 16 registers, with confidence level of $\pm 5\sigma$, to store code bins in this experiment. Table 3 briefly gives a comparison of the proposed and the conventional methods.

The proposed method is a practical linearity test for BIST. The total performance may be verified with additional dynamic test such as THD.

6. Conclusions

This work proposed a *cumulative DNL* (CDNL) testing method for the BIST of ADCs. Instead of checking every code bin (2^n bins), two randomly selected codes that are separated by k LSBs are sampled. The histogram of code differences is used to derive the DNL and gain error. A noise and jitter calibration mechanism was also proposed. A computer simulation was conducted and measurement of a commercial 12-bit ADC was made. The results show that our method can achieve an error of less than 5% for 2^{12} samples, which can only be achieved by using more than 2^{22} samples with the conventional method. Furthermore, the proposed CDNL method requires significantly fewer bins — roughly ten — than the conventional method, which requires 2^n bins. With a short test time and a small number of bins, the proposed CDNL is suitable for use in the BIST of ADCs.

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