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Ge technology beyond Si CMOS

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Abstract. To save energy, low voltage operation is the most important criterion for CMOS ICs. To reach this goal, high mobility new channel materials are required for CMOS ICs at ≤14 nm technology nodes. The high electron mobility InGaAs nMOSFET and high hole mobility Ge pMOSFET were proposed for CMOS at 0.5 V operation, since the poor hole mobility of InGaAs makes it unsuitable for all InGaAs CMOS. However, the epitaxial InGaAs nMOSFET on Si faces fundamental material challenges with large defects and high leakage current. Although dislocation-defects-free Ge-on-Insulator (GeOI), ultra-thin-body (UTB) InGaAs IIIV-on-Insulator (IIIVOI), and selective GeOI on Si were pioneered by us, it is still difficult to reach InGaAs-nMOS/Ge-pMOS CMOS targeting to ≤14 nm CMOS. In contrast, Ge is the ideal candidate for all Ge CMOS logic due to both higher electron and hole mobility than Si. Significantly higher (2.6X) hole mobility of GeOI pMOSFET than universal SiO_2/Si value was reached at a medium 0.5 MV/cm effective electric field (E_{eff}) and 1.4 nm equivalent-oxide-thickness (EOT). Nevertheless, the Ge nMOSFET suffers from large EOT and fast mobility degradation with increasing E_{eff}, due to the surface Fermi-level pinning to valance band, poor high-κ/Ge interface and low dopant activation. Using novel laser annealing and proper gate stack, small EOT of 0.95 nm, small sub-threshold swing of 106 mV/dec, and 40% better high-field mobility than universal SiO_2/Si data were achieved in Ge nMOSFET. Such all-Ge CMOS has irreplaceable merits of much simpler process, lower cost, and potentially higher yield than the InGaAs-nMOS/Ge-pMOS CMOS platform.

1. Introduction

The IC chips consume a large portion of energy globally and will increase more in the near future. Therefore, low voltage CMOS must be developed to lower the energy and power consumption, according to fundamental physics of $P=C_{load}V_D^2f$, where the C_{load}, V_D, and f are the load capacitance, driven voltage, and operation frequency of an IC. To maintain high performance operation at a low voltage, high mobility new channel materials are necessary for CMOS IC at ≤14 nm technology nodes. Thus, high electron mobility InGaAs nMOSFET and high hole mobility Ge pMOSFET were proposed for ≤14 nm CMOS at 0.5 V operation, which can lower the AC switching power as much as 50% from the current 0.7 V V_D bias used for 22 nm CMOS ICs. However, the integration of InGaAs on Si faces fundamental material challenges: the large 8% lattice-mismatch, high dislocation densities, and anti-phase domain boundaries by polar-nonpolar mismatched lattice. These defects further lead to high leakage current in epitaxial grown InGaAs nMOSFET on Si substrate. Although the device improves with increasing the buffer layer thickness, this will cause the integration of InGaAs nMOSFET with bottom Si devices more difficult.

To address these epitaxial growth issues, dislocation-defects free Ge and InGaAs on Si were demonstrated by us using the Ge-on-Insulator (GeOI) [1]-[2], ultra-thin-body (UTB) InGaAs IIIV-on-Insulator (IIIVOI) [3]-[4], and selective GeOI on Si [5] using the wafer bonding, smart-cut, or selective etching method. Alternatively, Ge has higher electron (3X) and hole (4X) mobility than Si that is the ideal candidate for all Ge CMOS logic. This is quite different to the InGaAs case, where the poor hole mobility prevents to form all InGaAs CMOS. This all-Ge CMOS approach is much simpler than the CMOS platform of InGaAs nMOSFET and Ge pMOSFET, which has unique merits of smaller numbers of mark, simpler process step, lower cost, and potentially higher yield. However, the Ge nMOSFET suffers from large equivalent-oxide-thickness (EOT) and fast mobility degradation with increasing oxide effective electric field (E_{eff}), which are related to the surface Fermi-level pinning to valance band, poor high-κ/Ge interface and low dopant activation. In this paper, we will discuss the potential to use GeOI, IIIVOI, selective GeOI, and the progress of all Ge CMOS.

2. Experiments

The Ge/SiO_2/Si GeOI was formed by first depositing SiO_2 on both Ge and Si wafers using PECVD, O_2 plasma treatment to top SiO_2, bonding Ge/SiO_2 and SiO_2/Si at 500°C, etching back and polishing the Ge [1]. Figure 1 show the fabricated GeOI without and with O_2 plasma treatment. Void-free Ge/SiO_2-SiO_2/Si interface with improved mechanical strength was reached by using O_2 plasma treatment at such low temperature. Dislocation-free Ge is obtained and the smooth Ge/SiO_2 interface allows further thinning down the body thickness.

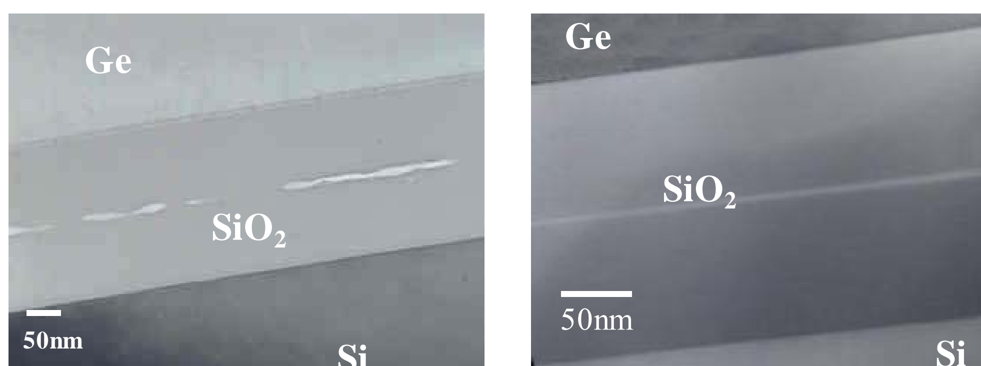

Figure 1. Cross-sectional TEM of low-temperature bonded GeOI without (left) and with (right) O_2 plasma treatment before bonding.

We further fabricated the selective GeOI [5]. As shown in Figure 2, the selective GeOI was formed by SiO_2 deposition on both H^+-implanted Ge and standard 1-Poly Si-6-Metal (1P6M) 0.18μm MOSFETs, O_2 plasma enhanced bonding, smart-cut, followed by 400°C annealing and slight polishing.

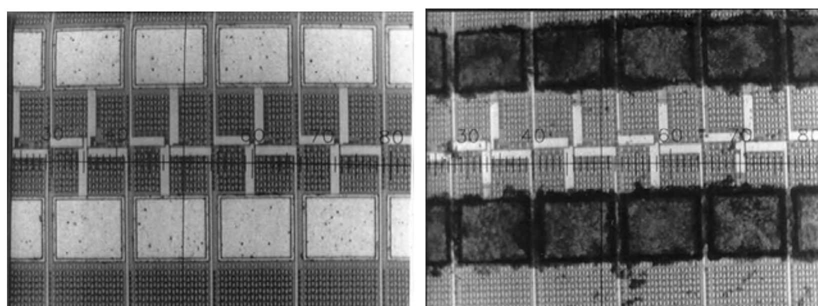

Figure 2. Top view of selective GeOI on 1P6M 0.18μm CMOS before (left) and after (right) bonding.

We also extended the GeOI to wider semiconductor-on-Insulator (SemiOI). Figure 3 shows the fabricated InAlAs/InGaAs IIIVOI [3]-[4]. An inverted InAlAs/InGaAs/InAlAs HEMT hetero-structure was first grown on InP substrate, followed by PECVD SiO_2 deposition, applying O_2 plasma treatment to top SiO_2/InAlAs/InGaAs/InAlAs/n^+-InGaAs/InAlAs/InP and SiO_2/Si, bonding at 400°C, and selective etching the InP substrate and InAlAs buffer layer. Such low temperature bonding process was developed to decrease the thermal mismatch among III-V, SiO_2 and Si materials.

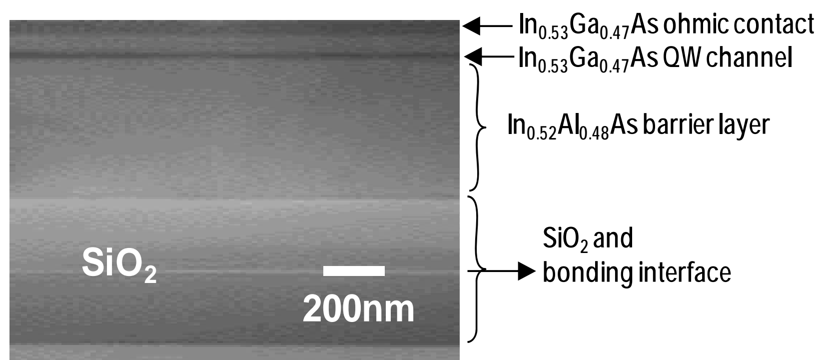

Figure 3. Cross-sectional TEM of InAlAs/InGaAs/InAlAs FET structure.

After GeOI or selective GeOI fabrication, the pMOSFET were made by high-κ $LaAlO_3$ gate dielectric and high work-function IrO_2 metal-gate formation, self-aligned source-drain B^+ implantation, and dopant activation at 500°C. The InAlAs/InGaAs IIIVOI FET was formed by gate-recess etching the top n^+ InGaAs contact layer, Ti/Au Schottky gate lift-off, and NiGeAu source-drain contacts [3].

For high performance Ge nMOSFET, a gate-last process was used. To improve the high-κ/Ge interface, an ultra-thin interfacial SiO_2 [6] and KrF laser annealing (248 nm, ~30 ns pulse) [7]-[8] were applied. The laser annealing was also used to increase the dopant activation of P^+-implanted source-drain. The gate dielectric is composited with ~0.8 nm SiO_2, 1 nm La_2O_3 and 3 nm ZrO_2, followed by 400°C furnace annealing. Then ultra-fast laser annealing was applied to prevent the Ge out-diffusion into high-κ gate dielectric [6]. The Ge nMOSFETs were made by patterning the deposited TaN gate and Al source-drain contact metal.

3. Results and discussion

3.1. Defect-free SemiOI transistors

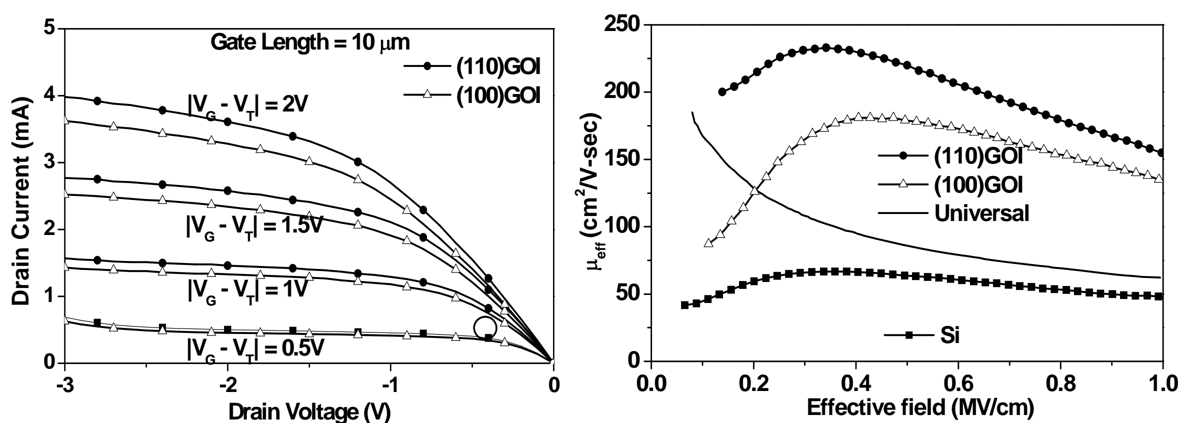

Figure 4. I_d-V_d (left) and mobility-E_{eff} (right) characteristics of IrO_2/$LaAlO_3$/GeOI pMOSFETs.

Figure 4 shows the I_d-V_d and mobility data of $IrO_2/LaAlO_3$/GeOI pMOSFETs. In addition to the good transistor characteristics, the metal-gate/high-κ/GeOI pMOSFET at (110)-orientation has 2.6X higher hole mobility than universal SiO_2/Si mobility, at a medium 0.5 MV/cm E_{eff} and a 1.4 nm EOT. The bonding top layer with different orientation to bottom substrate is the advantage of SemiOI technology.

The device I_d -V_d and gain-frequency characteristics of InAlAs/InGaAs IIIVOI nFETs are shown in Figure 5. A high drive current of 0.41 mA/μm was obtained for this nFET with a 1.1 μm gate length. The good device performance is evident from the high RF current gain ($|H_{21}|^2$) and cut-off-frequency (f_t) of 21 GHz that are close to those of a 0.35μm Si MOSFET with much smaller gate length. The better transistor performance is due to the significantly higher mobility of 8,100cm^2/Vs than that for a Si MOSFET.

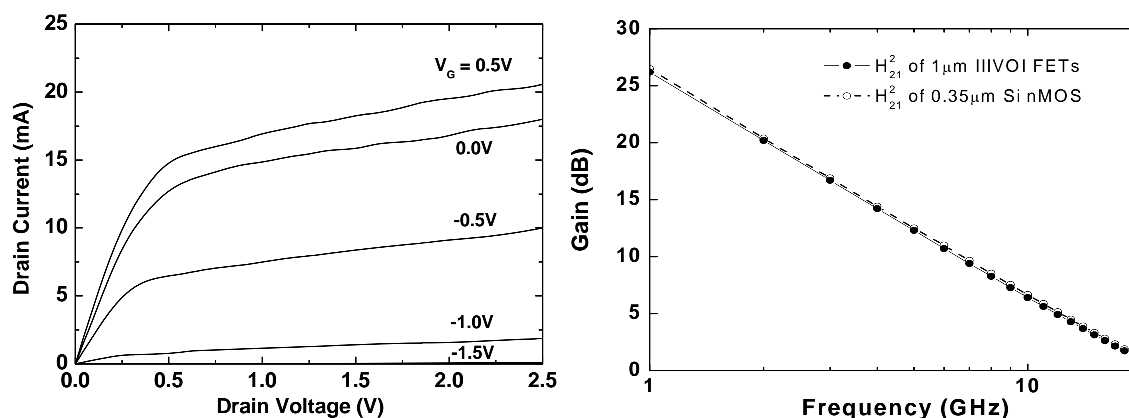

Figure 5. I_d-V_d (left) and gain-frequency (right) characteristics of Au/Ti/InAlAs/InGaAs/IIIVOI nFETs.

It is important to notice that although the selective wafer-bonding on 50-μm×50-μm area was obtained, this technique is still different to reach both the IIIVOI and GOI side-by-side for high mobility InGaAs-nMOS/Ge-pMOS CMOS platform. The low hole mobility makes InGaAs unsuitable for all-InGaAs CMOS. The epitaxial InGaAs nMOSFET on Si is still quite challenging due to the large defects density and high transistor leakage current.

3.2. High mobility Ge nMOSFET for all-Ge CMOS

The Ge has both higher electron and hole mobility than Si - an ideal candidate for all Ge CMOS logic. The GeOI pMOSFET shown in Figure 4 has much higher hole mobility than universal SiO_2/Si mobility at a small 1.4 nm EOT. However, Ge nMOSFET suffers from poor device performance due to surface Fermi-level pinning to valance band, low dopant activation, and poor high-κ/Ge interface. To address these issues, novel laser annealing with fast ~30 ns pulse was used [7]-[9]. The laser annealing melts surface semiconductor and re-crystallize within a very short time, which can fully activate the ion-implanted dopants and form ultra-shallow junction. Such laser annealing was proposed for highly scaled ≤14 nm CMOS to reach both ultra-shallow junction and low series resistance. We pioneered the use of laser annealing on high-κ gate dielectric [7]. Figure 6 shows the device characteristics of $TaN/ZrO_2/La_2O_3/SiO_2$/Ge MOS capacitors and nMOSFETs. Applying laser annealing on gate dielectric not only improves the C-V hysteresis but also increases the gate capacitance. The higher gate capacitance is attributed to the fast ~30 ns annealing with less high-κ/Ge interface reaction, which gives a small EOT of 0.95 nm from quantum-mechanical C-V simulation. From the measured transistor I_d-V_g characteristics, a small sub-threshold swing of 106 mV/dec was obtained that is consistent with the improved C-V hysteresis. Figure 7 shows the mobility-E_{eff} characteristics, after gate leakage correction [10]. At 1 MV/cm E_{eff}, 40% better high-field mobility than universal SiO_2/Si data was achieved in Ge nMOSFET. These results suggest the fast electron mobility degradation is not intrinsic to Ge nMOSFET.

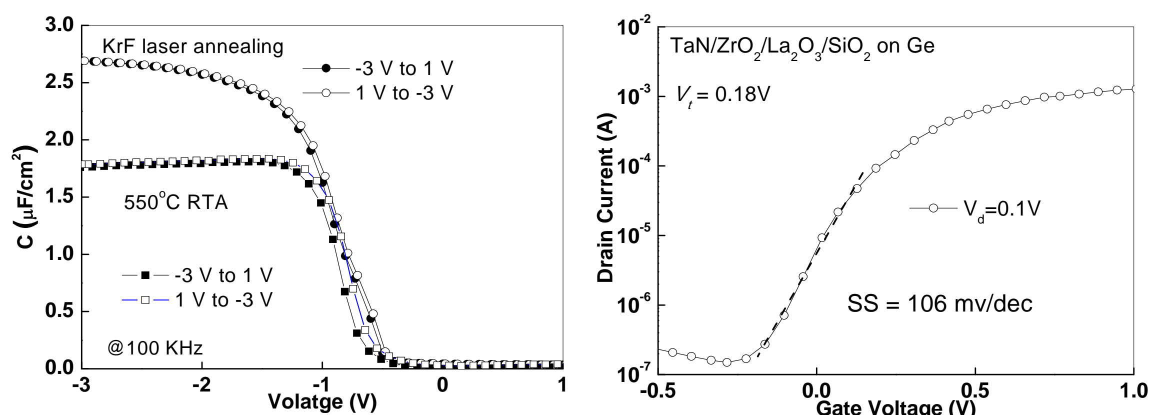

Figure 6. Capacitor C-V (left) and transistor I_d-V_g (right) characteristics of $TaN/ZrO_2/La_2O_3/SiO_2/Ge$ nMOSFETs by laser annealing.

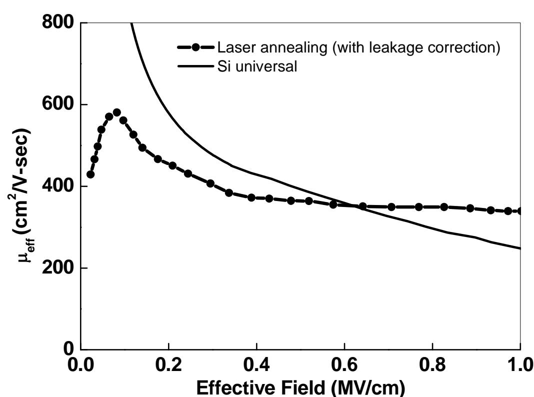

Figure 7. Mobility-E_{eff} characteristics of $TaN/ZrO_2/La_2O_3/SiO_2/Ge$ nMOSFET by laser annealing.

4. Conclusions

High mobility new channel materials are required at ≤14 nm CMOS, but the InGaAs/Si nMOSFET is still very challenging due to fundamental material issues with large defects and high leakage current. Although dislocation-defects-free InGaAs-IIIVOI, GeOI, and selective GeOI were developed, it is still difficult to reach InGaAs-nMOS/Ge-pMOS CMOS side-by-side with nm-scale dimension for ≤14 nm CMOS. In contrast, the GeOI pMOSFET shows 2.6X higher hole mobility than universal SiO_2/Si data at a medium 0.5 MV/cm E_{eff} and 1.4 nm EOT. Using novel laser annealing and proper gate stack on Ge nMOSFET, small 0.95 nm EOT and 40% better 1-MV/cm mobility than universal SiO_2/Si data were achieved. Although further device performance improvement on Ge nMOSFET is required, the fast mobility degradation with increasing E_{eff} is not an intrinsic limitation to Ge nMOSFET. The all-Ge CMOS has irreplaceable merits of much simpler process, lower cost, and potentially higher yield than the InGaAs-nMOS/Ge-pMOS CMOS platform.

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