PAPER

The Design of a *K*-Band 0.8-V 9.2-mW Phase-Locked Loop

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SUMMARY A 0.8-V CMOS Phase-Locked Loop (PLL) has been designed and fabricated by using a 0.13-μm 1p8m CMOS process. In the proposed PLL, the double-positive-feedbacks voltage-controlled oscillator (DPF-VCO) is used to generate current signals for the coupling current-mode injection-locked frequency divider (CCMILFD) and current-injection current-mode logic (CICML) divider. A short-pulsed-reset phase frequency detector (SPR-PFD) with the reduced pulse width of reset signal to improve the linear range of the PFD and a complementary-type charge pump to eliminate the current path delay are also adopted in the proposed PLL. The measured in-band phase noise of the fabricated PLL is −98 dBc/Hz. The locking range of the PLL is from 22.6 GHz to 23.3 GHz and the reference spur level is −69 dBm that is 54 dB bellow the carrier. The power consumption is 9.2 mW under a 0.8-V power supply. The proposed PLL has the advantages of low phase noise, low reference spur, and low power dissipation at low voltage operation.

key words: *phase-locked loop (PLL), VCO, coupling current-mode injection-locked frequency divider (CCMILFD), SPR-PFD, complementary-type charge pump*

1. Introduction

The phase-locked loop (PLL) is a key building block in radio-frequency (RF) systems, and generates the carrier signal to convert the data up or down to the desired frequency band. Nowadays, research effort has been made to develop RF systems in an advanced CMOS technology so that RF circuits can be integrated with digital circuitry in a System-On-a-Chip (SoC) design. As CMOS technology is scaling down to the nanometer, the supply voltage is also lowered. It is therefore highly desirable to implement a PLL that can operate at a high frequency beyond 10 GHz from a supply voltage as low as sub-1 V. Recently, PLLs in the frequency range of 10–24 GHz have been proposed in [1]–[5] with supply voltages of 1 V or above 1 V.

The challenges in implementing a low-voltage RF PLL are on the design of voltage-controlled oscillator (VCO) and frequency dividers. For VCOs, low phase noise is required most importantly to avoid corrupting signals in RF systems. However, low supply voltage would limit the signal swing and reduce the negative resistance in the VCO. Besides VCOs, low-voltage, high-frequency, and wide-locking-range frequency dividers are also necessary in designing a low-voltage PLL to ensure the correct frequency division. In the conventional current-mode-logic (CML) type frequency dividers, low supply voltage results in insufficient voltage headroom for internal nodes and thus makes the circuit fail when operated at high frequencies [6].

To avoid the above design problems, both DPF-VCO with current-mode outputs and current-mode frequency dividers are adopted in the proposed *K*-band current-mode PLL design. In this design, a high-frequency phase frequency detector (PFD) which generates a short-pulse reset signal to enhance the linear range of the PFD is also proposed. Wide linear range can improve the locking behavior of the PLL. In addition, with a high-operating-frequency PFD, the higher reference frequency can be chosen. The lock time of the PLL can be decreased and the reference spur can be pushed further away from the desired frequency band. Under sub-1 V supply voltage, a complementary-type charge pump (CP) that can be operated at 0.8-V supply voltage to reduce the ripple of tuning voltage is also proposed. It helps to reduce the voltage ripple of the tuning voltage of VCO and suppress the reference spur.

The proposed current-mode PLL is measured at 23.2 GHz with the in-band phase noise of −98 dBc/Hz. The total dc current consumption is 11.5 mA, 5.2 mA in VCO and CCMILFD and 6.3 mA in the rest of circuits under a 0.8-V power supply. The reference spur level is −69 dBm, which is 54 dB below the carrier. By using the current-mode technique in the PLL, the supply voltage and power consumption can be lowered significantly while keeping good performance of phase noise and reference spur.

This paper is organized as follows. In Sect. 2, the proposed 24-GHz CMOS PLL architecture and the detailed circuit implementation are presented. In Sect. 3, the measurement results of the fabricated PLL are demonstrated. Finally, the conclusion is given in Sect. 4.

2. Circuit Realization of Phase-Locked Loop

In this paper, a low-voltage and low-power *K*-band PLL with current-mode techniques is designed. The block diagram is shown in Fig. 1. The loop is composed of a DPF-VCO, a divide-by-2 CCMILFD [7], a divide-by-2 CICML divider [7], a divide-by-8 CML frequency divider, a phase-frequency detector (PFD), a complementary-type charge pump, and a loop filter. This is a third-order system with a second-order loop filter. The higher reference clock frequency of 750 MHz in simulation is chosen. For the purpose of measurement, two open-drain output buffers

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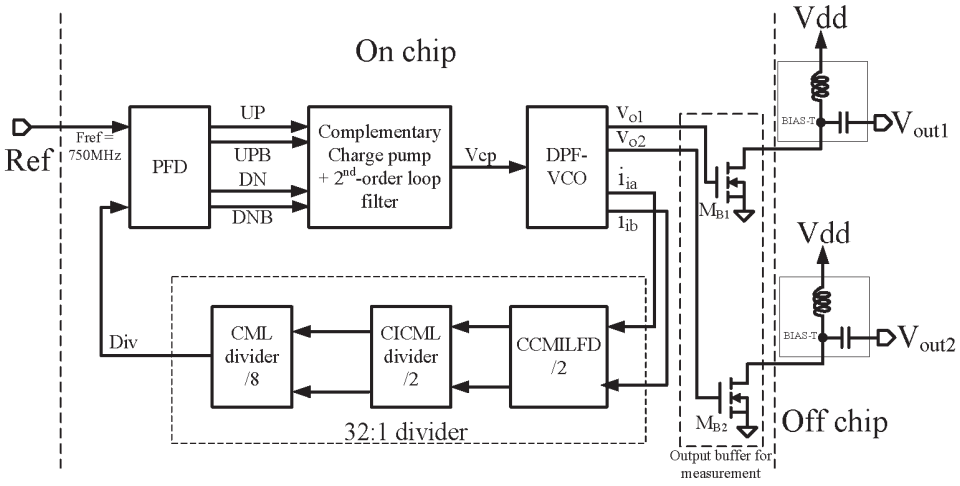

Fig. 1 Block diagram of the proposed *K*-band current-mode PLL.

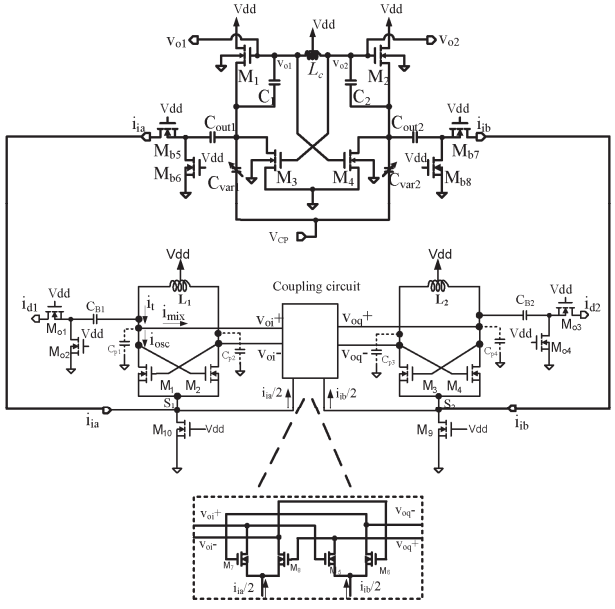

Fig. 2 The circuit diagram of DPF-VCO and CCMILFD.

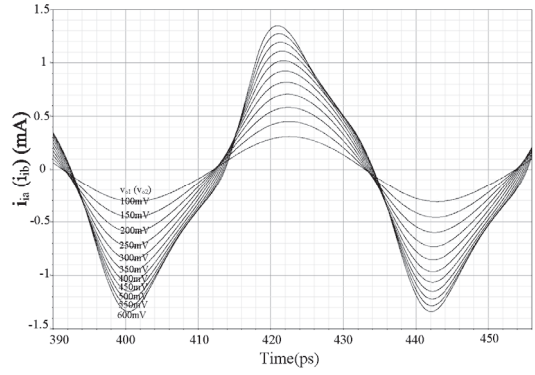

Fig. 3 The simulated current output of VCO versus voltage swing from 100 mV to 600 mV at resonant network by Spectre RF.

M_{B1} and M_{B2} are used. The detailed circuit operations of all building blocks are discussed in the following subsections.

2.1 DPF-VCO and CCMILFD

The circuit diagram of the DPF-VCO and high frequency current-mode frequency divider is shown in Fig. 2. In the DPF-VCO, two Colpitts structures and one NMOS cross-coupled pair core are used. As shown in Fig. 2, (M_1, C_1, C_{var1}) and (M_2, C_2, C_{var2}) are the two Colpitts structures to form the first positive feedback loop. (M_3, M_4) is the NMOS cross-coupled pair to provide the second positive feedback loop. A center-tapped inductor L_C is used in this circuit with the inductance of 0.48 nH and the quality factor of 17. The resonant frequency of the VCO is determined by the LC tank of (L_C, $C_{1,2}$, $C_{var1,var2}$). The voltage V_{cp} is controlled by the charge pump circuit to tune the output frequency of DPF-VCO.

For the current-mode frequency dividers CCMILFD [7], input current signals are taken from VCO. When the VCO starts to oscillate, the voltage signals v_{o1} and v_{o2} at the gates of M_1 (M_4) and M_2 (M_3) become differential signals and hence the currents can be generated and sent to the CCMILFD through two current-mode output buffer stages which are composed of (M_{b5}, M_{b6}, and C_{out1}) and (M_{b7}, M_{b8}, and C_{out2}). C_{out1} and C_{out2} are large dc blocking capacitors and can be viewed as a low-impedance path for high-frequency signals. $M_{b5,7}$ are common-gate (CG) amplifier with low-impedance path and $M_{b6,8}$ are the current sources for the CG amplifiers. The simulated output current i_{ia} (i_{ib}) versus the voltage signal v_{o1} (v_{o2}) by Spectre RF is shown in Fig. 3. With the increasing voltage swing of v_{o1} (v_{o2}) from 100 mV to 600 mV, the output current i_{ia} (i_{ib}) is increased from 0.33 mA to 1.3 mA.

Though, in this design, the outputs of the DPF-VCO are not from the LC tank, the overall phase noise which is contributed by the parasitic resistor of LC-tank and active elements can also be characterized by using the theory in [8], [9]. Since the output signal in the proposed circuit is

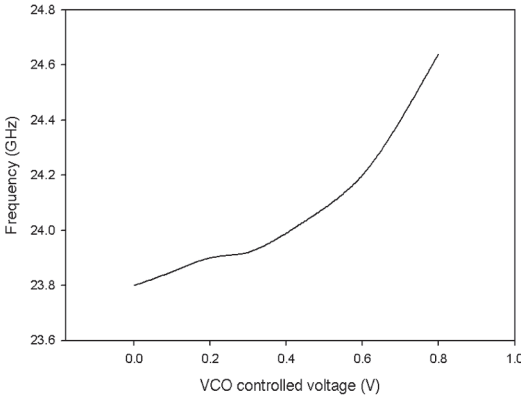

Fig. 4 The simulated tuning range of VCO by Spectre RF.

taken from the node between the capacitors $C_{1,2}$ and $C_{var1,2}$, the noise-to-signal ratio can be expressed as

$$\frac{N_{out}}{S_{out}} \equiv \frac{\overline{(V_{n\_out})^2}}{\left(V_{sig\_out}\right)^2} = \frac{\overline{(V_{n\_LC}\cdot\eta)^2}}{\left(V_{sig\_LC}\cdot\eta\right)^2} = \frac{\overline{(V_{n\_LC})^2}}{\left(V_{sig\_LC}\right)^2}\frac{N_{LC}}{S_{LC}} \quad (1)$$

where $\eta \equiv C_{1,2}/(C_{1,2} + C_{var1,2})$ and (N_{LC}/S_{LC}) is the noise-to-signal ratio at LC tank. The simulated phase noise at 1-MHz offset frequency is −105 dBc/Hz.

The tuning range of center frequency is varied from 23.8 GHz to 24.6 GHz as the tuning voltage of VCO is varied from 0 to 0.8 V. The simulated result by Spectre-RF is shown in Fig. 4.

2.2 Phase-Frequency Detector (PFD)

In order to increase the linear range of the PFD, a technique of early reset mechanism to generate a short pulse of reset signal is proposed. The circuit diagram of the PFD is shown in the Fig. 5. M_{UP1}-M_{UP6} and M_{DN1}-M_{DN6} form the true single phase clock (TSPC) pre-charged D-FF. The non-inverting delay stages $Delay\_cell_1$ and $Delay\_cell_2$ are inserted into the commonly used pre-charged D-FF to extend the linear range [10]. The early-reset circuits are composed of (M_{UP7}, M_{UP8}) and (M_{DN7}, M_{DN8}). They are controlled by the Pre_reset signal to reset the output of the PFD.

The timing diagram of SPR-PFD is presented in Fig. 6. t_{d1} is the inserted delay between Ref and Ref_delay through the $Delay\_cell_1$. t_{d2} is the minimum time requirement for the next Ref_delay signal that the next Ref can be detected after the falling edge of Reset. t_{d3} and t_{pd3} are the delay times of Reset and Pre_reset signal after Div is "Hi", respectively. t_{rst} is the pulse period of Reset signal without the early reset mechanism and t_{prst} is the new pulse period with early reset mechanism. At the first rise of Div, the phase difference $\Delta\Phi$ between two inputs is in the range of $2\pi - \Delta < \Delta\Phi < 2\pi - \delta$, where the δ is given by $\delta = 2\pi \cdot t_{d3}/t_{ref}$ [11]. With the early-reset mechanism, the Δ and δ in this design are overwritten as

$$\Delta = 2\pi \cdot \left(t_{prst}/t_{ref}\right) \quad (2)$$

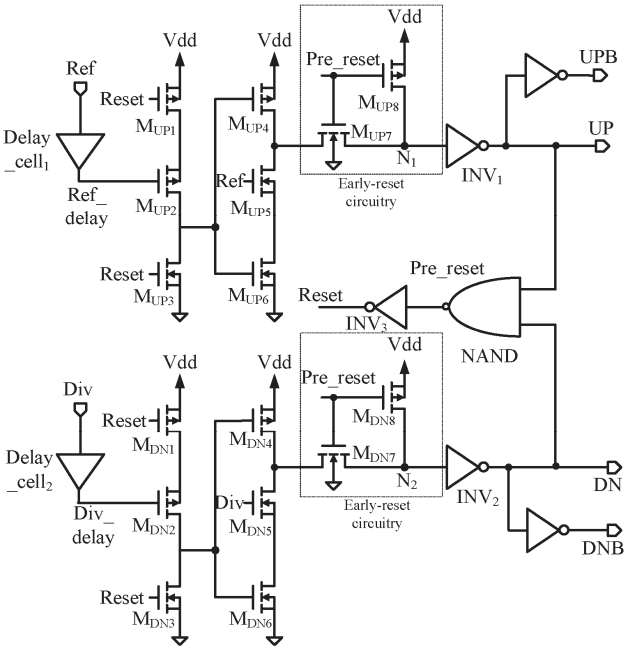

Fig. 5 The proposed circuit diagram of SPR-PFD.

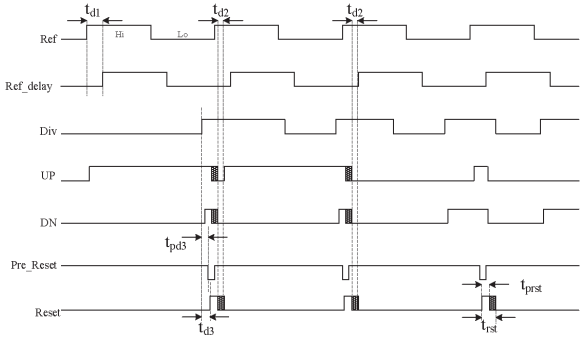

Fig. 6 The timing diagram of SPR-PFD.

$$\delta = 2\pi \cdot \left(t_{pd3}/t_{ref}\right) \quad (3)$$

As the UP and DN are "Hi", the Pre_reset is activated to block the path from the D-FF and pull up the nodes N_1 and N_2 immediately and the UP and DN signals are forced to be "Lo" quickly. Subsequently, the Reset is forced to go down and pulse width is shortened. When the time period from the falling edge of Reset to the rising edge of Ref_delay is greater than t_{d2}, the next Ref can be detected. Therefore, with the shorter pulse period of Reset, a wider detectable range for two inputs can be obtained even when the phase difference between the two input signals is very close to 2π.

In this design, from the simulation results as shown in Fig. 7, with the frequency of Ref of 750 MHz, the Δ is equal to 0.42π and t_{prst} is around 180 ps. Compared to the version without early-reset mechanism, when frequency of Ref signal is increased, the linear range of the PFD with early-reset circuit can be much better than without early-reset circuit.

2.3 Complementary-Type Charge-pump and Loop Filter

In the designed PLL, to make the circuit operate at a low voltage of 0.8 V, the current-steering charge pump is considered and a complementary-type charge pump is proposed and depicted in Fig. 8. The differential pairs of NMOS transistors (M_1, M_2) and PMOS transistors (M_{B1}, M_{B2}) are controlled by the (DN, UP) and (UPB, DNB) signals, respectively. The (UP, DN) and (UPB, DNB) signals switch the differential pairs instead of controlling switches on the output current path directly to prevent the glitches at the output node.

With the lock of the PLL, the I_{U1} and I_{D1} are generated by the short pulses of UP and DN which are designed to eliminate the dead-zone effect of the PFD. The asymmetrical current paths for I_{U1} and I_{D1} cause a noise source to the control voltage of VCO even when the loop is locked. It results in poor phase noise and higher reference spur of the PLL. In order to minimize this effect, the complementary part that is controlled by DNB and UPB is used.

The I_{UP} is summed by two currents I_{U1} and I_{U2} that are controlled by UP and UPB while the I_{DN} is generated by combining two currents I_{D1} and I_{D2}. The amplitude for the I_{UP} and I_{DN} can be expressed as

$$|I_{UP}| = |I_{U1}| + |I_{U2}| = |I_{D1}| + |I_{D2}| = |I_{DN}| \quad (4)$$

With the complementary current signals, I_{U1} and I_{D2} are mirrored once and I_{U2} and I_{D1} are mirrored twice to the output path, respectively. Therefore, the phase of I_{U1} is equal to the phase of I_{D2} and the phase of I_{U2} is equal to the phase of I_{D1}, The relationship between phases can be shown in (5) and (6).

$$\angle I_{U1} = \angle I_{D2} \quad (5)$$

$$\angle I_{U2} = \angle I_{D1} \quad (6)$$

Since the signal paths for I_{UP} and I_{DN} are the same in both amplitude and phase, the error charge to the loop filter can be minimized and the variation of V_{CP} can be reduced to improve the reference spur performance of VCO. From the simulation results in Fig. 9, the currents I_{UP} and I_{DN} can be more balanced and the error current can also be minimized. The V_{CP} ripple after the loop filter which has only 6-pF capacitance is also minimized to about 6 mV.

3. Experimental Results

The proposed *K*-band current-mode PLL was fabricated in

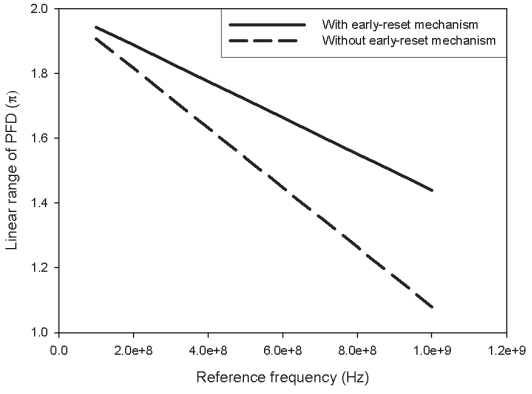

Fig. 7 The simulated linear range of the PFD with and without early-reset mechanism.

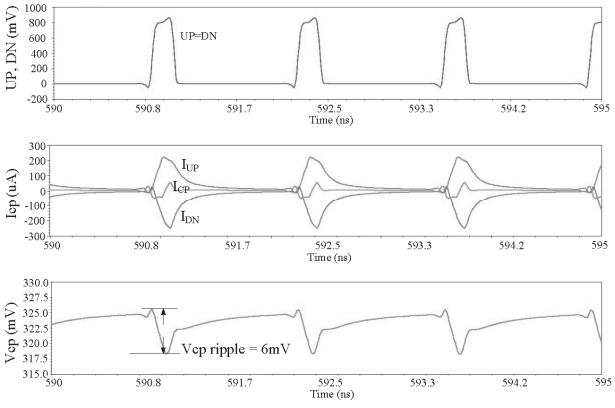

Fig. 9 The simulated current spikes of I_{UP} and I_{DN} and the Vc ripple by Spectre RF.

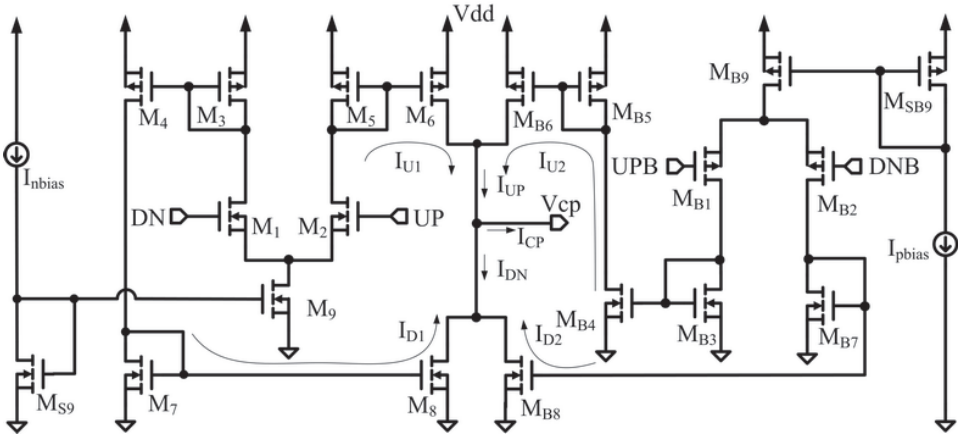

Fig. 8 The proposed circuit diagram of complementary charge pump.

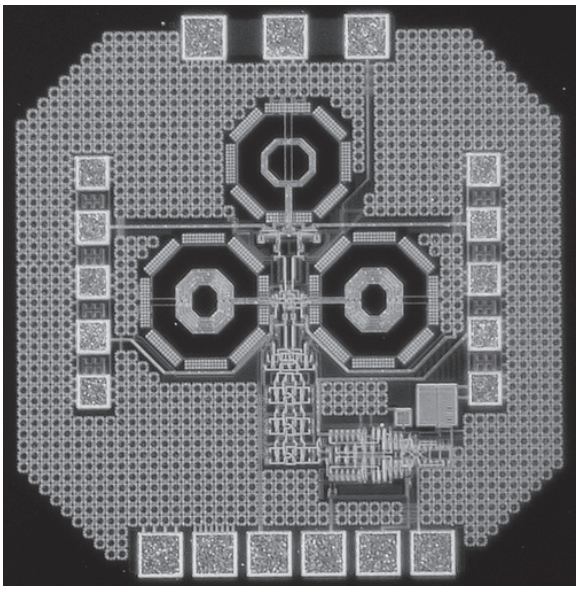

Fig. 10 Chip photo of the fabricated *K*-band current-mode PLL.

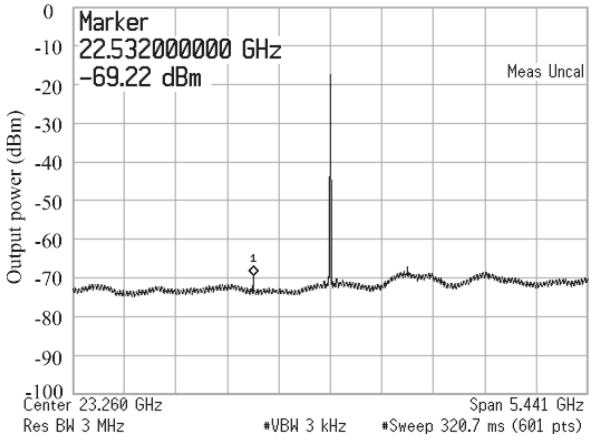

Fig. 11 The measured reference spur of the fabricated *K*-band current-mode PLL.

0.13-μm 1p8m CMOS technology. The chip micrograph of the fabricated PLL is shown in Fig. 10. The area is 1 mm × 1 mm including testing pads. On-wafer probing measurement is adopted to measure the performance of the PLL. There are two GSGSG RF probes with pitch 100 μm, one 100 μm-pitch 6-pin DC probe, and one 150 μm-pitch 3-pin DC probe used to test the chip. The reference clock signal is generated by a signal generator.

The output spectrum of the fabricated PLL is measured from the single-ended output node v_{out1} or v_{out2} and the measurement result is shown in Fig. 11. As can be seen from Fig. 11, the output level is about −17 dBm and the reference spur is about 54 dBc. The reference spur can be expressed by VCO gain [K_{vco} (Hz/V)], amplitude of tuning voltage ripples (v_{ripple}), and reference frequency (f_{ref}) as

$$\text{ref spur in dBc} = 20 \cdot \log_{10} \frac{K_{vco} \cdot v_{ripple}}{2 \cdot f_{ref}} \tag{7}$$

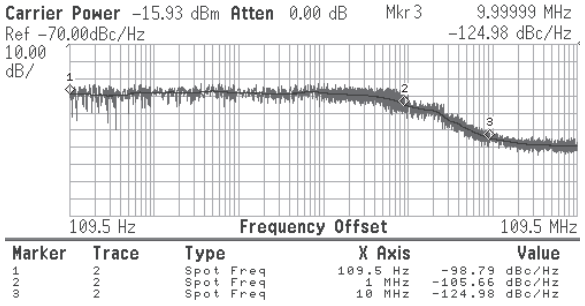

Fig. 12 The measured phase noise of the fabricated *K*-band current-mode PLL.

Table 1 Performance summary and comparison of proposed PLL.

	This work	[3]	[4]	[5]
Vdd [V]	0.8	1.5V, 1.3	1	1.5
Idc without buffer [mA]	11.5	320	17.5	15
VCO tuning range	3%	NA	6%	20%
In-band Phase noise[dBc/Hz]	-98	> -50	-101	-80
Operating frequency [GHz]	22.6-23.3	17.6-19.4	24.2	20.05-21
Reference spur [dBc]	54	44	NA	50
Ref clock [MHz]	728	600	12GHz	78
Technology [CMOS]	0.13-µm	0.13-µm	0.18-µm	0.13-µm
Chip size [mm2]	1x1	1.7	1.235	0.6

From the above equation, it is evident that reducing both v_{ripple} and K_{vco} can minimize the spurs. In addition, the increasing reference frequency also helps to reduce the spur. In the fabricated PLL, due to the low K_{VCO} of DPF-VCO, reduced Vripple of charge pump, and higher reference frequency, the measured reference spur power is −69 dBm, which is 54 dB below the carrier as shown in Fig. 11 at two sides of the center frequency.

The in-band phase noise of the fabricated PLL is measured with −98 dBc/Hz and shown in Fig. 12. The locking range of the PLL is around 700 MHz from 22.6 GHz to 23.3 GHz which is limited by the tuning range of VCO under low supply voltage. Due to the process variations, the operation frequency is shifted down slightly. The total current consumption is 11.5 mA under a 0.8-V power supply. The DPF-VCO and CCMILFD consume 5.2 mA whereas the rest of circuits such as PFD, complementary charge pump, and CML dividers consume 6.3 mA.

The measurement results are summarized in Table 1 where comparisons to other reported PLLs are given. As compared to other PLLs in [3] and [4] which have similar frequency of reference clocks, the proposed PLL has better performances in reference spur and phase noise under the lowest supply voltage of 0.8 V and lower power dissipation of 9.2 mW.

4. Conclusion

In the proposed *K*-band current-mode PLL, the DPF-VCO

is used to enhance the phase noise performance and minimize the power consumption. The current-mode frequency dividers CCMILFD and CICML are adopted to lower the power dissipation and increase the locking range under a low supply voltage of 0.8 V. Besides the design and optimization of circuits, the higher reference clock also helps improve the phase noise and reference spur of the PLL. The measured in-band phase noise of the PLL −98 dBc/Hz and the measured reference spur level is −69 dBm. The locking range of the PLL is from 22.6 GHz to 23.3 GHz and the current consumption of the PLL is 11.5 mA. The chip area of the PLL is 1 mm^2. The performance of the proposed PLL has been verified through the experiment at low supply voltage to show its great potential in applications of low-voltage low-power RF systems.

Acknowledgments

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References

[1] D.-J. Yang and K.O. Kenneth, "A 14-GHz 256/257 dual-modulus prescaler with secondary feedback and its application to a monolithis CMOS 10.4-GHz phase-locked loop," IEEE Trans. Microw. Theory Tech., vol.52, no.2, pp.461–468, Feb. 2004.

[2] M. Tiebout, C. Sandner, H.-D. Wohlmuth, N.D. Dalt, and E. Thaller, "A fully integrated 13 GHz ΔΣ fractional-N PLL in 0.13 μm CMOS," IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp.386–387, Feb. 2004.

[3] J. Kim, J.-K. Kim, B.-J. Lee, N. Kim, D.-J. Jeong, and W. Kim, "A 20-GHz phase-locked loop for 40 Gb/s serializing transmitter in 0.13 μm CMOS," IEEE J. Solid-State Circuits, vol.41, no.4, pp.899–908, April 2006.

[4] W. Alan, L. Ng, C. Gerry, T. Leung, K.-C. Kwok, L. Lincoln, K. Leung, and H.C. Luong, "A 1 V 24 GHz 17.5 mW PLL in 0.18 μm CMOS," IEEE J. Solid-State Circuits, vol.41, no.6, pp.1236–1244, June 2006.

[5] Y. Ding and K.O. Kenneth, "A 21-GHz 8-modulus prescaler and a 20-GHz phase-locked loop fabricated in 130-nm CMOS," IEEE J. Solid-State Circuits, vol.42, no.6, pp.1240–1249, June 2007.

[6] C. Cao and K.O. Kenneth, "A power efficient 26-GHz 32:1 static frequency divider in 130-nm bulk CMOS," IEEE Microwave and Wireless Components Letters, vol.15, no.11, pp.721–723, Nov. 2006.

[7] Z.-D. Huang, C.-Y. Wu, and B.-C. Huang, "Design of 24-GHz 0.8-V 1.5-mW coupling current-mode injection-locked frequency divider with wide locking range," IEEE Trans. Microw. Theory Tech., vol.57, no.8, pp.1948–1958, Aug. 2009.

[8] D.B. Leeson, "A simple model of feedback oscillator noise spectrum," Proc. IEEE, vol.54, pp.329–330, Feb. 1966.

[9] T.H. Lee and A. Hajimiri, "Oscillator phase noise: A tutoial," IEEE J. Solid-State Circuits, vol.35, no.3, pp.326–336, March 2000.

[10] G.-Y. Tak, S.-B. Hyun, T.Y. Kang, B.G. Chio, and S.S. Park, "A 6.3–9-GHz CMOS fast settling PLL for MB-OFEM UWB applications," IEEE J. Solid-State Circuits, vol.40, no.8, pp.1671–1679, Aug. 2005.

[11] M. Mansuri, D. Liu, and C.-K.K. Yang, "Fast frequency acquisition phase-frequency detectors for GSamples/s phase-locked loops," IEEE J. Solid-State Circuits, vol.37, no.10, pp.1331–1334, Oct. 2002.

[12] R. Aparicio and A. Hajimiri, "A noise-shifting differential colpitts VCO," IEEE J. Solid-State Circuits, vol.37, no.12, pp.1728–1736, Dec. 2002.

[13] T. Shibasaki, H. Tamura, K. Kanda, H. Yamaguchi, J. Ogawa, and T. Kuroda, "A 20-GHz injection-locked LC divider with a 25% locking range," IEEE VLSI symposium, pp.170–171, June 2006.

[14] A. Mazzanti, P. Uggetti, and F. Svelto, "Analysis and design of injection-locked LC dividers for quadrature generation," IEEE J. Solid-State Circuits, vol.39, no.9, pp.1425–1433, Sept. 2004.

[15] Marc Tiebout, "A CMOS direct injection-locked oscillator topology as high-frequency low-power frequency divider," IEEE J. Solid State-Circuits, vol.39, no.7, pp.1170–1174, July 2004.

[16] H. Wu and A. Hajimiri, "A 19 GHz 0.5 mW 0.35 μm CMOS frequency divider with shunt-peaking locking-range enhancement," IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp.412–413, Feb. 2001.

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