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Design and implementation of configurable ESD protection cell for 60-GHz RF circuits in a 65-nm CMOS process

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ABSTRACT

The configurable electrostatic discharge (ESD) protection cells have been implemented in a commercial 65-nm CMOS process for 60-GHz RF applications. The distributed ESD protection scheme was modified to be used in this work. With the consideration of parasitic capacitance from I/O pad, the ESD protection cells have reached the 50-Ω input/output matching to reduce the design complexity for RF circuit designer and to provide suitable ESD protection. Experimental results of these ESD protection cells have successfully verified the ESD robustness and the RF characteristics in the 60-GHz frequency band. These ESD protection cells can easily be used for ESD protection design in the 60-GHz RF applications, and accelerate the design cycle.

1. Introduction

Nanoscale CMOS technologies have been used to implement RF circuits due to the advantages of scaling-down feature size, improving high-frequency characteristics, low power consumption, high integration capability, and low cost for mass production. However, the thinner gate oxide in nanoscale CMOS technology seriously degrades the electrostatic discharge (ESD) robustness of IC products [1–4]. Therefore, on-chip ESD protection circuits must be added at all input/output (I/O) pads in RF IC against ESD damages [5]. Several ESD protection designs have been reported for RF circuits. To minimize the impacts from ESD protection circuit on RF performances, the ESD protection circuit at input/output pads must be carefully designed. ESD protection devices cause RF performance degradation with several undesired effects [6–9]. Parasitic capacitance is one of the most important design considerations for RF ICs. Conventional ESD protection devices with large dimensions have the parasitic capacitance which is too large to be tolerated for RF front-end circuits. The parasitic capacitance of ESD protection device causes signal loss from the pad to ground, as shown in Fig. 1. Moreover, the parasitic capacitance also changes the input/output matching condition. Consequently, RF performance is deteriorated. As the operating frequencies of RF circuits are increasing, on-chip ESD protection designs for RF applications are more challenging.

The frequency band of 57–64 GHz has been allocated for unlicensed usage in the next-generation wireless communications. RF circuits operating at this 60-GHz band have the benefits of excellent interference immunity, high security, multi-gigabit speed, and frequency re-usable. Recently, several CMOS transceivers operating at this frequency band have been reported [10–13]. Some ESD protection designs that could be used for 60-GHz broadband RF applications were also presented [14–20]. In this work, the brief review of RF ESD protection designs for 60-GHz band in CMOS processes will be discussed in Section 2.

In the digital or mixed-signal integrated circuits, the standard cell methodology was often used to accelerate the design cycle to shorten the time to market. With the similar concept, the configurable ESD protection cells in CMOS technology for 60-GHz RF applications are implemented in this work to reduce the design complexity for RF circuit designer. The ESD protection cells have reached the 50-Ω input/output matching. Such ESD protection cells have been fabricated to verify their ESD robustness and RF performances [21]. The detailed simulation and measurement results of the ESD protection cells will be presented in Sections 3 and 4.

2. Review of RF ESD protection designs for 60-GHz broadband RF applications

2.1. Typical ESD protection scheme

The typical ESD protection scheme consisted of double diodes at I/O pad, as shown in Fig. 2 [5]. Besides, the power-rail ESD clamp circuit provided ESD current paths between V_{DD} and V_{SS}. In Fig. 2, a P+/N-well diode (D_P) and an N+/P-well diode or an N-well/P-substrate diode (D_N) are placed at input pad or output pad. When D_P and D_N are under forward-biased condition, they can provide efficient discharging paths from I/O pad to V_{DD} and from V_{SS} to I/O pad, respectively.

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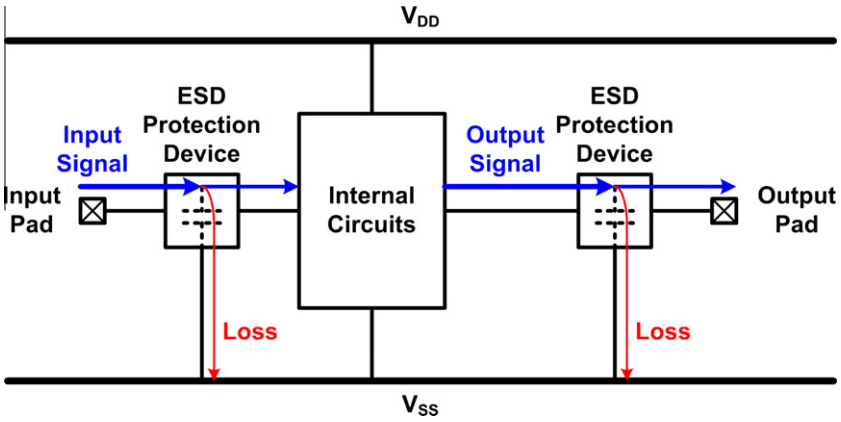

Fig. 1. Signal loss at input and output pads of IC with ESD protection devices.

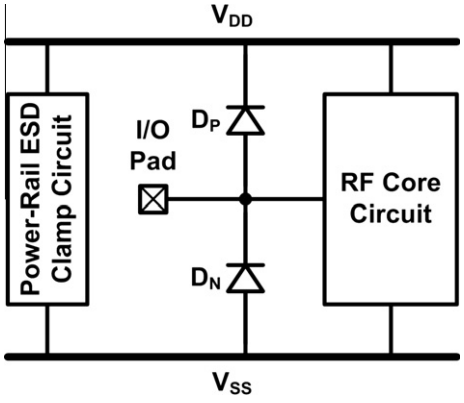

Fig. 2. Typical ESD protection scheme with double diodes at I/O pad.

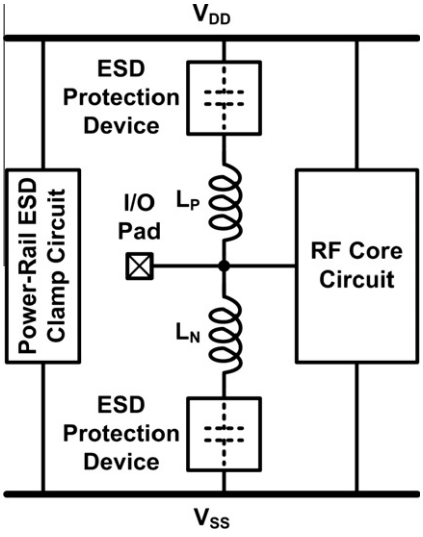

Fig. 3. ESD protection design with series LC resonator.

During positive-to-V_{DD}-mode (PD-mode) and negative-to-V_{SS}-mode (NS-mode) ESD stresses, ESD currents were discharged through the forward-biased D_P and D_N, respectively. Under positive-to-V_{SS}-mode (PS-mode) ESD stress, ESD current was discharged from the I/O pad through the forward-biased D_P to V_{DD}, and discharged to the grounded V_{SS} pad through the turn-on efficient power-rail ESD clamp circuit. Similarly, under negative-to-V_{DD}-mode (ND-mode) ESD stresses, ESD current was discharged from the V_{DD} pad through the turn-on efficient power-rail ESD clamp circuit and the forward-biased D_N to the I/O pad. With the assistance of power-rail ESD clamp circuit, the ESD diodes prevented from being operated under breakdown conditions under PS-mode and ND-mode ESD stresses.

However, this typical ESD protection circuit is only suitable for small ESD protection devices, because the parasitic capacitance of the ESD protection device is directly contributed at the I/O pad. The device dimensions of ESD diodes should be decreased to reduce the parasitic capacitance at I/O pad, which in turn reduces RF performance degradation caused by the parasitic capacitances of the ESD diodes. However, the minimum device dimensions of ESD diodes cannot be shrunk unlimitedly, since the ESD robustness needs to be maintained.

2.2. ESD protection design with series LC resonator

Fig. 3 shows the ESD protection design utilizes the series LC resonator [14]. At frequencies above the resonant frequency of the series LC resonator, the impedance becomes large, which means the signal loss from the ESD protection circuit is reduced. Thus, wideband ESD protection can be achieved by using the series LC resonator. During ESD stresses, the ESD current can be discharged through the inductor (L_P or L_N) and the ESD protection device. However, the transient voltage across the RF circuits under ESD stress is the total voltage drop across the inductor and the ESD protection device. The transient voltage across the RF circuits under ESD stress must be reduced to improve ESD robustness of the RF circuits, especially for the circuits realized in nanoscale CMOS technology.

2.3. ESD protection design with inductor

The ESD protection design with inductor as the ESD protection device for RF circuits had been reported [15]. As shown in Fig. 4, the ESD protection inductor (L_{ESD}) is placed between the input pad and V_{SS}. Besides, a dc blocking capacitor (C_{block}) is needed in this design to provide a separated dc bias for the internal circuits. Since inductor exhibited higher impedance at higher frequencies, and the frequency component of the RF signal is much higher than that of ESD events, the inductor can bypass the ESD current while block the RF signal. To efficiently bypass the ESD current, the metal width of the ESD protection inductor should be wide enough to enhance the current handling capability and to reduce the parasitic series resistance. However, inductors realized by very wide metal traces occupy large chip area. This is the main design concern in the inductor-based ESD protection.

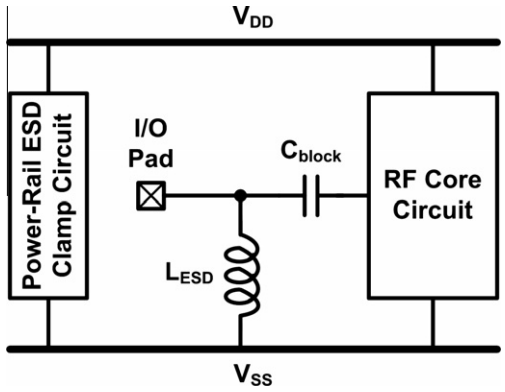

Fig. 4. ESD protection design with inductor.

2.4. ESD protection design with T-coil

ESD protection design for wideband RF applications by using T-coil had been reported [16]. As shown in Fig. 5a, this circuit can provide a purely resistive input impedance of R_T under proper impedance matching design. With proper design, large ESD protection devices can be used without degrading RF performance. Another T-coil-based ESD protection design had been reported. As shown in Fig. 5b, the transformer plus diode (T-diode) was designed for ESD protection in wideband RF circuits [17]. This T-diode also used a transformer (L_1 and L_2) to compensate the parasitics of ESD diodes.

Although the T-coil and the T-diode were suitable for wideband RF front-end circuits, the design concern for the T-coil-based ESD protection was also the inductors, which must be realized by wide metal trace and occupy large chip area.

2.5. Distributed ESD protection scheme

Fig. 6 shows the distributed ESD protection scheme [18]. Such distributed ESD protection scheme can achieve wideband impedance matching as the ESD protection diodes divided into small sections and matched by the inductors. The number of ESD protection diodes can be varied to optimize the performance.

2.6. RF-ESD co-design

ESD protection devices can be treated as a part of the impedance matching network at the I/O pad. By co-designing the ESD protection circuit and the impedance matching network, large ESD protection devices can be used to achieve high ESD robustness without sacrificing RF performance. The RF circuit co-designed with ESD protection devices had been presented. Fig. 7 shows an

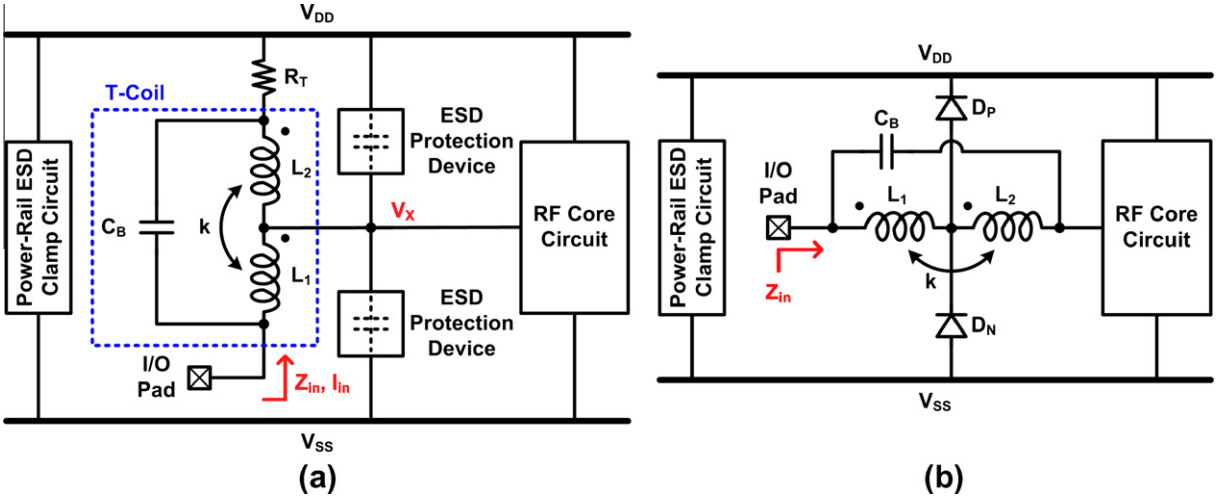

Fig. 5. ESD protection design with (a) T-coil and (b) T-diode.

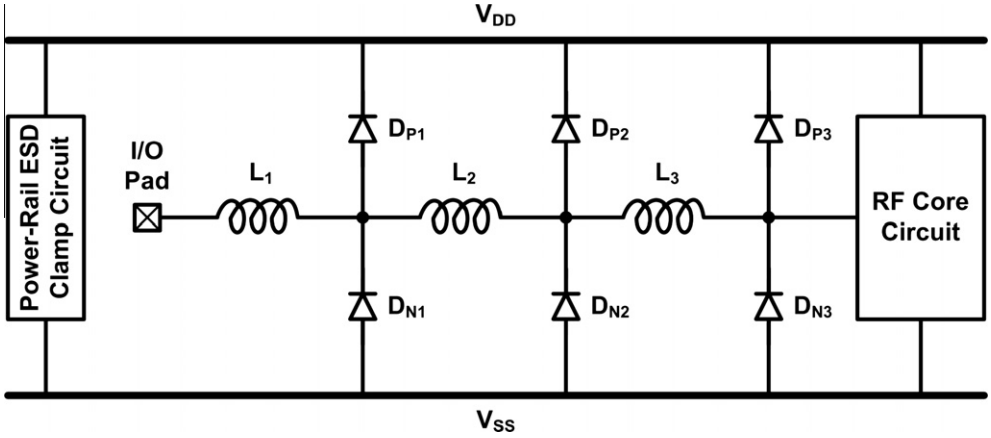

Fig. 6. Distributed ESD protection scheme.

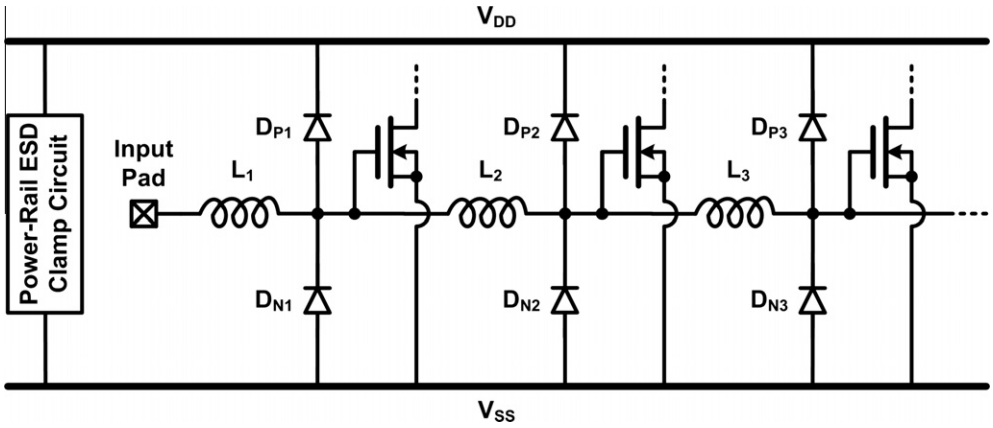

Fig. 7. RF distributed amplifier co-designed with ESD diodes.

example of RF-ESD co-design on the distributed amplifier [19,20]. In this configuration, ESD current can be discharged from the input pad through the ESD diodes to V_{DD} or V_{SS}. Of course, the ESD devices had been carefully designed to provide ESD current paths.

2.7. Comparison among ESD protection designs

The comparison among ESD protection designs for 60-GHz RF circuits is listed in Table 1, where the items to be compared include the need of dc blocking capacitor (C_{block}), signal loss, and ESD level. Besides the ESD protection design with inductor, the C_{block} is not necessary for the I/O pads, which will not limit the design freedom of RF circuits. For the signal loss, the ESD protection designs with extra inductive components can achieve low signal loss. Besides, the inductor size can be scaled down with the increasing operating frequency.

By using the ESD protection scheme of series LC resonator, inductor, T-coil, or distributed ESD protection, the internal circuits can be clamped to the clamping voltage of ESD protection devices. The series LC resonator existed higher clamping voltage, which consists of one inductor and one ESD protection device. With the higher clamping voltage at internal circuits, the ESD protection design performed lower ESD robustness, especially in nanoscale CMOS processes with gate oxide thickness of ~20 Å. The other ESD protection designs are expected to perform good ESD robustness. It should be noted that the inductor has large voltage overshoots during the charged-device model (CDM) ESD stress, which typically has a fast rise time of <1 ns [22]. Therefore, the inductive ESD protection must be carefully designed to prevent from the large voltage overshoots during CDM ESD stress.

Table 1
Comparison among ESD protection designs for 60-GHz RF circuits.

ESD protection design	Needing C_{block}	Signal loss	ESD level
1. Typical ESD protection scheme	No	High	Good
2. ESD protection design with series LC resonator	No	Low	Poor
3. ESD protection design with inductor	Yes	Low	Good
4. ESD protection design with T-coil	No	Low	Good
5. Distributed ESD protection scheme	No	Low	Good
6. RF-ESD co-design	Designable	Designable	Designable

3. ESD protection cell design

To reduce the design complexity for RF circuit designer, the configurable ESD protection cells in 65-nm CMOS technology for 60-GHz RF applications are implemented in this work. These ESD protection cells are designed to be directly used in the RF circuits, and they have reached the 50-Ω input/output matching, as shown in Fig. 8.

In the previous design of distributed ESD protection scheme, the parasitic capacitance of I/O pad was not considered. To realize the configurable ESD protection cells for 60-GHz applications, which the parasitic capacitance of I/O pad is considered, the distributed ESD protection scheme is modified to be used in this work. The ESD protection cells with different ESD robustness are listed in Table 2. Fig. 9a shows the circuit diagrams of the cells A and B with 1-stage ESD protection. The 1-stage ESD protection is designed with a low-C pad, an on-chip spiral inductor, and a pair of ESD diodes. Similarly, the circuit diagrams of the cells C and D with 2-stage ESD protection are shown in Fig. 9b. The 2-stage ESD protection is designed with a low-C pad, two on-chip spiral inductors, and two pairs of ESD diodes. Besides, the power-rail ESD clamp circuit is added beside each ESD protection cells to provide ESD current paths between V_{DD} and V_{SS}.

Although the distributed ESD protection scheme is used in this work, the matching procedures are different. The design procedures of ESD protection cells with 1-stage ESD protection and 2-stage ESD protection are shown in Fig. 10a and b, respectively. The loci of S_{11}-parameters in Fig. 10 are used to achieve input matching. The centered point of the Smith chart is normalized to 50 Ω. The serial numbers (1–4) labeled on each nodes of 1-stage ESD protection in Figs. 9a and 10a indicated the design procedure along the ESD diodes (D_{P1} and D_{N1}), inductor (L_1), and low-C pad from the RF core circuit (modeled as 50-Ω load) to the external

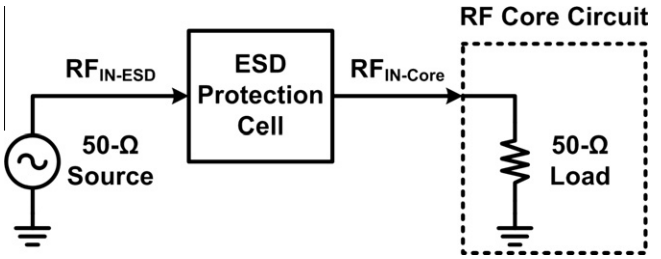

Fig. 8. ESD protection design for 60-GHz RF ICs with 50-Ω-matched ESD protection cell.

Table 2
Design parameters and measurement results of ESD protection cells.

	ESD cell A	ESD cell B	ESD cell C	ESD cell D
Design parameters				
L_1	0.13 nH	0.13 nH	0.1 nH	0.1 nH
D_{P1}	8 μm × 0.6 μm	15 μm × 0.6 μm	13 μm × 0.6 μm	17 μm × 0.6 μm
D_{N1}	8 μm × 0.6 μm	15 μm × 0.6 μm	13 μm × 0.6 μm	17 μm × 0.6 μm
L_2	N/A	N/A	0.06 nH	0.06 nH
D_{P2}	N/A	N/A	10 μm × 0.6 μm	13 μm × 0.6 μm
D_{N2}	N/A	N/A	10 μm × 0.6 μm	13 μm × 0.6 μm
Measurement results				
S_{11}-parameter at 60 GHz	−17.6 dB	−25.3 dB	−27.4 dB	−22.1 dB
S_{21}-parameter at 60 GHz	−0.70 dB	−0.91 dB	−1.83 dB	−2.10 dB
Parasitic cap. at 60 GHz	0.4 fF	0.3 fF	23.7 fF	29.7 fF
Noise figure at 60 GHz	0.5 dB	0.8 dB	1.2 dB	1.5 dB
PS-mode HBM robustness	1 kV	1.75 kV	2.25 kV	2.5 kV
PD-mode HBM robustness	1 kV	2 kV	2.75 kV	3.5 kV
NS-mode HBM robustness	0.75 kV	1.5 kV	2.25 kV	2.75 kV
ND-mode HBM robustness	0.75 kV	1.5 kV	2.25 kV	2.75 kV
PS-mode TLP It_2	0.42 A	0.74 A	1.09 A	1.37 A
PD-mode TLP It_2	0.43 A	0.74 A	1.11 A	1.44 A
NS-mode TLP It_2	0.38 A	0.73 A	1.08 A	1.41 A
ND-mode TLP It_2	0.37 A	0.71 A	1.08 A	1.40 A
PS-mode VF-TLP It_2	0.55 A	0.71 A	0.95 A	1.06 A
PD-Mode VF-TLP It_2	0.66 A	1.10 A	1.53 A	2.02 A
NS-mode VF-TLP It_2	1.56 A	2.82 A	3.93 A	5.14 A
ND-mode VF-TLP It_2	1.56 A	2.69 A	3.91 A	5.09 A

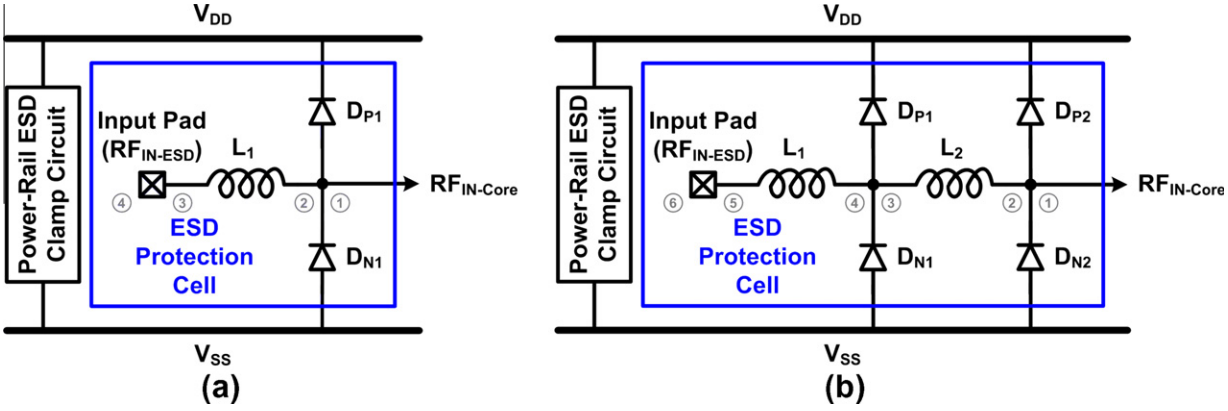

Fig. 9. Circuit diagrams of ESD protection cells with (a) 1-stage ESD protection and (b) 2-stage ESD protection.

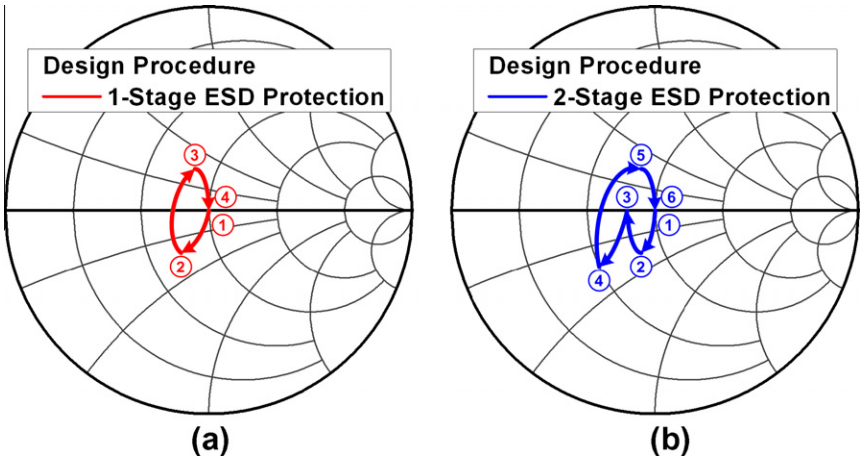

Fig. 10. Design procedures of ESD protection cells with (a) 1-stage ESD protection and (b) 2-stage ESD protection, expressed in Smith chart.

50-Ω source at the input pad. Similarly, the serial numbers (1–6) labeled on each nodes of 2-stage ESD protection in Figs. 9b and 10b indicated the design procedure along the ESD diodes (D_{P2} and D_{N2}), inductor (L_2), ESD diodes (D_{P1} and D_{N1}), inductor (L_1),

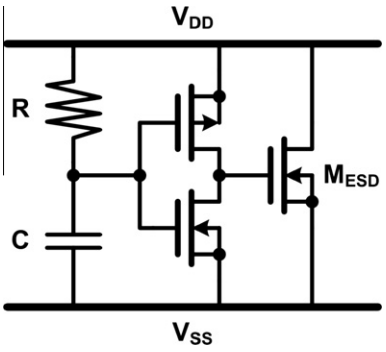

Fig. 11. Power-rail ESD clamp circuit used in this work.

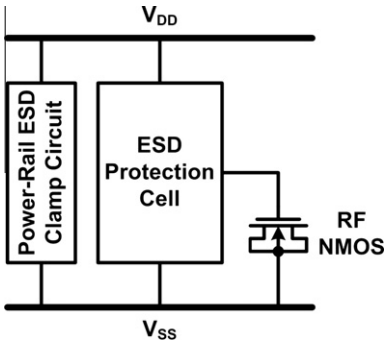

Fig. 13. RF-NMOS emulator to verify ESD protection effectiveness of proposed ESD protection cell.

and low-C pad from the RF core circuit to the input pad. With the final point coming back to the original center point of the Smith chart in Fig. 10, these ESD protection schemes have good matching results.

Fig. 11 shows the power-rail ESD clamp circuit used in this work, where an RC-inverter-triggered NMOS (M_{ESD}) with ~2000-μm width is used. Since the power-rail ESD clamp circuit is placed between V_{DD} and V_{SS}, it does not contribute any parasitic effects to input/output ports. When the PD-mode (NS-mode) ESD stress occurs at the pad, the ESD current can be discharged through the diodes D_P (D_N) from the pad to V_{DD} (V_{SS}). Under PS-mode (ND-mode) ESD stress, the ESD current path consists of the diodes D_P (D_N) and the power-rail ESD clamp circuit. The ESD protection cells can provide the corresponding current discharging paths under all ESD stress modes.

The RF characteristics of the ESD protection cells are simulated by using the microwave circuit simulator ADS. A signal source with 50-Ω impedance drives the $RF_{IN\text{-}ESD}$ of the cell, and a 50-Ω load is connected to $RF_{IN\text{-}Core}$ to simulate the RF circuit. The device parameters of the ESD protection cells are selected by using the aforementioned design procedure. The design parameters of ESD protection cells A, B, C, and D with different ESD robustness are listed in Table 2. In these designs, all diodes are implemented by STI diodes, and the spiral inductors are realized by top thick metal with 5-μm width. These configurable ESD protection cells with different ESD robustness and signal loss can be chosen by RF circuit designer.

The simulated reflection (S_{11}) parameters are shown in Fig. 12a. These ESD protection cells exhibit good input matching (S_{11}-parameters < −12 dB) among 57–64 GHz. The simulated transmission (S_{21}) parameters are compared in Fig. 12b. At 60-GHz frequency, the cells A, B, C, and D have about 0.8-dB, 1.3-dB, 1.6-dB, and 2.2-dB power loss, respectively.

To facilitate the on-wafer RF measurement, one set of these test circuits are arranged with G–S–G style in layout. Besides, another set of the test circuits are implemented with the RF-NMOS emulator, as shown in Fig. 13. The ESD robustness of the ESD-protected RF circuits can be estimated by the ESD protection cell with the RF-NMOS emulator. All test circuits have been fabricated for RF and ESD verifications. Fig. 14a and b shows the die photos of the cells B and D on the fabricated chip, respectively.

4. Experimental results

4.1. RF performances

With the on-wafer RF measurement, the S-parameters of these four ESD protection cells have been extracted around 60 GHz. The voltage supply of V_{DD} (V_{SS}) is 1.2 V (0 V), and the input dc bias is 0.6 V. The source and load resistances to the test circuits are kept at 50 Ω. The measured S_{11}-parameters and S_{21}-parameters versus frequency are shown in Fig. 15a and b, respectively. As shown in Fig. 15a, the S_{11}-parameters of these ESD protection cells among 57–64 GHz are all lower than −15 dB. At 60-GHz frequency, the cells A, B, C, and D have about 0.7-dB, 0.9-dB, 1.8-dB, and 2.1-dB power loss, respectively.

The measured input matching (S_{11}-parameters) and output matching (S_{22}-parameters) expressed in Smith chart of the ESD protection cells within 57–64 GHz are shown in Fig. 15c and d, respectively. All S_{11}-parameters and S_{22}-parameters of these ESD protection cells located around the 50-Ω center point of Smith

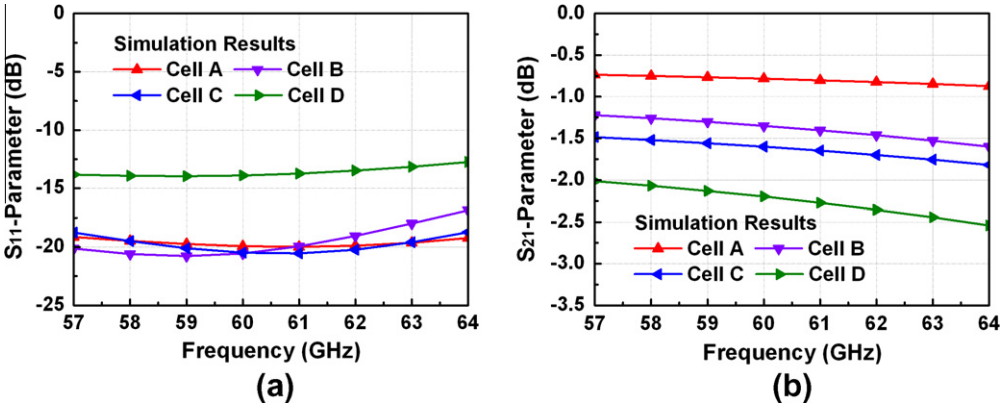

Fig. 12. Simulation results of ESD protection cells on (a) S_{11}-parameters and (b) S_{21}-parameters.

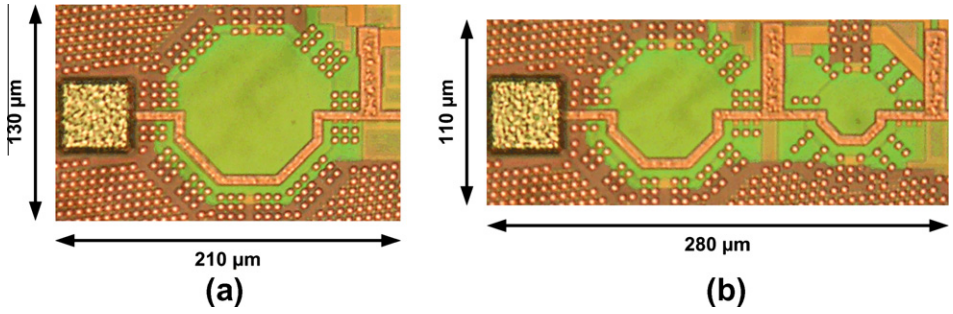

Fig. 14. Die photos of (a) ESD protection cell B and (b) ESD protection cell D.

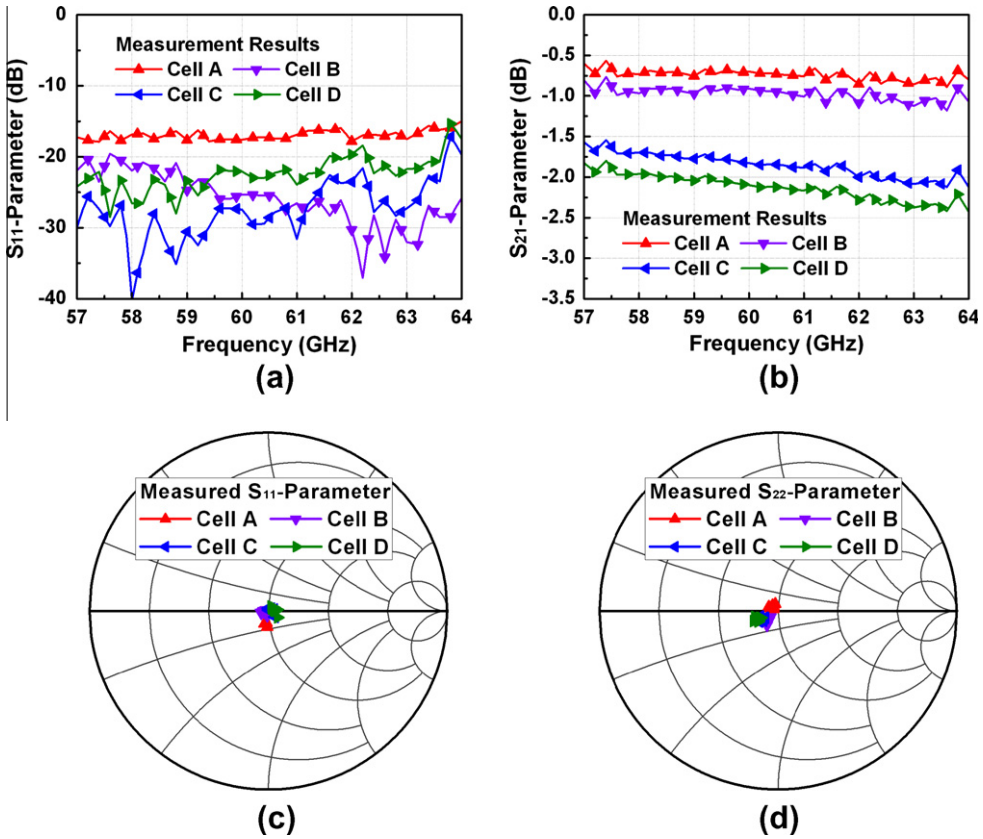

Fig. 15. Measurement results of fabricated ESD protection cells on (a) S_{11}-parameters and (b) S_{21}-parameters versus frequency and (c) S_{11}-parameters and (d) S_{22}-parameters in Smith chart.

chart. Therefore, these 50-Ω-matched ESD protection cells can be directly used in RF circuits.

The parasitic capacitances of the ESD protection cells can be extracted from the measured S-parameters. The extracted parasitic capacitances of the ESD protection cells are shown in Fig. 16. At 60-GHz frequency, the cells A, B, C, and D have about 0.4-fF, 0.3-fF, 23.7-fF, and 29.7-fF parasitic capacitance, which are also listed in Table 2.

4.2. ESD robustness

The human-body-model (HBM) ESD robustness of the fabricated ESD protection cells with the RF-NMOS emulators are evaluated by the ESD tester. The PS-mode, PD-mode, NS-mode, and ND-mode ESD robustness of all ESD protection cells are listed in Table 2. The cells A, B, C, and D can sustain 0.75-kV, 1.5-kV, 2.25-kV, and 2.5-kV HBM ESD tests, respectively. Besides, the power-rail ESD clamp circuit can sustain over 8-kV HBM ESD tests.

The *I–V* characteristics of the ESD protection cells in high-current regions were characterized by using the transmission line pulsing (TLP) system with 10-ns rise time and 100-ns pulse width. Fig. 17a–d shows the TLP-measured *I–V* curves of the fabricated ESD protection cells under PS-mode, PD-mode, NS-mode, and ND-mode tests, respectively. The secondary breakdown currents (It_2) indicated the current-handling ability of ESD protection cells were obtained from the TLP-measured *I–V* curves. The secondary breakdown currents of ESD protection cells are listed in Table 2.

Another very fast TLP (VF-TLP) system with 0.2-ns rise time and 1-ns pulse width was also used in this study. The VF-TLP system can be used to capture the transient behavior of ESD protection cells in the time domain of charged-device-model (CDM) ESD event [23]. The VF-TLP-measured It_2 of ESD protection cells are also

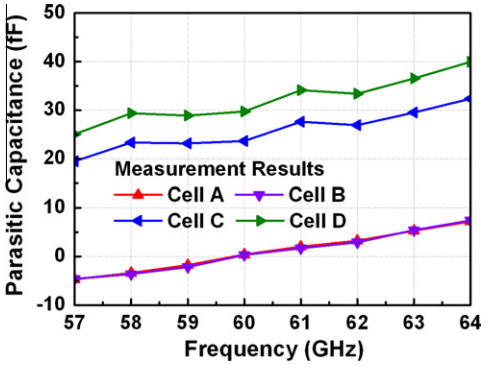

Fig. 16. Measurement results of fabricated ESD protection cells on parasitic capacitances.

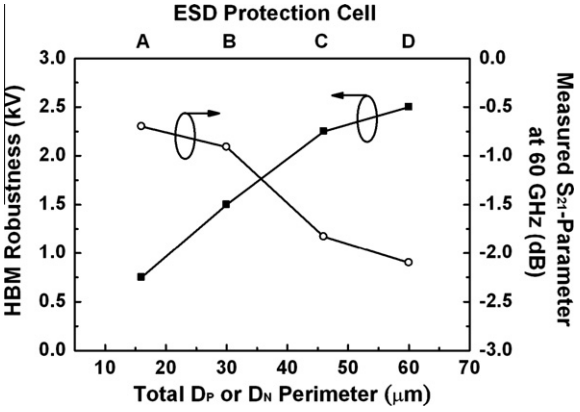

Fig. 18. Dependence of HBM ESD robustness and measured S_{21}-parameters of ESD protection cells on different D_P or D_N size.

listed in Table 2. The VF-TLP-measured It_2 are similar to the peak currents under CDM ESD tests. Therefore, with these VF-TLP-measured data, the CDM ESD robustness of final product can be expected [23].

4.3. Comparison

The HBM ESD robustness and the measured S_{21}-parameters at 60 GHz of ESD protection cells on different D_P or D_N size are compared in Fig. 18. According to the experimental results, the S_{21}-parameters/HBM ESD robustness of cells A, B, C, and D are −0.70/0.75, −0.91/1.5, −1.83/2.25, and −2.10/2.5 dB/kV, respectively. The ratios of S_{21}-parameters at 60 GHz to HBM ESD robustness of ESD protection cells are about −1 dB/kV. Although the power losses are increased with the increases of D_P or D_N size, the ESD protection cells can effectively protect the RF circuits.

5. Example of ESD protection cells applied to 60-GHz LNA

The ESD cells can be easily used to protect the 60-GHz RF circuits. Fig. 19 shows the ESD protection cell applied to a 60-GHz low-noise amplifier (LNA) [12]. The RF characteristics of LNA with

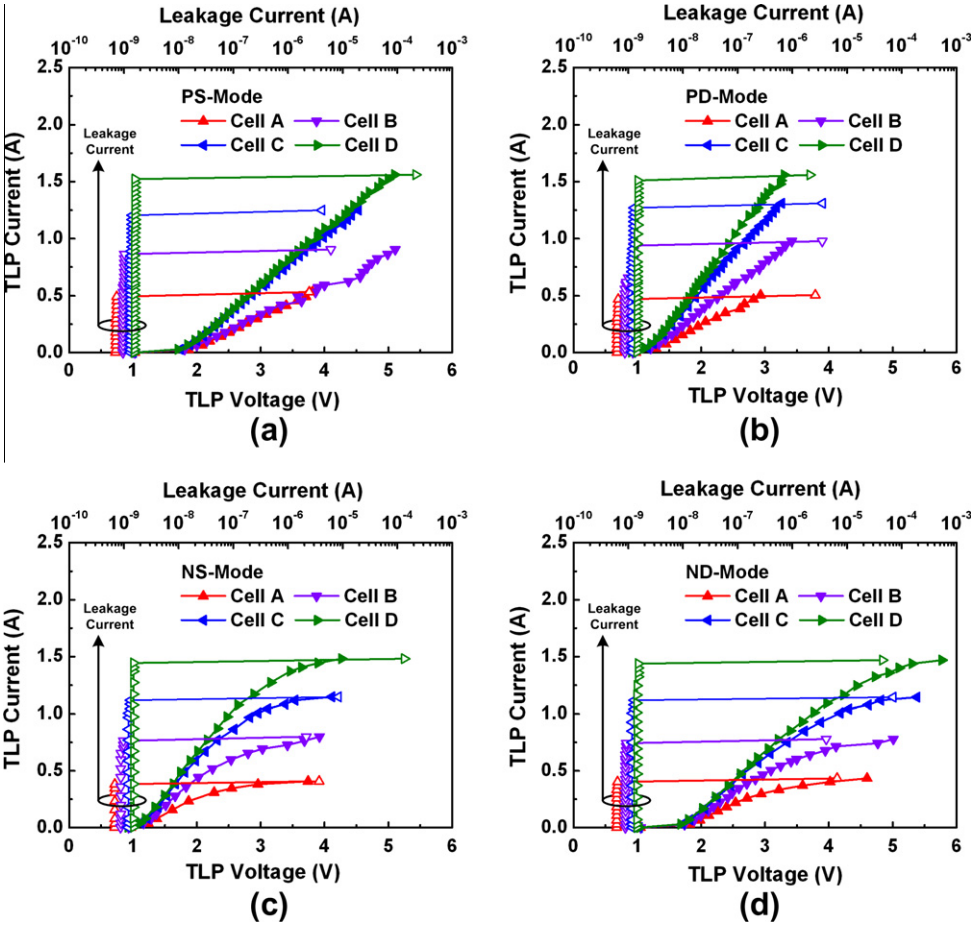

Fig. 17. TLP-measured *I–V* characteristics of ESD protection cells under (a) PS-mode, (b) PD-mode, NS-mode, and (d) ND-mode tests.

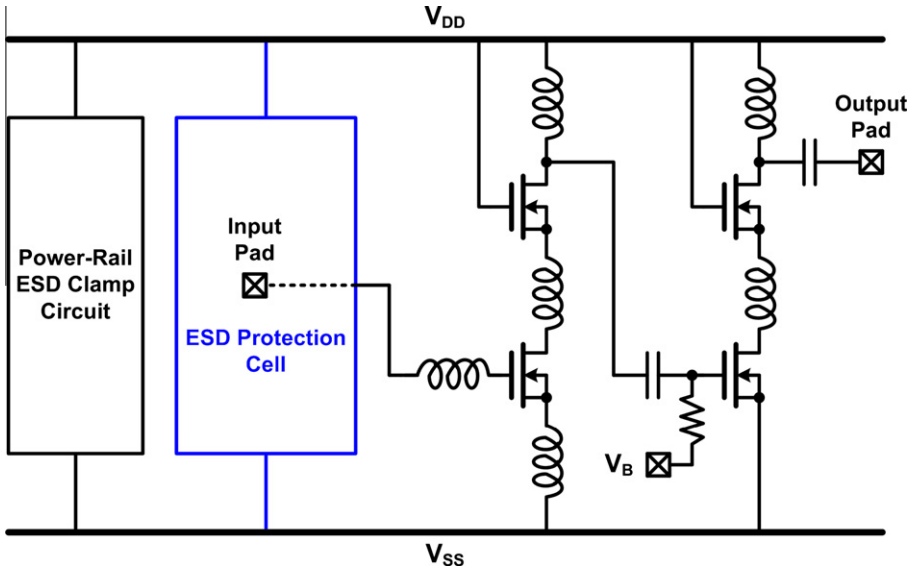

Fig. 19. Circuit schematic of 60-GHz LNA with ESD protection cell.

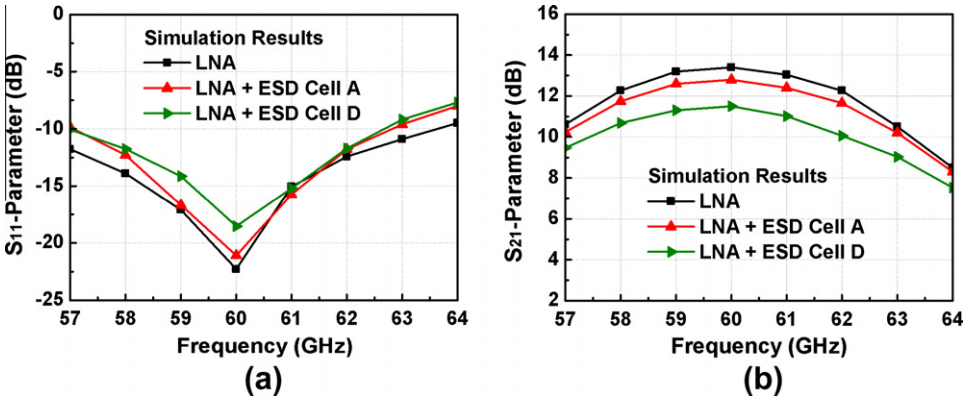

Fig. 20. Simulation results of 60-GHz LNA with and without ESD protection cells on (a) S_{11}-parameters and (b) S_{21}-parameters.

and without ESD protection cells are simulated in 65-nm CMOS process. The used RF simulator was also ADS.

As simulating the RF performances, the previous measured S-parameters of ESD protection cells are inserted at the first stage of the 60-GHz LNA. Fig. 20a and b shows the simulated S_{11}-parameters and S_{21}-parameters of 60-GHz LNA with and without ESD protection cells. As shown in Fig. 20a, the LNA without ESD cell achieves good input matching (S_{11}-parameters < −20 dB) at operating frequency. After adding ESD cell A or D in the LNA, the simulated S_{11}-parameters are still less than −15 dB. The LNA without ESD cell achieves 13.4-dB power gain (S_{21}-parameters) at 60 GHz, as shown in Fig. 20b. With the ESD protection cell A or D adding in the LNA, the simulated power gain becomes 12.8 dB or 11.5 dB at 60 GHz. Although the ESD protection cells slightly degrade the RF performances of LNA, they can provide suitable ESD protection.

6. Conclusion

In this work, the ESD protection cells for 60-GHz RF applications are presented. These ESD protection cells have reached the 50-Ω input/output matching. These useful ESD protection cells reduce the design complexity for RF circuit designer and provide suitable ESD robustness. These ESD protection cells are developed to support foundry's customers for them to easily apply ESD protection in the 60-GHz RF circuits. Verified in commercial 65-nm CMOS process, the cells A, B, C, and D have about 0.7-dB, 0.9-dB, 1.8-dB, and 2.1-dB power loss, respectively. Besides, they can sustain 0.75-kV, 1.5-kV, 2.25-kV, and 2.5-kV HBM ESD tests, respectively.

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