Electrical and Reliability Investigation of Cu TSVs With Low-Temperature Cu/Sn and BCB Hybrid Bond Scheme

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***Abstract*—A wafer-level 3-D integration scheme using Cu through-silicon vias (TSVs) and fine-pitch Cu/Sn–BCB hybrid bonding was developed and investigated with electrical characterization and reliability assessment. The hybrid bonding could be achieved below 250 °C. Low Kelvin resistance and stable daisy chain resistance were achieved in 5- and 10-μm TSV test structures across the whole wafer. Without obvious deterioration in reliability test results, the integrated Cu TSV and hybrid bond scheme can be potentially designed for 3-D integration applications.**

***Index Terms*—Hybrid bonding, through-silicon via (TSV), 3-D integration.**

I. Introduction

THREE-dimensional integrated circuits are well known as one of the most promising approaches to extend and even beyond "Moore's law" [1]–[6]. This is due to advantages such as smaller form factor, higher performance, low power consumption, and great ability of heterogeneous integration [2], [5]. Several 3-D integration schemes have been proposed in worldwide companies and institutes to establish 3-D integration platforms [6]–[8].

Bonding technology is significant in 3-D integration for vertical stack of active layers. Among various bonding approaches, oxide bonding is usually limited by the surface planarization and particle contamination, whereas metal and polymer hybrid bonding is an attractive option to attain the simultaneous formation of electrical interconnect and mechanical strength. Therefore, hybrid bonding has a high possibility of process flow simplification and cost reduction for 3-D integration. In previous researches, Cu-based hybrid bonding with oxide and BCB has been investigated [4], [8]. However, the research does not perform the complete 3-D integration with reliability evaluation yet. In addition, high bonding temperature about 350 °C−400 °C for Cu bonding [12] is required and may induce possible damage and thermal stress. This letter reports the demonstration and corresponding electrical and reliable performances of the wafer-level 3-D integration scheme with Cu through-silicon vias (TSVs) based on Cu/Sn and BCB low-temperature hybrid bonding.

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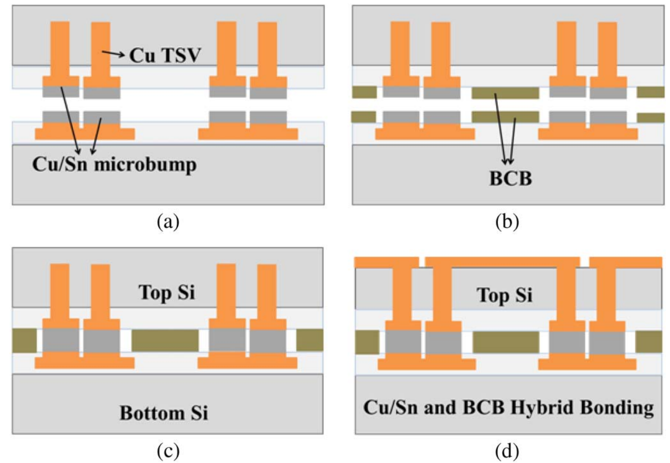

Fig. 1. Structure design and process flow of 3-D integration. (a) Cu/Sn microbumps. (b) BCB coating and lithography. (c) Hybrid bonding. (d) Thinning and backside RDL.

II. Fabrication of Cu TSV and Cu/Sn–BCB Hybrid Bonding

Fig. 1 shows the structure design and schematic process flow of the carrierless wafer-level 3-D integration scheme. Several key technologies were adopted to perform the integration scheme, such as Cu TSVs, fine-pitch Cu/Sn microbumps, BCB patterning, hybrid bonding, wafer thinning, and backside redistribution layer (RDL) formation. Cu TSVs were formed by the sequential steps of the deep reactive-ion etching Bosch process for 40-μm via depth etching, 400-nm plasma-enhanced tetraethyl orthosilicate oxide liner deposition, TiN/Cu barrier/seed layer sputtering, Cu filling, and overburden chemical mechanical polishing (CMP). Fine-pitch Cu/Sn microbumps were fabricated on a bottom wafer, while Cu TSVs on a top wafer. BCB was then spun on both the top and bottom wafers and lithographed for patterning. The 3/2-μm-thick Cu/Sn and 4-μm BCB were adopted to perform hybrid bonding under 10^{-3} torr, at 250 °C for 30 min. After bonding, the top wafer was thinned down to 40 μm by grinding and CMP to expose Cu TSVs. Passivation polyimide (PI) was then

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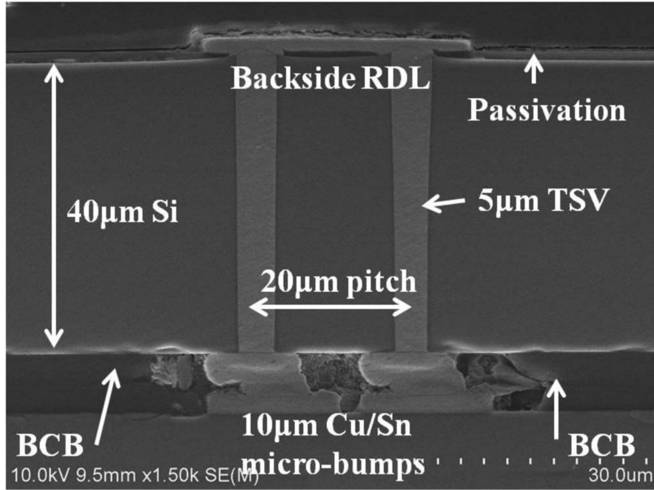

Fig. 2. Cross-sectional SEM image of the 3-D integration scheme: 5-μm-via size 40-μm-depth Cu TSV based on fine-pitch Cu/Sn and BCB hybrid bonding. Both bonding interfaces of the two bond structures disappear after thickness optimization of Cu/Sn and BCB.

TABLE I
TSV PARAMETERS INCLUDE VIA DIAMETER, PITCH, VIA DEPTH, AND BUMP SIZE IN THE INTEGRATION SCHEME

	Via	*Pitch*	*Depth*	*Bump*
Size A	5 μm	20 μm	40 μm	10 μm
Size B	10 μm	40 μm	40 μm	20 μm

covered and patterned, followed by backside RDL to perform the 3-D integration scheme.

The wafer-level integration with Cu TSVs based on Cu/Sn and BCB hybrid bonding was successfully developed under 250 °C low bonding temperature. Fig. 2 shows the cross-sectional scanning electron microscope (SEM) image of the completed 3-D integration scheme. The image also shows that no voids or seams in Cu TSVs and bonding joints, which indicates good TSV filling and bonding integrity for the follow-up processes without any cracks in BCB.

III. ELECTRICAL INVESTIGATION OF Cu TSV AND Cu/Sn MICROBUMP INTERCONNECTION

Kelvin structure and daisy chain with 5- and 10-μm TSVs in this 3-D integration scheme were fabricated and investigated with electrical property and reliability. Table I presents TSV parameters including via diameter, pitch, via depth, and bump size in the integration scheme. The four-point source measurement unit measurement method for effectively removing the loading effect was applied with sweeping injection current from -100 to 100 mA to extract ΔV between the two pads. As the illustration shown in Fig. 3(a), the theoretical resistances could be simply expressed in (1) and (2). Herein, Rs is the resistance of top/bottom metallization, and N is the total number of via chain. Thus

$$R_{\text{Kelvin}} = R_{10\,\mu\text{m}\,\text{TSV}} + R_{\text{CuSn_microbump}} \quad (1)$$

$$R_{\text{daisy_chain}} = N \cdot (R_{\text{unit_cell}}). \quad (2)$$

Fig. 3(b) shows the electrical results of 10-μm Kelvin structure and $N = 200$ daisy chain. The low Kelvin resistance of

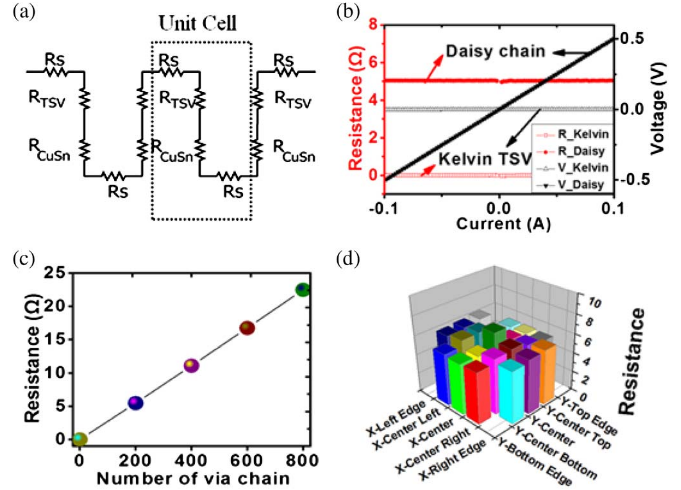

Fig. 3. Electrical characterization of the 3-D integration scheme. (a) Illustration of an equivalent via chain circuit. (b) 10-μm TSV Kelvin resistance ($\sim$12 mΩ) and $N = 200$ daisy chain resistance ($\sim$5 Ω). (c) Via chain characteristics of $N = 800$ series. (d) Chain resistances on different wafer locations.

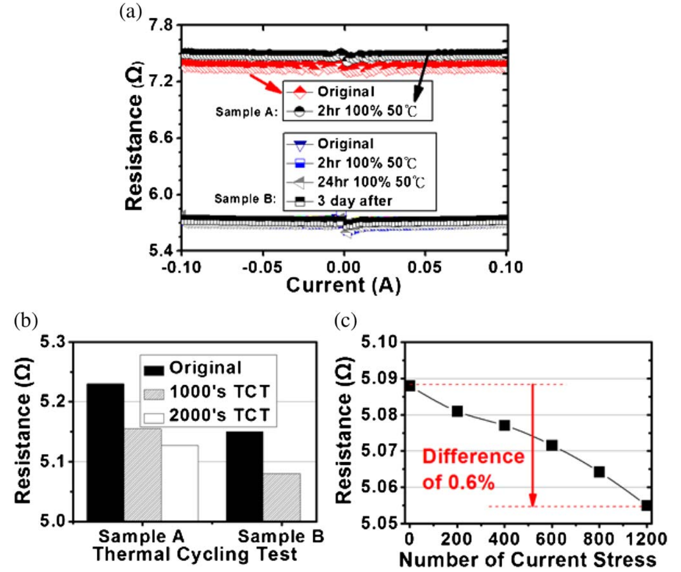

Fig. 4. Reliability test results of (a) humidity test, (b) thermal cycle test, and (c) multiple current stressing.

12 mΩ and the stable daisy resistance of 5 Ω indicate that the major contribution of resistance is resulted from the top and bottom metallization. Fig. 3(c) shows the electrical measurement results and via chain characteristics. The resistance linearly increases by increasing the number of 10-μm via chain, even up to $N = 800$ series. The large number of via chain without any electrical open reveals excellent bonding integrity and a reliable process for the 3-D scheme integration. Fig. 3(d) shows the chain resistances on various wafer locations. The resistance deviation is below 10%, indicating excellent integration performance and accurate alignment across the whole wafer.

IV. RELIABILITY TEST OF 3-D INTEGRATION SCHEME

The electrical characterization results presented the excellent performance of Cu TSVs and Cu/Sn microbump interconnection. To consider the mass production application, the

reliability assessment was performed with humidity test, ac current stressing, and thermal cycle test. Fig. 4(a) shows the results of 45 °C and 100% humidity test for 2 h. No obvious deterioration was observed, even after a three-day test, which indicates the excellent sealing capability of BCB. It provides the good seal protection against corrosion and metal oxidation in the moist environment. The slight resistance increase may come from the resistance change of the RDL level after the humidity test. Fig. 4(b) shows the results of the thermal cycle test. Several samples were tested by using JESD22-A104B temperature cycling test (TCT) equipment under conditions of -40 °C-125 °C with the dwell time of 5 min and the ramping rate of 15 °C/min. Resistances were extracted regularly every 1000 cycles of TCT. All the samples passed the first 1000 cycles. After high-cycle operation, the observed failures were majorly from the coefficient of thermal expansion mismatch-caused peeling at the RDL–PI interface and a few from the thermostress-induced debond at the BCB bonding interface in the inspection results. In addition, the measurement results show even a slight resistance improvement. Fig. 4(c) shows the result of multiple current stressing with the applied current from -100 to 100 mA. Although the large current density of 10^5 A/cm^2 may induce the metal atom migration, the result even shows 0.6% resistance reduction, which may come from the metal grain growth and possible disappearance of the bonding interface. All the reliability test results imply that the 3-D integration scheme is quite reliable and could be potentially applied for product manufacture.

V. Conclusion

In this letter, one wafer-level 3-D integration scheme with Cu TSVs based on Cu/Sn and BCB hybrid bonding has been successfully demonstrated. With the low-temperature hybrid bonding technology, the scheme has low Kelvin resistance and stable via chain resistance across the whole wafer. The reliability test results show no obvious deterioration, which indicates that the integration scheme could be potentially applied for 3-D integration applications.

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