

Lateral Two-Dimensional p-i-n Diode in a Completely Undoped GaAs/AlGaAs Quantum Well

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2013 Jpn. J. Appl. Phys. 52 014001

(<http://iopscience.iop.org/1347-4065/52/1R/014001>)

View [the table of contents for this issue](#), or go to the [journal homepage](#) for more

Download details:

IP Address: 140.113.38.11

This content was downloaded on 28/04/2014 at 01:13

Please note that [terms and conditions apply](#).

Lateral Two-Dimensional p–i–n Diode in a Completely Undoped GaAs/AlGaAs Quantum Well

Van-Truong Dai^{1*}, Sheng-Di Lin¹, Shih-Wei Lin¹, Jau-Yang Wu¹, Liang-Chen Li², and Chien-Ping Lee¹

¹Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan

²Center for Nano Science and Technology, National Chiao Tung University, Hsinchu 300, Taiwan

E-mail: daitruong.ee96g@g2.nctu.edu.tw

Received August 3, 2012; accepted October 16, 2012; published online December 10, 2012

A lateral two-dimensional p–i–n junction in an entirely undoped GaAs/AlGaAs quantum well has been fabricated. The optical and electrical characteristics of the junction are reported. The threshold voltage of the junction and the electroluminescence spectrum of the quantum well confirm the formation of the lateral two-dimensional junction. © 2013 The Japan Society of Applied Physics

1. Introduction

In recent years, there has been an increasing interest in the surface acoustic wave (SAW)-driven single-photon sources owing to their potential applications in high-speed quantum communications.^{1–3)} Foden et al.¹⁾ proposed that when a SAW propagates through a two-dimensional (2D) p–i–n junction, a series of traveling quantum dots are formed in the i-region of the junction. Consequently, a constant stream of electron packets, which can be manipulated by a controlled gate voltage, flows from a two-dimensional electron gas (2DEG) channel into a two-dimensional hole gas (2DHG) channel, where electrons and holes are recombined to create bursts of optical pulses. By controlling the split gate voltage, one can obtain a stream of single electrons to generate single photons. In SAW-driven single-photon source devices, the key component is a high-quality 2D p–i–n junction.

Most of the III–V optoelectronic devices rely on junctions formed by stacks of epilayers, where the electrical current flows across the junction vertical to the sample surface. The lateral p–n junctions, which are difficult to fabricate and seldom used, however, are often desirable for many device applications. The lateral p–n junctions have a coplanar geometry; therefore, they are suitable for optoelectronic integration. In addition, they allow direct injection of electrons and holes into the active region of a device without having to pass through the higher-band-gap materials. Consequently, the transit time of injection carriers can be reduced. Furthermore, since the cross section of the lateral junction is determined by the thickness of the epilayer, the capacitance of the junction can be much smaller than that of conventional vertical junctions. Thus, the 2D lateral junctions can lead to a new family of high-frequency and optoelectronic devices.^{4–9)} Furthermore, lateral 2D p–n junctions are also potential candidates for investigating the properties of electron spins in low-dimensional systems by optical methods.¹⁰⁾

With the aim of reliably fabricating 2D lateral p–n junctions, several methods have been developed over the past years.^{2,3,6–8,10–15)} The authors of Refs. 2, 12, and 13 fabricated lateral p–n junctions by molecular beam epitaxy (MBE) growth on a patterned GaAs substrate. The amphoteric nature of the Si dopant was employed to simultaneously form 2DEG on the (001) planes and 2DHG on (113)A planes on the patterned substrates. Kaestner et al.¹⁵⁾ used a partly etched GaAs/AlGaAs heterostructure to define a 2DEG

region and a 2DHG region. Hosey et al.¹⁴⁾ integrated MBE growth with a focused ion beam to fabricate a lateral p–n junction. In the present work, we developed a reliable and relatively easy method to fabricate a lateral p–i–n junction in a completely undoped GaAs/AlGaAs quantum well structure by utilizing conventional metallization and lithography processes. By using metal–insulator–semiconductor (MIS) structures, 2DEG or 2DHG can be induced in the quantum well under appropriate gate biases. A dual gate structure is used so that 2DEG and 2DHG can be formed side by side to create a lateral p–n junction.

2. Sample Design and Process

The layer structure used for lateral junction fabrication is that of a GaAs/AlGaAs quantum well shown in Fig. 1(a). The sample was grown on a semi-insulating (100) GaAs substrate by using a solid-source MBE system. A 400 nm Al_{0.33}Ga_{0.67}As was grown on top of a 100 nm GaAs buffer layer, followed by a 10-period GaAs/Al_{0.33}Ga_{0.67}As (3 nm/3 nm) superlattice. A 20 nm GaAs quantum well between two Al_{0.33}Ga_{0.67}As barriers was grown as the conductive channel of the device. Finally, the sample was capped with a 10 nm GaAs layer. All the layers were completely undoped.

The device processing starts with a mesa etching step to define the channel region. The n-type ohmic contact region was then defined and recessed down to the GaAs channel. Afterwards, the n-type contact metal composed of Ni/Ge/Au/Ni (5 nm/70 nm/70 nm/35 nm) was deposited by E-gun evaporation and annealed at 450 °C for 2 min. The p-type contact metal of Pd/AuZn (40 nm/100 nm) was annealed at 420 °C for 2 min. A photosensitive polyimide insulator (SU-8 2000.5, HD Microsystems) was then coated and patterned on the surface and cured for 30 min at 200 °C in nitrogen, which gave a thickness of about 350 nm. Finally, the metal Ti/Au (20 nm/100 nm) was deposited on top of the polyimide layer to form the gate.

The top view of a finished device is shown in Fig. 1(b). The upper half is the p-channel device and the lower half is the n-channel device. The devices are normally off because the epitaxy layers are totally undoped. With a negative (positive) voltage applied on the p-gate (n-gate) of the p-channel (n-channel) device, the 2D hole (electron) gases in the p-channel (n-channel) can be electrically induced. By measuring the conductance between the two p-ohmic (n-ohmic) contacts, we can determine the threshold voltage of the p-channel (n-channel) devices.

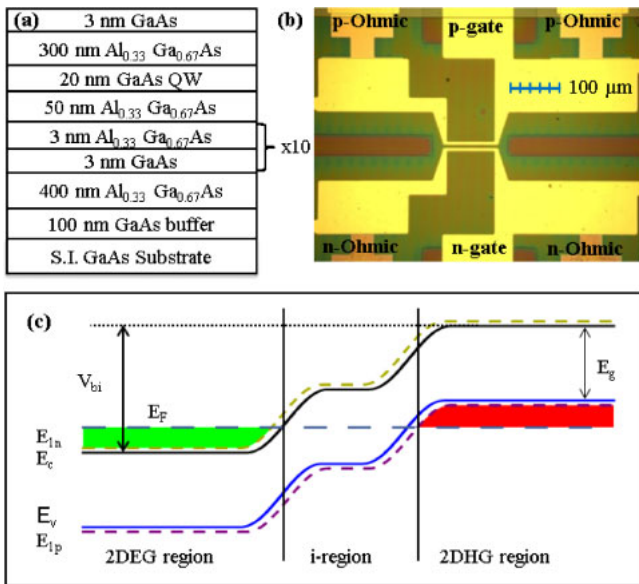


Fig. 1. (Color online) (a) Lateral 2D p-i-n structures grown by MBE. (b) Optical microscopy image of the finished device. (c) Schematic band energy diagram of the lateral 2D p-i-n diode at equilibrium $V_{pn} = 0$ and induced 2DEG and 2DHG underneath n-gate and p-gate, respectively.

3. Results and Discussion

In our device layout, the n-gate and the p-gate are placed side by side with 5 μm spacing [see Fig. 1(b)]. With a negative voltage applied on the p-gate and a positive voltage applied on the n-gate, both 2DHG and 2DEG channels can be induced in the GaAs quantum well, so a lateral 2D p-i-n diode is formed. The schematic band diagram along the channel of the 2D p-i-n diode is shown in Fig. 1(c). E_{1n} and E_{1p} are the ground state energies for the electrons and holes, respectively, E_F is the Fermi level in the quantum well, and E_g is the GaAs band gap. Using an infinitely deep quantum well approximation, the built-in voltage V_{bi} of the lateral p-n junction is given by¹⁶⁾

$$eV_{bi} = E_g + \frac{\pi\hbar^2 N_{sp}}{m_p} + \frac{\pi\hbar^2 N_{sn}}{m_n} + \frac{\pi^2\hbar^2}{2d^2} \frac{m_n + m_p}{m_n m_{np}},$$

where N_{sp} and N_{sn} are the area densities of electrons and holes in the 2DHG and 2DEG, respectively, d is the width of the quantum well, and m_n and m_p are the effective electron and hole masses, respectively. N_{sp} and N_{sn} are functions of gate voltage. In a GaAs/AlGaAs quantum well ($m_n = 0.067 m_0$, $m_p = 0.48 m_0$, and $E_g = 1.515 \text{ eV}$ at 77 K), we can approximate $N_{sp} = N_{sn} = 10^{11} \text{ cm}^{-2}$. With the quantum well width $d = 20 \text{ nm}$, the built-in voltage is estimated to be $V_{bi} = 1.535 \text{ V}$ at 77 K. The built-in potential eV_{bi} of the lateral 2D junction is larger than the band gap E_g .

The fabricated device [Fig. 1(b)] has a channel length of 120 μm and channel width of 7.5 μm for both 2DEG and 2DHG channels. The spacing between the n-gate and the p-gate is 5 μm . The device was mounted on a ceramic holder and wire-bonded, and then placed in a low-temperature tank for electrical measurement. In Fig. 2, we show the drain current versus gate voltage curve for the n-channel device measured at 77 K and the drain-source voltage V_{ds} of

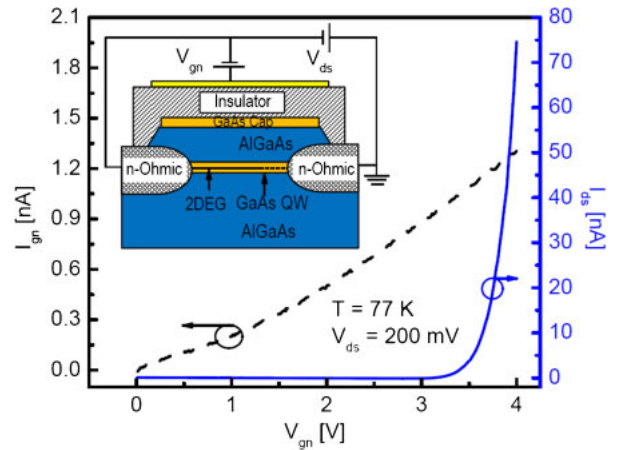


Fig. 2. (Color online) Current-voltage characteristics of 2DEG at temperature of 77 K and bias of $V_{ds} = 200 \text{ mV}$ between n-drain and n-source. The solid line is the drain current and the dashed line is the gate leakage current. The inset shows a schematic diagram of the measurement setup for the 2DEG channel.

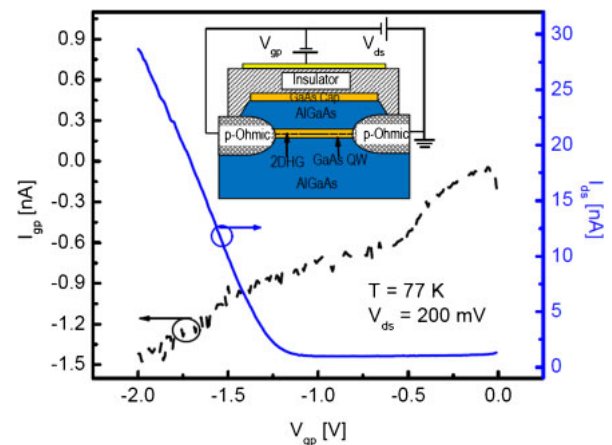


Fig. 3. (Color online) Current-voltage characteristics of 2DHG at temperature of 77 K and bias of $V_{ds} = 200 \text{ mV}$ between p-drain and p-source. The solid line is the drain current and the dashed line is the gate leakage current. The inset shows a schematic diagram of the measurement setup for the 2DHG channel.

200 mV. The inset shows a schematic of the measurement setup for the 2DEG channel. The n-channel device turned on at a threshold voltage of +3.5 V. To ensure that the insulator layer is working well, the gate current I_{gn} was monitored at the same time. The leakage current I_{gn} is less than 1.5 nA up to 4.0 V (see Fig. 2). Similarly, the electrical characteristics of the p-channel device were measured with a negative gate bias. Figure 3 shows the measured drain and gate currents. The threshold voltage of the p-channel device is about -1.25 V. The gate leakage current I_{gp} was less than 1.5 nA with the bias up to -2 V. Because of the presence of negative charges on the GaAs/polyimide interface,^{17,18)} the threshold voltage of the n- and p-channel shifts towards more positive values. Therefore, the threshold of the p-channel is smaller than that of the n-channel. In fact, the threshold voltages of the p- and n-device depend on the measurement condition, because the interface charges change over long periods and when the device is illuminated.

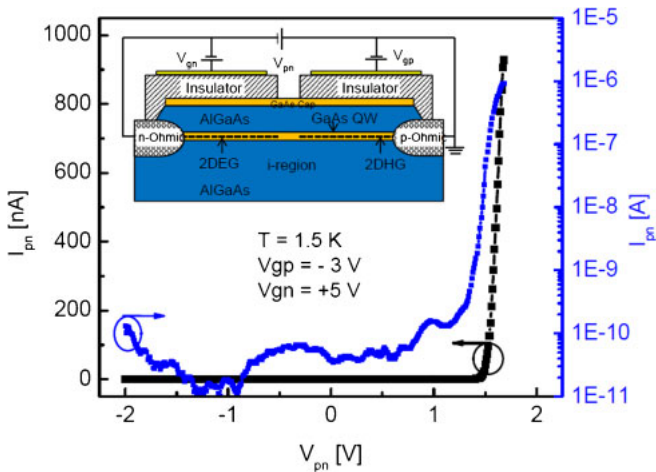


Fig. 4. (Color online) Current–voltage characteristics of the lateral 2D p–i–n diode at temperature of 1.5 K with p–gate and n–gate biasing at $V_{gp} = -3$ V and $V_{gn} = +5$ V, respectively. V_{pn} is the operation voltage of the diode. The inset shows a schematic diagram of the measurement setup for the lateral 2D p–i–n junction.

By biasing the n- and p-channel devices above their threshold voltages, the electrical characteristics of the p–i–n device were then measured with the setup schematically shown in the inset of Fig. 4. The measurement was carried out at 1.5 K in a helium continuous-flow cryostat. The gate voltage of the p-channel device V_{gp} was set at -3 V and that of the n-channel device V_{gn} at $+5$ V. The current flow between the p-channel and the n-channel I_{pn} was measured as a function of the voltage applied between the p and n ohmic contacts V_{pn} . Note that the current I_{pn} in Fig. 4 was plotted both in the linear and logarithmic scales for clarity. One can see clearly the rectifying behavior with a turn-on voltage of 1.53 V. This is in agreement with the theoretical calculation of the built-in voltage $V_{bi} = 1.535$ V.¹⁶⁾ The turn-on voltage of the p–i–n diode, however, slightly depends on the gate voltage applied to the n-gate and the p-gate. From the band diagram [Fig. 1(c)] and the built-in voltage V_{bi} (shown above), we can see that the turn-on voltage is approximately at the band gap energy and depends on the carrier densities in 2DEG and 2DHG. The higher the gate bias (positive for the n gate and negative for the p gate) is, the higher the built-in potential is and, therefore, the higher the turn-on voltage is. The current of the diode can go up to hundreds of μ A. In the reverse bias, the leakage current is below 1 nA up to -2 V.

The electroluminescence (EL) emission of the p–i–n diode measured at 1.5 K is shown in Fig. 5. The device was measured under gate voltages of $V_{gn} = 7$ V and $V_{gp} = -7$ V, and a forward current $I_{pn} = 200$ μ A. There are two peaks in the EL spectra. The peak at 1.529 eV (811 nm) with the full-width at half-maximum of 4.4 meV is, we believe, from the ground state emission of the 20 nm GaAs/AlGaAs quantum well. The results are in good agreement with the theoretical calculation. Using the infinite-well approximation, the ground state of electrons in the quantum well $E_{1n} = 0.014$ eV and the ground state of holes in the quantum well $E_{1p} = 0.002$ eV. Otherwise, the band gap energy of GaAs at 1.5 K is 1.517 eV. Therefore, the energy of ground state excitons of the quantum well can be estimated to be

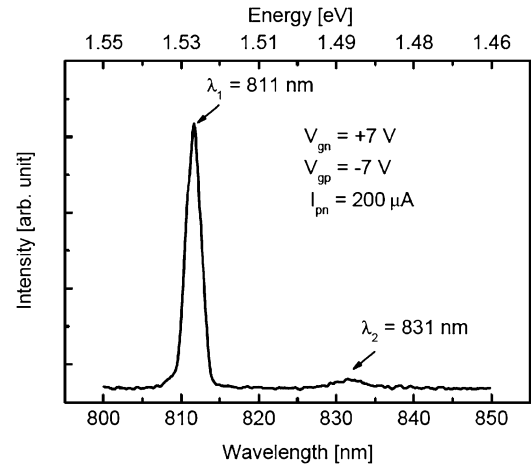


Fig. 5. Electroluminescence spectra of the lateral 2D p–i–n diode at temperature of 1.5 K with p–gate and n–gate biasing at $V_{gp} = -7$ V and $V_{gn} = +7$ V, respectively, and a forward current $I_{pn} = 200$ μ A.

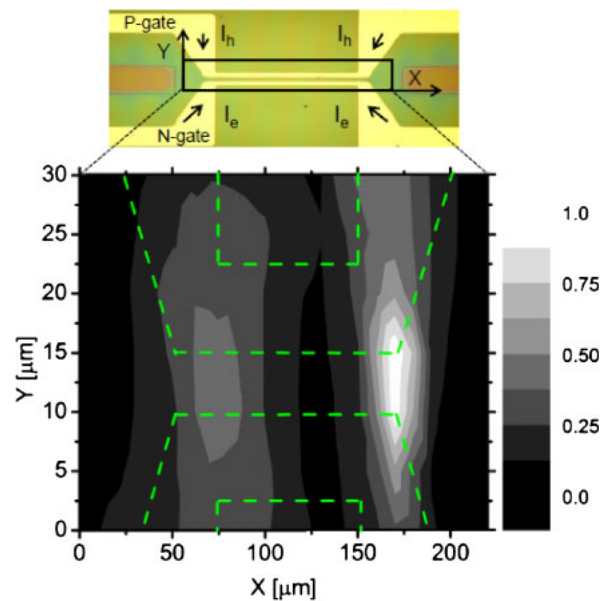


Fig. 6. (Color online) Contour plot of integrated spectrum intensity. Temperature $T = 77$ K, gate bias $V_{gp} = -5$ V, $V_{gn} = +5$ V, and forward current $I_{pn} = 100$ μ A.

approximately 1.533 eV (809 nm). The small peak at 831 nm is probably from the acceptor level in the quantum well. The positions of the peaks are independent of the diode current. The electroluminescence emission spectra of our devices are stable and much cleaner than those of previously reported lateral 2D junctions,^{2,8,10,14)} which is important for using the device for further studies and applications.

Furthermore, to confirm that the light was indeed emitted from the 2D p–i–n junction, EL intensities were measured as a function of position with a spatial resolution of 10 μ m. The device was inserted into the micro-photoluminescence (μ -PL) system. The stage can be controlled by using a Newport Universal Motion Controller ESP 300 with a step resolution of 0.5 μ m. Thus, a spectrum of the diode is captured by Princeton camera ST-133 for each position of the device. Figure 6 shows the contour plot of the integrated spectral intensity versus position. The scanned area is

$225 \times 30 \mu\text{m}^2$. The device was measured with $I_{\text{pn}} = 100 \mu\text{A}$, $V_{\text{gp}} = -5 \text{V}$, and $V_{\text{gn}} = +5 \text{V}$ at 77 K. From the result, one can clearly see that the emitted light is indeed from the junction area (in the middle between the dashed guide lines), but close to the two sides of the device. The reason for such distribution is because the lowest resistive path is near the two sides. Additionally, the emitted light coming from the right corner is much stronger than that coming from the left corner. This is possibly attributed to the asymmetric gate geometry [see Fig. 1(b)] and the resistance difference of the ohmic contacts.

4. Conclusion

In conclusion, we have developed a relatively simple method to fabricate high-quality lateral 2D p-i-n junctions. By using the MIS structure, 2DEG and 2DHG can be induced side by side in a completely undoped GaAs/AlGaAs quantum well. The electrical and optical properties of the device have been investigated. Our results show that the device is promising for applications in SAW-driven single-photon sources and probing the intrinsic spin Hall effect in low-dimensional systems by optical means.

Acknowledgements

We would like to thank the Center of Nano Science and Technology at National Chiao Tung University for the use of their equipment. This work was financially supported by the National Science Council and Ministry of Education of Taiwan.

- 1) C. L. Foden, V. I. Talyanskii, G. J. Milburn, M. L. Leadbeater, and M. Pepper: *Phys. Rev. A* **62** (2000) 011803.
- 2) J. R. Gell, P. Atkinson, S. P. Bremner, F. Sfigakis, M. Kataoka, D. Anderson, G. A. C. Jones, C. H. W. Barnes, D. A. Ritchie, M. B. Ward, C. E. Norman, and A. J. Shields: *Appl. Phys. Lett.* **89** (2006) 243505.
- 3) G. De Simoni, V. Piazza, L. Sorba, G. Biasiol, and F. Beltram: *Appl. Phys. Lett.* **94** (2009) 121103.
- 4) N. Tsutsui, V. Ryzhii, I. Khmyrova, P. O. Vaccaro, H. Taniyama, and T. Aida: *IEEE J. Quantum Electron.* **37** (2001) 830.
- 5) V. Ryzhii, M. Ryzhii, V. Mitin, and T. Otsuji: *J. Appl. Phys.* **107** (2010) 054512.
- 6) B. Kaestner, D. A. Williams, and D. G. Hasko: *Microelectron. Eng.* **67–68** (2003) 797.
- 7) B. Kaestner, J. Wunderlich, J. Sinova, and T. Jungwirth: *Appl. Phys. Lett.* **88** (2006) 091106.
- 8) M. Cecchini, V. Piazza, F. Beltram, M. Lazzarino, M. B. Ward, A. J. Shields, H. E. Beere, and D. A. Ritchie: *Appl. Phys. Lett.* **82** (2003) 636.
- 9) G. De Simoni, L. Mahler, V. Piazza, A. Tredicucci, C. A. Nicoll, H. E. Beere, D. A. Ritchie, and F. Beltram: *Appl. Phys. Lett.* **99** (2011) 261110.
- 10) J. Wunderlich, B. Kaestner, J. Sinova, and T. Jungwirth: *Phys. Rev. Lett.* **94** (2005) 047204.
- 11) J. M. Z. Ocampo, P. O. Vaccaro, S. Saravanan, K. Kubota, and T. Aida: *Appl. Phys. Lett.* **82** (2003) 2951.
- 12) A. North, J. Burroughes, T. Burke, A. Shields, C. E. Norman, and M. Pepper: *IEEE J. Quantum Electron.* **35** (1999) 352.
- 13) P. O. Vaccaro, H. Ohnishi, and K. Fujita: *Appl. Phys. Lett.* **72** (1998) 818.
- 14) T. Hosey, V. Talyanskii, S. Vijendran, G. A. C. Jones, M. B. Ward, D. C. Unitt, C. E. Norman, and A. J. Shields: *Appl. Phys. Lett.* **85** (2004) 491.
- 15) B. Kaestner, D. G. Hasko, and D. A. Williams: *Jpn. J. Appl. Phys.* **41** (2002) 2513.
- 16) A. S. Achayan, A. E. Yesayan, E. M. Kazaryan, and S. G. Petrosyan: *Semiconductors* **36** (2002) 903.
- 17) O. A. Tkachenko, V. A. Tkachenko, D. G. Baksheyev, K. S. Pyskin, R. H. Harrell, E. H. Linfield, D. A. Ritchie, and C. J. B. Ford: *J. Appl. Phys.* **89** (2001) 4993.
- 18) S. E. Laux, D. J. Frank, and F. Stern: *Surf. Sci.* **196** (1988) 101.