Transconductance Enhancement due to Back Bias for Submicron NMOSFET

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Abstract—For the first time, a new phenomenon of transconductance enhancement due to back bias found in submicron MOSFET's is reported. A two-dimensional numerical simulation has been performed to investigate the origin of this observation. The enhancement of the channel potential gradient is verified to be the main reason responsible for this anomalous transconductance enhancement effect. Moderate channel doping concentrations ($5 \times 10^{16} \sim 5 \times 10^{17}$ cm^{-3}), short channel lengths (submicron regime), and operation under small drain bias are three key conditions for the maximum transconductance enhancement due to the back bias to occur. A conventional linear I-V model, which employs an effective channel length defined by the source/drain metallurgical junctions and bias-independent source/drain extrinsic resistance is not able to predict *such characteristics*.

I. INTRODUCTION

THE mobility degradation of MOSFET's inversion carriers caused by vertical field induced surface scattering has been extensively studied [1]–[7]. The degradation of mobility on the microscopic scale will produce a degradation of the transconductance G_m on the macroscopic scale [8]. Furthermore, as the effective vertical field is proportional to the effective charge density contributed from the bulk depletion charge Q_B and surface inversion charge Q_{INV}, the increasing amount of Q_B generated by higher magnitude of reverse back bias, V_{BS}, will further aggravate the degradation of channel carrier mobility, and thus the maximum transconductance, $G_{m,max}$. However, most existing literature [1]–[8] focused on large devices in order to minimize the parasitic and two-dimensional effects. Therefore, the validity of the above statement is limited to the intrinsic-channel-region-dominating devices in which the depletion of bulk charge and the inversion

of surface carrier are dominantly controlled by the gate bias and back bias. In this paper, we will report an interesting $G_{m,max}$ enhancement effect due to back bias, which is observed in the submicron devices with moderate channel doping concentrations ($N_A = 5 \times 10^{16} \sim 5 \times 10^{17}$ cm^{-3}). The origin responsible for this phenomenon has been investigated by using a two-dimensional device simulator. In this approach, the physical mechanism is completely understood and can explain the experimental observation very well.

II. EXPERIMENTAL RESULTS

N-channel MOSFET's with the channel doping concentration ranging from 1×10^{16} to 2×10^{18} cm^{-3} were fabricated using submicron N^+ poly gate CMOS technology. The gate oxide thickness is 145 Å. The N^+ source/drain were formed by As^{75} implant (80 Kev, 5×10^{15} cm^{-2}) and followed by N_2 annealing (900°C, 30 min). The achieved source/drain junction depth is about 0.25 μm. The devices have the gate length drawn on the mask (L_M) varying from 0.5 μm to 100 μm. The transconductance (G_m) measured in the linear region ($V_{DS} = 0.1$ V) under various back biases ($V_{BS} = 0, -1.5, -3.0, -4.5$ V) are shown in Figs. 1(a) and (b) for long-channel ($L_M = 100$ μm) and short-channel ($L_M = 0.7$ μm) devices, respectively. It is obvious that $G_{m,max}$ of the long-channel device degrades with increasing reverse back bias, while that of the short-channel device shows an anomalous enhancement effect.

Channel doping concentration ($1 \times 10^{16} \sim 2 \times 10^{18}$ cm^{-3}) and channel length (0.5 $\sim$100 μm) are two key parameters, which determine G_m behavior under back bias. The variation amount of $G_{m,max}$ due to back bias is denoted as $\Delta G_{m,max}(V_{BS})$. The relative variation calculated by $\Delta G_{m,max}(V_{BS})/G_{m,max}(G_{m,max} = G_{m,max}(V_{BS} = 0))$ is used as the enhancement indicator. Fig. 2 summarizes $\Delta G_{m,max}(V_{BS})/G_{m,max}$ for various channel doping concentrations and channel lengths. For devices with moderate channel doping concentration ($N_A = 5 \times 10^{16} \sim 5 \times 10^{17}$ cm^{-3}), a pronounced $G_{m,max}$ enhancement due to reverse back bias is observed in the submicron channel regime. The maximum $\Delta G_{m,max}(V_{BS})/G_{m,max}$ occurs at $L_M = 0.8 \sim 0.5$ μm for $N_A = 5 \times 10^{16} \sim 5 \times 10^{17}$ cm^{-3}; that is, the critical channel length with a maximum $\Delta G_{m,max}(V_{BS})/G_{m,max}$ decreases with N_A increasing. As N_A is increased continuously to the order of 1×10^{18} cm^{-3}, $G_{m,max}$ enhancement due to reverse back bias is not found for the channel lengths investigated. In the other limiting

(a)

Fig. 2. Measured $G_{m.\max}$ variation, $\Delta G_{m.\max}/G_{m.\max}$ as a function of poly gate length $(L_M = 0.5{\sim}10~\mu\text{m})$ and channel doping concentration. N_A. $\Delta G_{m.\max}(V_{BS} = -3.0~\text{V}) = G_{m.\max}(V_{BS} = -3.0~\text{V}) - G_{m.\max}$ $(V_{BS} = 0)$. $N_A = 2 \times 10^{16}~\text{cm}^{-3}$ (—●—), $5 \times 10^{16}~\text{cm}^{-3}$ (—△—), 2×10^{17} cm^{-3} (—▲—), $5 \times 10^{17}\text{cm}^{-3}$ (—○—), $1 \times 10^{18}\text{cm}^{-3}$ (—■—).

The mechanism underlying this interesting phenomenon is investigated by using a two-dimensional device simulator and a quantitative model is proposed to explain our observation satisfyingly.

III. TWO-DIMENSIONAL NUMERICAL SIMULATION RESULTS AND DISCUSSION

G_m is a small signal parameter, which can be derived from the I-V equation. The result shows that G_m is determined by three key parameters: the effective channel mobility $(\mu_{\text{eff}}(V_{GS}, V_{BS}, N_{SUB}))$, the derivative of μ_{eff} with respect to the gate bias $(\partial\mu_{\text{eff}}/\partial V_{GS})$, and the channel potential gradient $(\partial\Phi_F(x)/\partial x$, Φ_F is the quasi-Fermi potential). In the weak inversion region $(V_{GS} < V_T)$, G_m increases exponentially with V_{GS} increasing. As the devices go into strong inversion region $(V_{GS} > V_T)$, G_m degradation will be initiated due to μ_{eff} degradation. Consequently, $G_{m.\max}$ is observed where $\partial\mu_{\text{eff}}/\partial V_{GS}$ is negligible, and a critical gate overdrive $(V_{GS} - V_T)$ is defined. At this critical bias point, the back bias effect on $G_{m.\max}$ is determined by the derivative of μ_{eff} and $\partial\Phi_F(x)/\partial x$ with respect to the back bias $(\partial\mu_{\text{eff}}/\partial V_{BS}$ and $\partial(\partial\Phi_F(x)/\partial x)/\partial V_{BS})$. For long-channel devices in linear operation condition. good linearity is maintained for $\Phi_F(x)$ under various back biases; that is, $\partial(\partial\Phi_F(x)/\partial x)/\partial V_{BS}$ is negligible. For this case, the back bias effect on $G_{m.\max}$ is simply determined by $\partial\mu_{\text{eff}}/\partial V_{BS}$, which is always negative; hence, $G_{m.\max}$ degradation due to back bias is generally observed. However, with the emergence of submicron devices, the source/drain extrinsic overlap length becomes comparable to the intrinsic channel length. As a result, the channel potential distribution

(b)
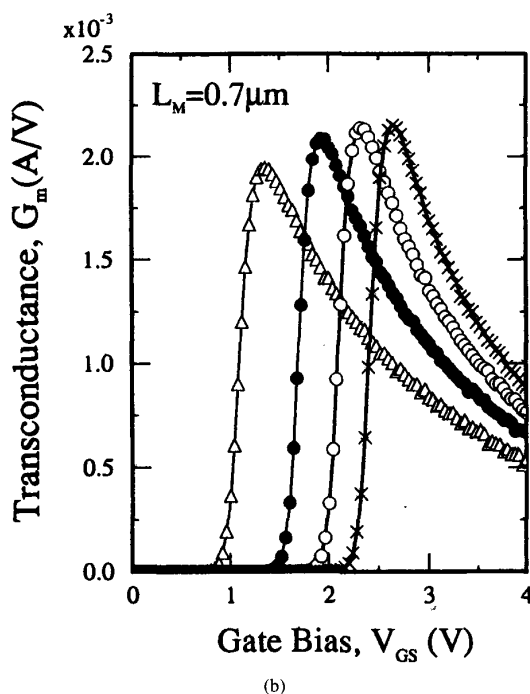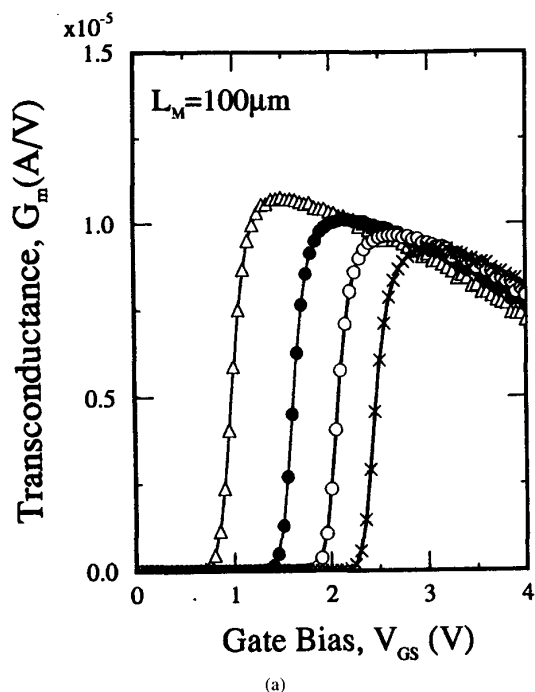
Fig. 1. Measured G_m vs. V_{GS} characteristics for (a) long channel NMOS($L_M = 100~\mu$m) and (b) short channel NMOS ($L_M = 0.7~\mu$m). Bias conditions are $V_{DS} = 0.1$ V with $V_{BS} = 0$(—△—), $V_{BS} = -1.5$ V (—●—), $V_{BS} = -3.0$ V (—○—) and $V_{BS} = -4.5$ V (—×—).

case, as N_A is decreased to 2×10^{16} cm^{-3} or below, $G_{m,\max}$ enhancement effect also disappears; and nearly zero $\Delta G_{m,\max}(V_{BS})$ is presented in the submicron regime.
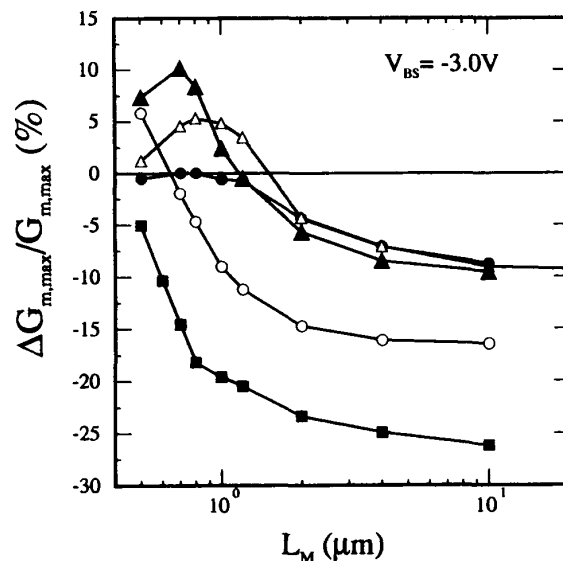
is a complicated two-dimensional problem, which will be aggravated by applying back biases. The extrinsic overlap region and the intrinsic channel region is clearly defined by using the decoupled C-V method proposed by Guo *et al.* [9]. In this approach, the two-dimensional charge sharing effect can be successfully separated from the intrinsic channel region. For this issue, a two-dimensional device simulator becomes indispensable in order to investigate the basic mechanism. In this work, PISCES-2B was used with the mobility model modified and calibrated based on the experimental data of long-channel devices over a wide range of channel dopant concentrations. This calibrated mobility model was also verified by the I-V characteristics of short-channel devices with a bias-independent contact resistance. Good agreement was achieved between the experimental and simulation results.

In the case of submicron devices with moderately doped channels ($N_A = 5 \times 10^{16} \sim 5 \times 10^{17}$ cm^{-3}), the back bias has a significant effect on the quasi-Fermi potential and electrostatic potential distribution along the channel surface, $\Phi_{FN}(x)$ and $\Psi_{SI}(x)$, respectively; that is, an one dimensional approach is not valid, and the channel potential is not determined simply by the source/drain terminal biases. Simulation was performed on a 0.65 μm device with N^+ source/drain structure and with $N_A = 2 \times 10^{17}$ cm^{-3}. The back bias effect on $\Phi_{FN}(x)$ is shown in Fig. 3(a) with varied back biases ($V_{BS} = 0$ and -3.0 V) and the gate biased around where $G_{m,\max}$ occurs ($V_{GS} = 1.25 \sim 1.35$ V for $V_{BS} = 0$ and $V_{GS} = 2.25 \sim 2.35$ V for $V_{BS} = -3.0$ V). The figures demonstrate very clearly that good linearity is achieved from the $\Phi_{FN}(x)$ curves with $V_{BS} = 0$. However, with $V_{BS} = -3.0$ V, the $\Phi_{FN}(x)$ are no longer linear across the whole channel of the submicron device, even under low drain voltage operation ($V_{DS} = 0.1$ V). The reason can be well interpreted by the more detailed simulation results illustrated in Figs. 3(b)–(e). Fig. 3(b) shows that, as the gate bias is fixed ($V_{GS} = 1.5$ V), Ψ_{SI} at source/drain terminals are pinned to the same value for $V_{BS} = 0$ and $V_{BS} = -3$ V, and then split away from the extrinsic overlap region into the central channel region. The Ψ_{SI} lowering due to back bias in the extrinsic overlap region is much smaller than that in the central (intrinsic) channel region; that is, because the channel dopant in the extrinsic overlap region is mostly depleted by the built-in barrier at the source/drain junctions, i.e., the back bias (body) effect is greatly relieved due to charge sharing effect. As a result, the threshold voltage for strong inversion is a decreasing function from the extrinsic overlap region to the intrinsic channel region. For the intrinsic channel region, the threshold voltage is defined as V_T (in this example, $V_T(V_{BS} = 0) = 1.0$ V, $V_T(V_{BS} = -3.0$ V) $= 2.0$ V), and $G_{m,\max}$ always occurs at a nearly constant ($V_{GS} - V_T$) even under varied back biases (in this example, $V_{GS} - V_T(V_{BS}) = 0.3$ V), i.e., the value of the gate bias associated with the $G_{m,\max}$ always shifts with nearly the same amount of V_T shift due to V_{BS}. In the extrinsic overlap region, the local threshold voltage (V_T') is smaller than V_T in the intrinsic channel region. Moreover, as mentioned previously, the threshold voltage shift due to back bias, (i.e., the body effect) in the extrinsic overlap region is greatly alleviated;
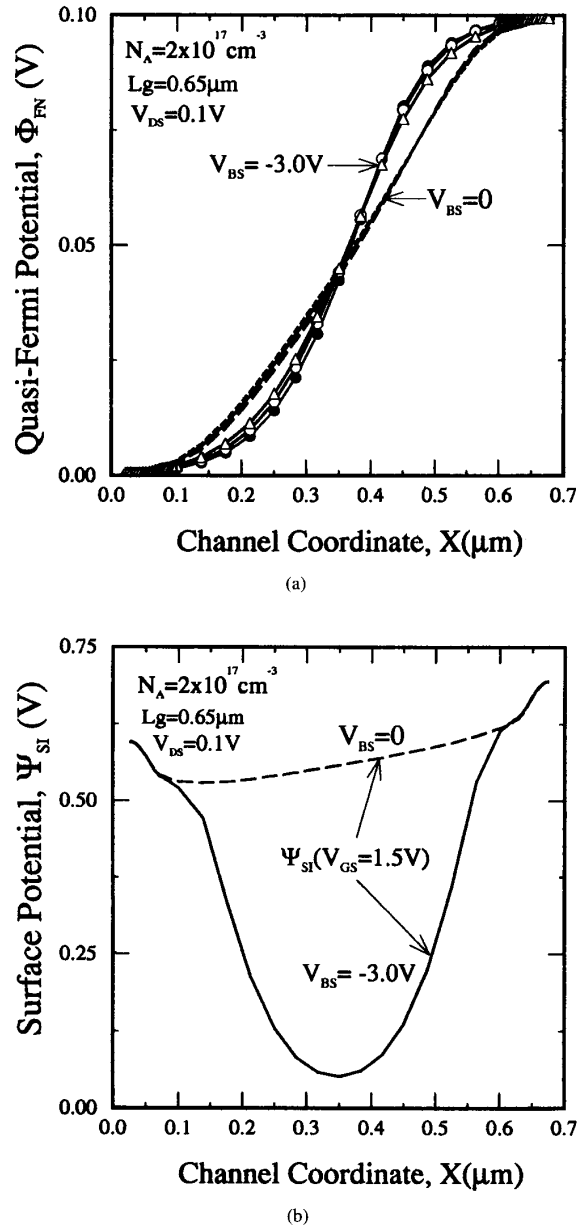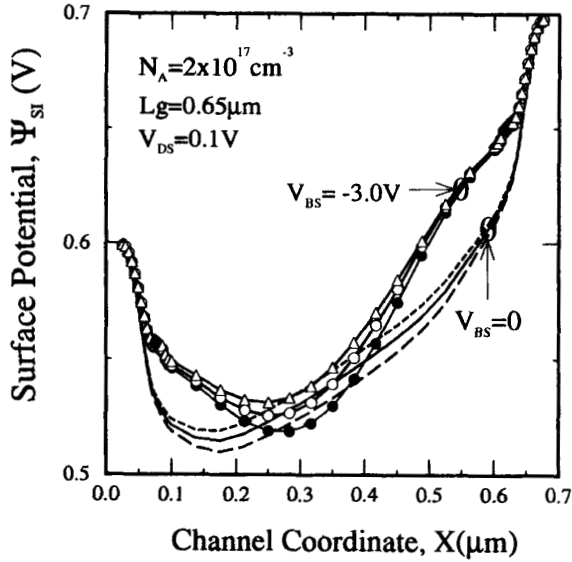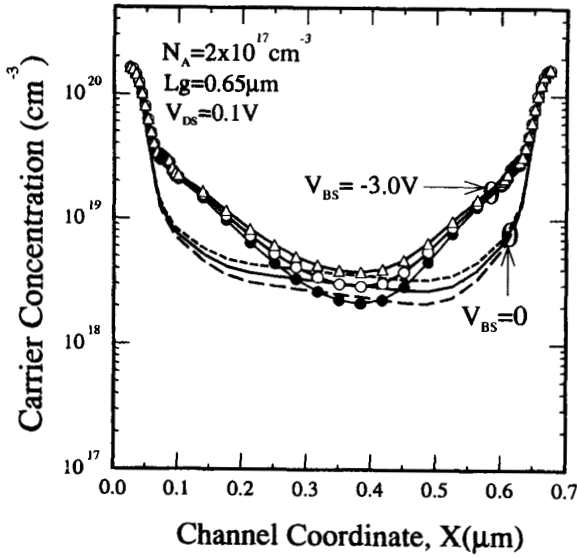

(a)

(b)

Fig. 3. Simulated results for short channel device ($L_M = 0.7$ μm, $L_g = 0.65\mu$m) with moderate channel doping concentration, $N_A = 2 \times 10^{17}$cm^{-3}, (a) quasi-Fermi potential distribution profile, $\Phi_{FN}(x)$ (b) surface potential distribution profile, $\Psi_{SI}(x)(V_{GS} = 1.5$ V, $V_{BS} = 0, -3.0$ V)

hence, the local gate overdrive ($V_{GS} - V_T'$) in the extrinsic overlap region is higher than ($V_{GS} - V_T$) in the intrinsic channel region. Ψ_{SI} in the extrinsic overlap region will then locally increase due to the enhanced gate overdrive, and this local increase of Ψ_{SI} induced by the reverse back bias is illustrated in Fig. 3(c). The inversion carrier concentration in the extrinsic overlap region is enhanced greatly due to the local increase of Ψ_{SI} as shown in Fig. 3(d). The enhanced

(c)

(e)

Fig. 3 (e) Quasi-Fermi potential gradient $\partial\Phi_{FN}/\partial x$ along channel surface.

(d)

Fig. 3. Simulated results for short channel device (L_M = 0.7μm, L_g =0.65μm) with moderate channel doping concentration, N_A = 2 × 10^{17}cm^{-3}, (c) surface potential distribution profile, $\Psi_{SI}(x)$ (d) inversion carrier concentration profile, $n(x)$, Bias conditions for (a) and (c)~(e) are: V_{BS} with V_{GS} =1.25 V (— — —), $V_{GS}(G_{m,max})$ =1.30 V (———), and V_{GS} =1.35 V (———), and V_{BS} = −3.0 V with V_{GS} =2.25 V (—●—), $V_{GS}(G_{m,max})$ =2.30 V (—○—), and V_{GS} =2.35 V (—△—).

inversion carrier concentration results in the reduced series resistance and the reduced voltage drop across the extrinsic overlap region as shown in Fig. 3(a). As the total voltage drop across the whole channel (composed of the intrinsic channel and extrinsic overlap regions) is fixed by the drain bias (V_{DS}), i.e., the difference of Φ_{FN} between source/drain terminals just equals V_{DS}, the decrease of voltage drop in
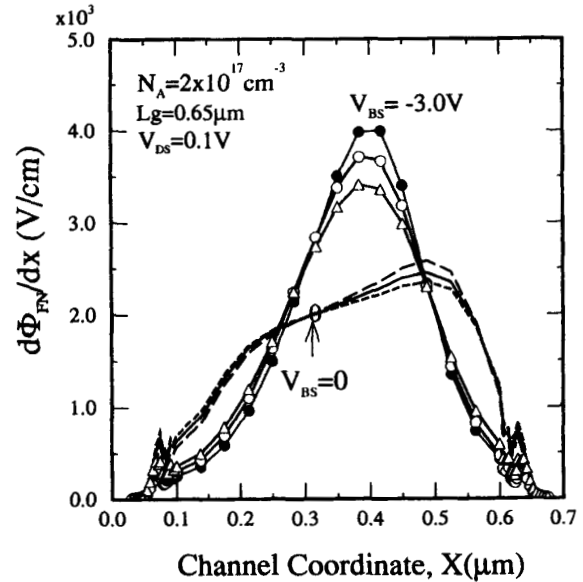
the extrinsic overlap region results in the increase of voltage drop and thus the increase of $\partial\Phi_{FN}(x)/\partial x$ across the intrinsic channel region as shown in Fig. 3(e). It is demonstrated that $\partial\Phi_{FN}(x)/\partial x$ under V_{DS} =0.1 V is only 2.0~2.5×10^3 V/cm at V_{BS} =0, but increases greatly to 4.0 × 10^3 V/cm at V_{BS} = −3.0 V. It means that under low drain voltage operation, the potential gradient enhancement in the intrinsic channel region due to back bias is pronounced and has significant contribution to the drift velocity and then the driving current and $G_{m,max}$.

In the case that N_A is reduced to 2 × 10^{16} cm^{-3} or below, $G_{m,max}$ enhancement due to back bias no longer exists even for submicron devices. Fig. 4(a) illustrates the channel potential profile simulated for 0.65 μm device with N_A scaling down to 1 × 10^{16} cm^{-3}. No significant difference is observed due to the back bias. The channel potential keeps good linearity for both V_{BS} =0 and V_{BS} = −3.0 V; consequently, for the potential gradient, negligible difference is presented due to back bias as shown in Fig. 4(b). The relieved back bias effect in the intrinsic channel region, (i.e., body effect) is the main reason for the disappearance of $G_{m,max}$ enhancement due to back bias. The charge sharing effect is aggravated in short channel devices with low channel doping concentration, then the V_T shift due to back bias is greatly reduced. The smaller shift of V_T in the intrinsic channel region also reduces the difference of V_T and V_T'. According to above discussion, the local increase of Ψ_{SI} is greatly reduced, and the quasi-Fermi potential profile within the intrinsic channel region is little changed. Thus, the increase of the potential gradient becomes much less significant. As the back bias effect on both mobility degradation and potential gradient enhancement is greatly relieved, $G_{m,max}$ keeps nearly constant with various back biases as shown in Fig. 2; that is, nearly zero $G_{m,max}(V_{BS})$ is presented in the submicron regime.
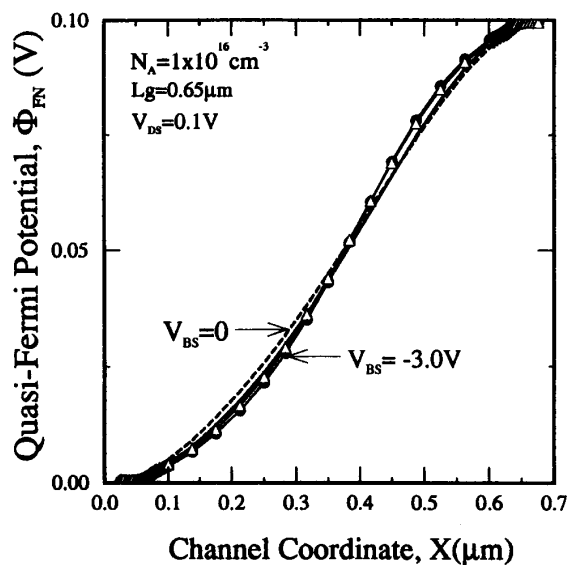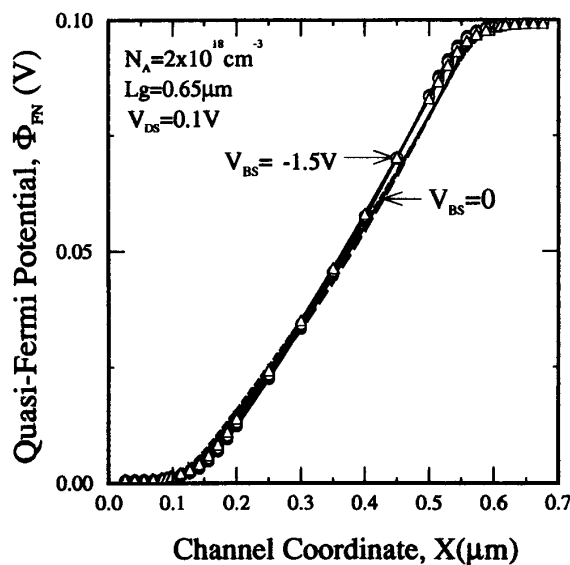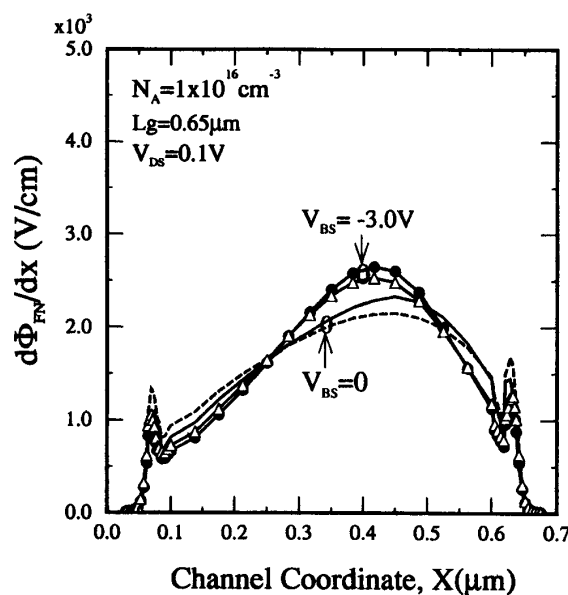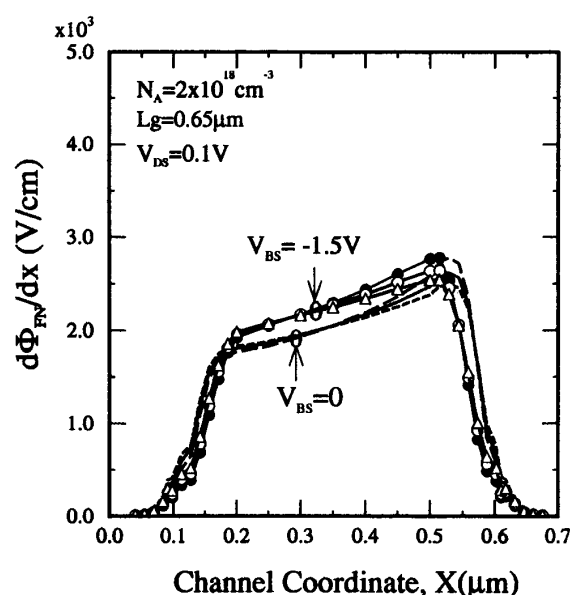
Fig. 4. Simulated results for short channel device (L_M =0.7 μm, L_g = 0.65 0.65μm) with lightly doped channel, N_A = 2 × 10^{16} cm^{-3} (a) quasi-Fermi potential distribution profile $\Phi_{FN}(x)$ (b) quasi-Fermi potential gradient $\partial\Phi_{FN}/\partial x$ along channel surface. Bias conditions are: V_{BS} = 0 with $V_{GS}(G_{m,max})$ =0.23 V (———) and V_{GS} =0.3 V(———); and V_{BS} = −3.0 V with $V_{GS}(G_{m,max})$ =0.37 V (—•—), and V_{GS} =0.4 V (—△—).

Fig. 5. Simulated results for short channel device (L_M =0.7 μm, L_g =0.65 μm) with heavily dopedchannel, N_A = 2×10^{18} cm^{-3} (a) quasi-Fermi potential distribution profile, $\Phi_{FN}(x)$ (b) quasi-Fermi potential gradient $\partial\Phi_{FN}/\partial x$ along channel surface. Bias conditions are: V_{BS} =0 with V_{GS} = 4.1 V (———), $V_{GS}(G_{m,max})$ =4.2 V (———), and V_{GS} =6.3 V (———); and V_{BS} = −1.5 V with V_{GS} =6.1 V (—•—),$V_{GS}(G_{m,max})$ =6.2 V (—◦—), and V_{GS} =6.3 V (—△—).

In the other limiting case, for the 0.65 μm devices with N_A increasing to the order of 2 × 10^{18} cm^{-3}, the channel potential and potential gradient from simulation are illustrated in Figs. 5(a) and (b), respectively. As the extrinsic overlap region shrinks with increasing N_A, the intrinsic channel region dominates even for the submicron devices, so that the

local increase of Ψ_{SI} and carrier concentration enhancement in this extrinsic overlap region makes little contribution to the channel potential distribution ($\Phi_{FN}(x)$) and its gradient ($\partial\Phi_{FN}/\partial x$). The enhancement of $\partial\Phi_{FN}/\partial x$ due to back biases becomes insignificant and not enough to compensate the

mobility degradation aggravated by back biases, so $G_{m,\max}$ degrades with increasing reverse back bias; that is, as the simple one-dimensional model has predicted (mentioned in Section III).

In summary, the channel doping concentration and physical channel length are two key parameters, which determines the electrical channel length. One-dimensional model is only applicable for electrically long devices in which the channel potential distribution is determined solely by the source/drain terminal biases. In the case of short channel devices, the channel doping concentration has critical effect on the extrinsic overlap length and intrinsic channel length; and also the back bias effect on the channel potential distribution. For devices with moderate channel doping concentration ($5 \times 10^{16} \sim 5 \times 10^{17}$ cm^{-3}), the back bias effect is significant in the intrinsic channel region but greatly alleviated in the extrinsic overlap region, so that the nonequality of gate overdrive between the extrinsic overlap and intrinsic channel regions is enhanced by the back bias. Transconductance enhancement will be achieved when the potential gradient enhancement dominates over the mobility degradation due to back bias. In experimental, $G_{m,\max}$ enhancement due to back bias is observed for both conventional and LDD submicron devices, if the channel doping concentration lies within the moderate domain ($5 \times 10^{16} \sim 5 \times 10^{17}$ cm^{-3}).

IV. CONCLUSION

For the first time, transconductance enhancement due to reverse back bias in submicron NMOSFET's with moderate channel doping concentrations ($N_A = 5 \times 10^{16} \sim 5 \times 10^{17}$ cm^{-3}) has been reported. Two-dimensional numerical simulation becomes indispensable to investigate the mechanism of this unexpected phenomenon, since the quasi-Fermi potential and surface potential distribution in the above devices become a two-dimensional problem, which is difficult to predict accurately by a simple one-dimensional approach. The back bias effect on transconductance is determined by the competition between the mobility degradation and the channel potential gradient enhancement. Since the inversion carrier mobility always degrades with increasing reverse back bias, the enhancement of maximum transconductance is ascribed to the increase of channel potential gradient. For long-channel devices dominated by the intrinsic channel region, the aggravated mobility degradation dominates, so that the maximum transconductance always degrades with increasing reverse back bias. On the other hand, for submicron devices with nonnegligible extrinsic overlap region, channel potential gradient enhancement becomes so significant that transconductance enhancement is observed. This anomalous back bias effect is important for accurate VLSI circuit modeling and design.

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