Characteristics of Self-Induced Lightly-Doped-Drain Polycrystalline Silicon Thin Film Transistors with Liquid-Phase Deposition SiO_2 as Gate-Insulator and Passivation-Layer

Ching-Fa Yeh, Tzung-Zu Yang, and Tai-Ju Chen

Abstract— **As the passivation layer on the top of undoped offset region for offset-gate structured poly-Si TFTs is exposed to hydrogen plasma, a lightly-doped-like drain region could be equivalently self-induced. The hydrogenated polycrystalline silicon thin-film transistor of this structure, named self-induced lightly-doped-drain (SI-LDD) poly-Si TFTs, was first developed with liquid-phase deposition oxide as both the gate insulator and the passivation layer. This paper describes the optimum hydrogenation condition, and the electrical characteristics for the novel SI-LDD poly-Si TFTs. The effects of DC electrical stress on SI-LDD poly-Si TFTs are also described. Finally a model is proposed to explain the degradation phenomena observed in our SI-LDD devices.**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (Poly-Si TFTs) have been actively investigated for a long time because of their potential use in applications such as three-dimensional integrated circuits and active-matrix liquid-crystal displays (AMLCDs). Because of their high field-effect mobility and reliability, poly-Si TFTs can be used in both the peripheral circuits and switching devices of AMLCDs. However, poly-Si TFTs have an anomalous OFF-state leakage current which increases with gate voltage (V_{GS}) and drain voltage (V_{DS}), and are unacceptable for switching device application. Holding signal levels needed for acceptable image quality requires lowering the OFF-state current below 0.1 pA per micrometer of channel width [1].

The anomalous leakage current (I_{OFF}) is generally attributed to field enhanced carrier emission via trap states near the drain junction. To decrease the electric field in the drain depletion region, an offset-gate structured TFT (Fig. 1(a)) in which a lightly-doped n^- region is introduced between the undoped channel and the n^+ region has been proposed [2]–[4]. In that case, the additionally required implantation for lightly-doped n^- region complicates processing and increases costs. Besides, another TFT structure called the field-induced-drain (FID) TFT has also been proposed to reduce the anomalous leakage current and achieve high ON/OFF current ratio [5]–[8]. However, this FID structure (Fig. 1(b)) requires use of an additional field-plate electrode. Furthermore, the performance of the FID device is very sensitive to the field-plate bias and interlayer material compositional characteristic.

Recently, Kanicki [9] proposed a novel TFT with an undoped offset structure for achieving high ON/OFF current ratio

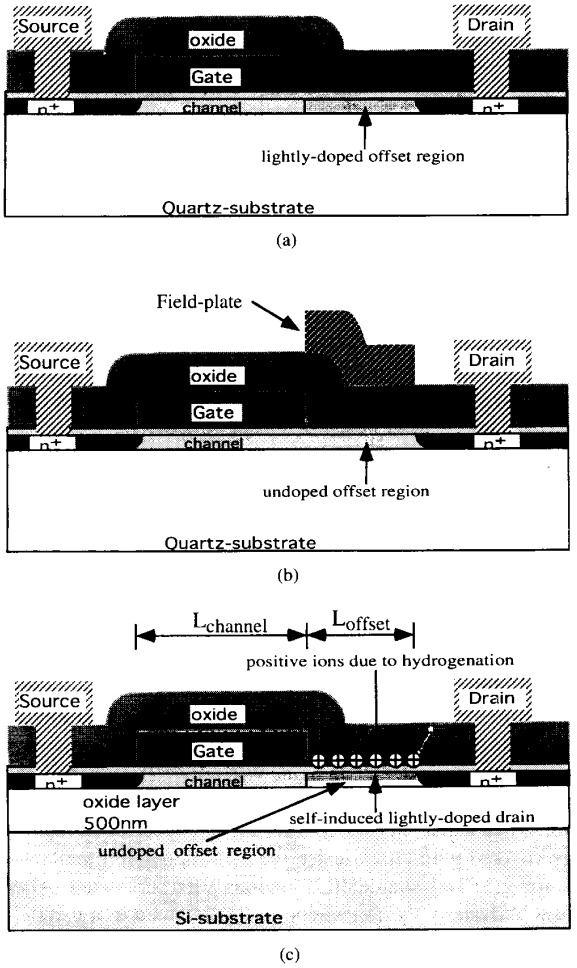

Fig. 1. (a) Offset-gate TFT structure; (b) field-induced-drain (FID) TFT structure; (c) self-induced lightly-doped-drain (SI-LDD) TFT structure.

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The authors are with the Department of Electronics Engineering & Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C.

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TABLE I
THE DEVICE CHARACTERISTIC PARAMETERS FOR THE SAMPLE GROUPS A, B, AND C. GROUPS A AND B: $L_{off} = 0\mu m$, GROUP C: $L_{off} = 0\mu m$

parameters / sample group	Hydrogenation time (hr)	Active poly-Si thickness (nm)	V_{th} (V)	S (V/dec)	μ_{FE} ($cm^2/V \cdot sec$)	N_t (cm^{-2})
A	0	100	12.9	2.11	17.9	7.25×10^{12}
B	3	100	6.91	1.28	25.5	4.20×10^{12}
C	3	30	3.37	0.425	22.4	3.00×10^{12}

(The maximum process temperature is 625°C)

independent of gate bias. With a dual passivation layer on top of the undoped offset region being exposed to hydrogen plasma, a lightly-doped-like region can be equivalently self-induced. The dual passivation layer was prepared by a series of processes including silicon dioxide (SiO_2) deposition by plasma enhanced chemical vapor deposition (PECVD), hydrogen plasma annealing and N-rich silicon nitride deposition by PECVD. These processes were very complicated, and the equipment was very expensive. In this study, we first developed an undoped poly-Si TFT structure with liquid-phase deposited (LPD) [10] oxide as a gate insulator and passivation layer. The apparatus used for LPD-oxide was very inexpensive, and the process easily performed at room-temperature. Because the hydrogenation treatment is an indispensable step in poly-Si TFTs processing, we called such devices "Self-Induced Lightly-Doped-Drain" (SI-LDD) poly-Si TFTs (Fig. 1(c)) [11], [12]. First, we will describe the investigation of the hydrogenation condition for the passivation layer, and then describe the electrical behavior of our SI-LDD poly-Si TFTs. The effects of DC electrical stress on the new devices will also be described. Finally, a model of SI-LDD and the migration of positive charges will be proposed to explain the results of this research.

II. DEVICE FABRICATION

The fundamental fabrication processes of SI-LDD TFTs are compatible with those of conventional TFTs. First, both the 30 nm and the 100 nm-thick active poly-Si layer prepared by solid-phase crystallization (SPC) method were patterned into islands, respectively. As both gate insulator and passivation layer, a 100 nm-thick silicon oxide was grown at 30°C by LPD method. The 400 nm-thick poly-Si layer was deposited and patterned as a gate electrode. After the undoped offset regions were covered with photo-resist, the self-aligned ion implantation for gate and source/drain regions was performed. After dopant activation, hydrogenation was performed in a parallel-plate plasma reactor at 300°C. The optimum hydrogenation time was determined. Finally, a 500 nm-thick interlayer oxide was formed by PECVD method. After metallization, sintering was performed at 400°C for 15 minutes. The maximum process temperature was 625°C. A schematic cross-sectional view of a finished SI-LDD poly-Si TFT is shown in Fig. 1(c). In this experiment, the channel length (L) is 20 μm, the channel width (W) is 100 μm, and the offset length (L_{off}) varies from 0 to 10 μm. Three groups of SI-LDD samples labeled A, B and C were prepared and are summarized in Table I.

To reduce the series resistance in the undoped offset region, the hydrogenation treatment must be optimized; that is, enough positive charges must be incorporated into the passivation layer to ensure that an adequate number of electrons will be induced in the surface layer of the offset region. Hydrogenation was performed in a atmosphere containing H_2 and N_2 gas mixture. As a parameter, the hydrogenation time was 1 hour, 2 hours, or 3 hours. To trace the effect of hydrogenation on incorporation of positive charges, the metal/oxide/single-crystal Si (MOS) capacitors with hydrogenated LPD-SiO_2 as insulator were also prepared.

III. RESULTS AND DISCUSSION

A. Hydrogenation Effect

First, the positive-charge incorporation in the passivation layer was investigated by means of flat-band voltage (V_{FB}) shifts of MOS capacitors exposed to hydrogen plasma. As shown in Fig. 2, the value of V_{FB} corresponding to C-V curves changed from -10.6 V to -20.2 V and to -24.2 V after 1 hr and 2 hrs of hydrogenation, respectively. These results show that positive charges indeed were incorporated in the passivation layer during hydrogenation. There is also evidence of positive charges incorporated in the passivation layer of SI-LDD poly-Si TFT: it became more conductive owing to electron accumulation on the surface layer of the undoped offset region. In other words, a lightly-doped-like region has been equivalently self-induced with the hydrogen plasma treatment. The quantity of positive charges is propositional to hydrogenation time. However, the V_{FB} changes indicated a saturation after 2 hrs. of hydrogenation. As shown in Fig. 3, there is also evidence of saturation on normalized ON current (I_{ON}) in SI-LDD poly-Si TFTs which can be attributed to positive-charge saturation in the passivation layer. Therefore, in this study, we considered 3 hours the optimum hydrogenation time.

B. Characteristics of Low-Temperature-Processed (LTP)SI-LDD Poly-Si TFTs

Next, we will discuss the characteristics of the LTP SI-LDD poly-Si TFTs with LPD-SiO_2 as gate insulator. Figure 4 shows the transfer characteristics (I_{DS}-V_{GS}) at V_{DS} =5 V for the group A samples (no hydrogenation) with L_{off} as a parameter. From the I_{DS}-V_{GS} of the conventional TFT (L_{off} =0 μm), the typical characteristic parameters including threshold voltage (V_{th}) of 12.9 V, subthreshold swing (S) of 2.11 V/dec,

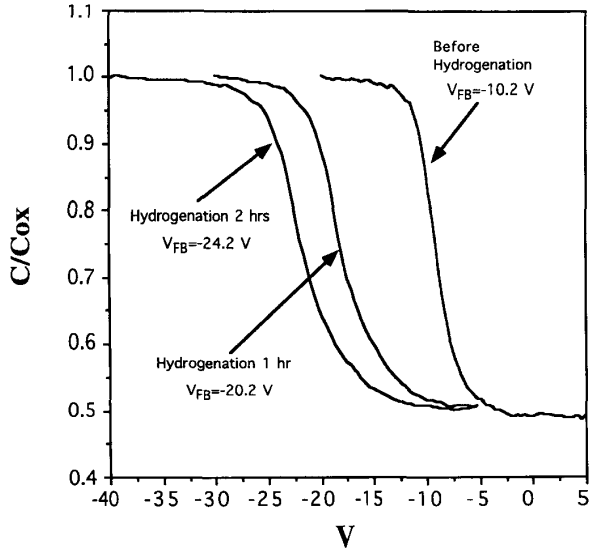


Fig. 2. High frequency (1 MHz) C-V characteristics and flat-band voltage (V_{FB}) of MOS capacitors before and after hydrogenation. The value of V_{FB} corresponding to C-V curves changed from -10.6 V to -20.2 V and to -24.2 Vafter 1 hr and 2 hrs of hydrogenation, respectively.

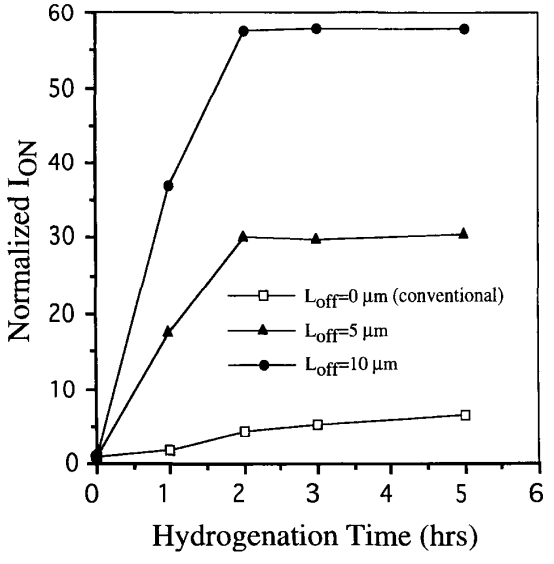


Fig. 3. Normalized ON current (I_{ON}) as a function of hydrogenation time for SI-LDD poly-Si TFTs with L_{off} =0 μm, 5 μm and 10 μm. Normalized I_{ON} saturated after 2 hrs of hydrogenation for TFTs with L_{off} =5 μm, and 10 μm.

mobility (μ_{FE}) of 17.9 cm^2/V·sec and trap-state density (N_t) of 7.25 $\times$ 10^{12} cm^{-2} were obtained and summarized in Table I. V_{th} is defined as the gate voltage which yields a normalized drain current of 0.1 μA·W/L measured at V_{DS} =5 V [13]. N_t existed in the poly-Si channel is calculated by extracting a straight line on the plot of In (I_{DS}/V_{GS}) versus $1/V_{GS}^2$ at low V_{DS} and high V_{GS} [14]. Since the group A were as-fabricated samples, no self-induced lightly-doped drain existed; ON-state performance was very poor and severely limited by the series

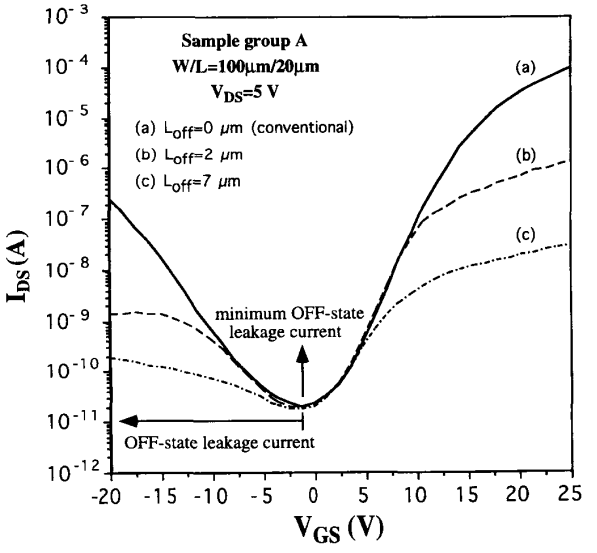
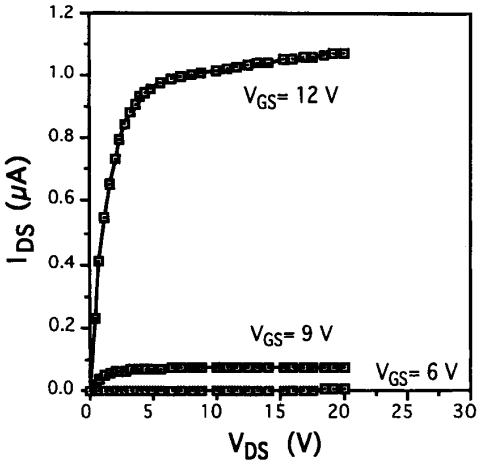


Fig. 4. A typical I_{DS}-V_{GS} characteristics at V_{DS} =5 V for sample group A poly-Si TFTs with L_{off} as a parameter.

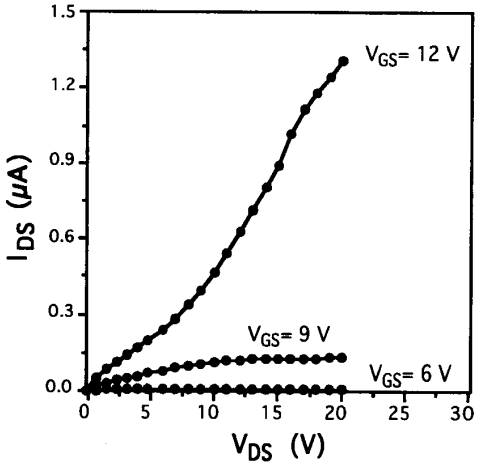
resistance in undoped offset region. On the other hand, for TFT with L_{off} = 2 μm or 7 μm, the OFF-state current increased with $|V_{GS}|$ in the range of -10 V < V_{GS} < 0 V. The behavior was similar to that in conventional poly-Si TFT. The OFF-state current in this gate bias range was dominated by the resistive leakage current [10], [15]. The increase of negative V_{GS} reduces the resistance of the channel region, as a result, the resistive leakage current increases.

Figures 5(a), (b) and (c) show typical output characteristics (I_{DS}-V_{DS}) for sample group A with L_{off} =0 μm, 2 μm and 7 μm, respectively. Except for conventional TFT (L_{off} =0 μm), both offset-gate structured TFTs showed triode-like characteristics in the low V_{DS} region. In other words, the TFTs without hydrogenation suffered from the so-called current-pinching phenomena in the low V_{DS} region. It is attributable to high series resistance in the undoped offset region.

However, a comparison of Fig. 6 (sample group B) with Fig. 4 shows 3 hours of hydrogenation time greatly improves transfer characteristics. When compared to the transfer characteristics of traditional TFT, significantly improved parameters including V_{th} of 6.91 V, S of 1.28 V/dec, μ_{FE} of 25.5 cm^2/V·sec and N_t of 4.2×10^{12} cm^{-2} were obtained; these are summarized in Table I. And, after 3 hrs. of hydrogenation the driving currents were increased over two orders of magnitude no matter whether the TFT was tested with L_{off} of 2 μm or 7 μm. Because a lightly-doped-drain had been induced and thus the conductivity was increased, these samples were therefore called SI-LDD TFTs. Moreover, in these SI-LDD TFTs, excellent turn-on characteristics without kink effect, as shown in Fig. 7(a), (b) and (c), were also achieved. The saturation current ($I_{DS,sat}$) only decreased a little even when the TFT was tested with L_{off} of 7 μm. And the saturation voltage ($V_{DS,sat}$) also increased with L_{off}. On the other hand, from a comparison of Fig. 4 and Fig. 6 we see that in our LTP SI-LDD poly-Si TFTs, the L_{off} of 2 μm was not long



(a)



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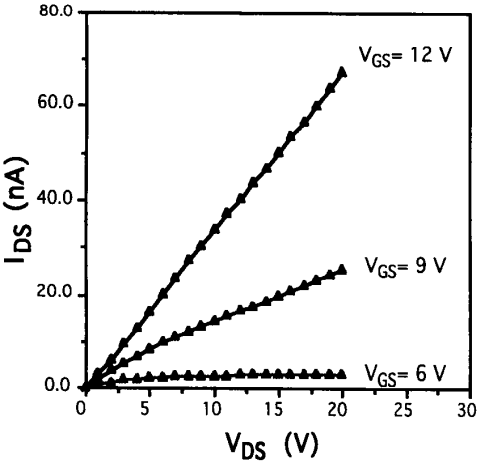

(c)

Fig. 5. A typical output characteristics (I_{DS}-V_{DS}) with V_{GS}as a parameter for sample group A. (a) L_{off} =0 μm (conventional), (b) L_{off} =2 μm, and (c) L_{off} =7 μm.

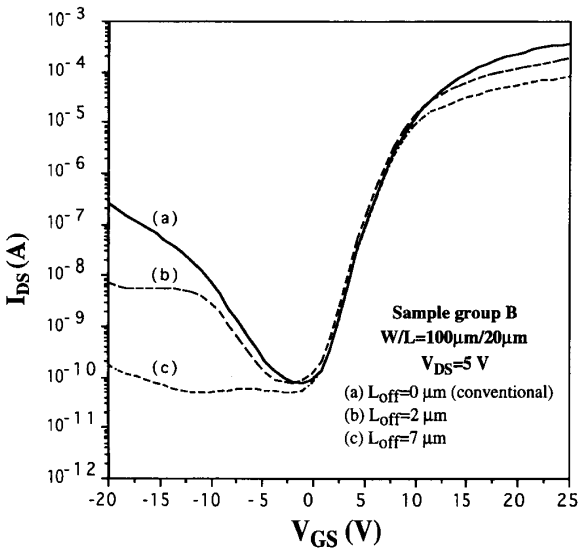

Fig. 6. A typical transfer characteristics (I_{DS}-V_{GS}) at V_{DS} =5 V for sample group B with L_{off} as a parameter.

enough to make OFF-state current independent of $|V_{GS}|$ for both sample groups A and B.

From Fig. 6, we see that the minimum OFF-state current of about 10^{-10} A is still too large to satisfy the specification of less than 0.1 pA per micrometer of channel width for switching-device application in AMLCD. To further improve ON/OFF electric characteristics, the effectness of thinning the active poly-Si films was also investigated for the SI-LDD TFTs. Fig. 8 shows a typical transfer characteristics of V_{DS} =5 V for the sample group C, in which the active poly-Si was 30 nm-thick. Compared with sample groups A and B, we found that the sample group C indeed had much-improved OFF-state characteristics. Especially, the minimum OFF-state drain current drops to about 2 pA. It shows that our SI-LDD TFTs with thinned poly-Si film achieves the specification of AMLCD. On the other hand, ON-state current of this sample group with L_{off} =7 μm was decreased about one order of magnitude compared with conventional TFT. Compromising OFF-state current with ON-state current, the offset length in 2~5 μm is therefore an optimum choice for SI-LDD poly-Si TFTs in sample group C. The characteristics parameters of LTP SI-LDD poly-Si TFT with 30 nm-thick active-layer and L_{off} =2 μm are summarized in Table I. The characteristics with V_{th} of 3.37 V, S of 425 mV/dec, μ_{FE} of 22.4 cm^2/V·sec, N_t of 3.0×10^{12} cm^{-2} and I_{ON}/I_{OFF} ratio of 2.08×10^7 at V_{DS} =5 V were obtained. All of the parameters exhibited eminently satisfactory performance. The excellent ON/OFF current ratio (>10^7), nearly independent of V_{DS} and V_{GS}, was achieved.

C. Reliability of SI-LDD Poly-Si TFT

The stability of the new SI-LDD poly-Si TFTs is of significant importance from the standpoints of fabrication technology and device structure. The long-term stability of the devices

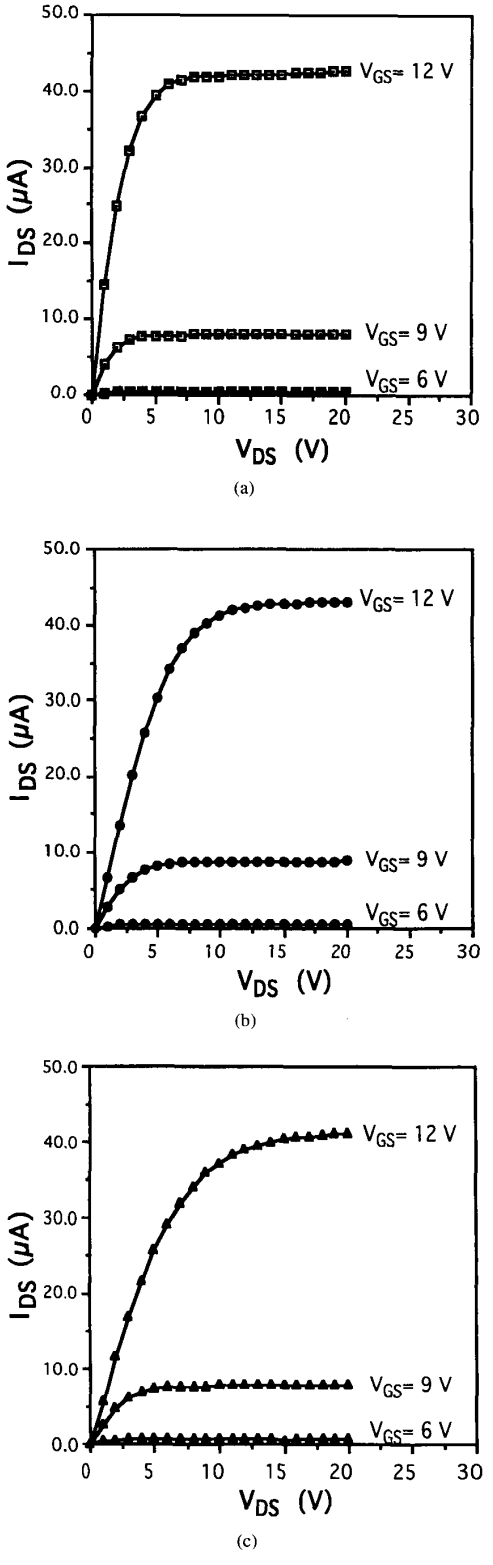

Fig. 7. A typical output characteristics (I_{DS}-V_{DS}) with V_{GS}as a parameter for sample group B. (a) L_{off} =0 μm (conventional), (b) L_{off} =2 μm, and (c) L_{off} =7 μm.

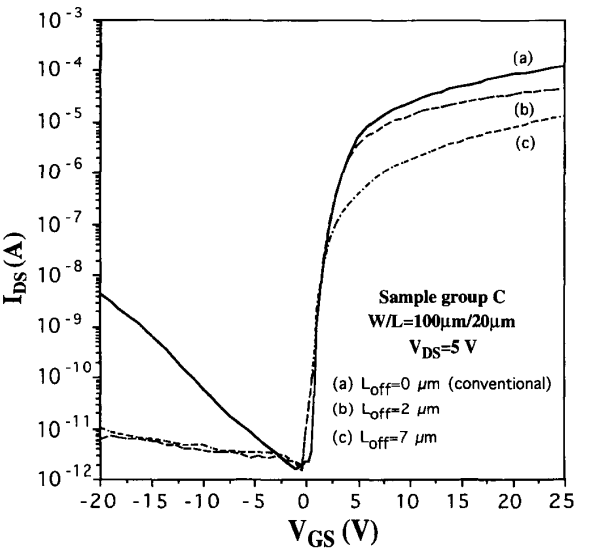

Fig. 8. A typical transfer characteristics (I_{DS}-V_{GS}) at V_{DS} =5 V for sample group C with L_{off} as a parameter.

after they were fabricated and stored for a long time was studied. We found no changes in the device performance even after two months of storage at room temperature. However, after DC electrical stress, the characteristics of the devices changed significantly.

Fig. 9 shows a typical change of I_{DS}-V_{GS} characteristics for the SI-LDD poly-Si TFT (sample group C) with L_{off} =2 μm under positive stress with V_{GS} =20 V and V_{DS} = 0 V for 1.23×10^5 s. It is seen that the characteristics curve after positive stress parallelly shifted to the left of the original curve. It is also found that the value of threshold voltage decreased from 3.59 V to 2.28 V, while the subthreshold swing was nearly unchanged. The degradation implied that there existes an instability factor that causes curve parallel shifting. The instability factor obviously can not be attributed to the generation of trapping states. In addition, the minimun of OFF-state current decreased from 7.0×10^{-12} A to 1.8×10^{-12} A, which was the level of the gate leakage current. The OFF-state current also increased with $|V_{GS}|$ and behaved like that in conventional TFTs without offset regions. The degradation phenomenon implied that the series resistance of the current path had increased. The result is consistent with the output characteristics after stress, which exhibited slight current-pinching phenomena in the linear region at low drain voltage. Figure 10 shows a typical change of I_{DS}-V_{GS} characteristics for the same devices (sample group C) after negative stress with V_{GS} = −20 V and V_{DS} =0 V for 2.72×10^5 s. We can see that device characteristics changed very much after negative stress in comparison with their before-stress values, and they changed differently than after positive stress. The I_{ON} after negative stress was significantly suppressed, it was suspected that the series resistance had increased. On the contrary, the OFF-state current (hole current) increased greatly in comparison with that before stress. The increase of minimum OFF-state leakage current was again attributed to the

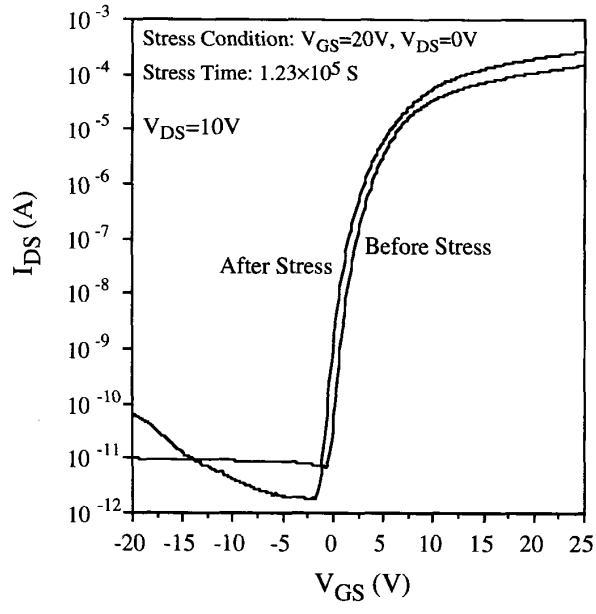

Fig. 9. A typical change of I_{DS}-V_{GS} characteristics for the SI-LDD poly-Si TFTs with L_{off} =2 μm (sample group C) under the stress with V_{GS} =20 V and V_{DS} = 0 V for 1.23 × 10^5 s.

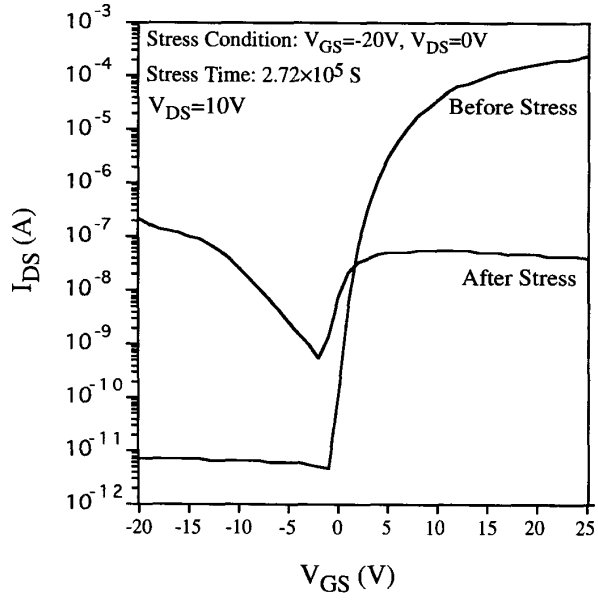

Fig. 10. The changes of I_{DS}-V_{GS} characteristics for the SI-LDD poly-Si TFTs with L_{off} = 22 μm (sample group C) under the stress with V_{GS} = −20 V and V_{DS} =0 V for 2.72 × 10^5 s.

series resistance of the current path, which must have locally decreased very much. The above results lead to suspicion that the positive charges in the gate oxide and the passivation layer above the offset region moved differently under both cases of high field stress. The details will be explained later.

To further clear the essential factor of device degradation, the bias-temperature (BT) test on the conventional poly-Si TFTs without offset region was also studied. The conventional device was also prepared with plasma-treated LPD-oxide as gate insulator. First, after the stress with V_{GS} =20 V at 150°C for 30 min, the transfer curve parallelly shifted to the left about 5 V. The subthrethold swing was nearly unchanged, Next, after the subsequent stress with V_{GS} = −20 V at 150°C for 30 min, the curve returned about 2.5 V, and the subthrethold swing increased. The value of threshold voltage also changed in response to the shift. The most possible mechanism that could change the performance of our SI-LDD TFTs under stress was the migration of positive charges in the oxide layer [16], [17]. We speculated that most of the positive charges were hydrogen atoms. During the hydrogenation treatment, there were positive charges incorporated in the passivation layer. Because the oxides regarded as paths for high diffusion of hydrogen [18], the hydrogen atoms could laterally diffuse into gate oxide. Therefore, many hydrogen atoms acumulated at the poly-Si/SiO_2 interface [19]. During stressing at V_{GS} = 20 V, the parallel shift toward the left for the transfer curve implied that the positive charges in the gate dielectric moved more near the poly-Si/SiO_2 interface. During subsequently stressing at V_{GS} = −20 V, the fact that the transfer curve returned toward the right suggested that the positive charges moved far away from the poly-Si/SiO_2 interface. In addition, some of the positive charges passivating the traps broke away from the defect sites caused by the high negative gate bias leading to the increase of the effective trap states density (N_t) [17], [20]. The tests implied that a possible migration phenomenon of positive charges in the plasma-treated LPD-oxide had occurred corresponding to the BT stress. In addition, because no changes in subthreshold swing were found in the BT tests, we could conclude that neither hot-carrier effect nor charge trapping in the gate dielectric [21–25] dominated the device degradation.

D. A Proposed Model

According to the above discussion, the most probable factor responsible for degradation in the performance of our SI-LDD TFT under stress was the migration of positive charges in the oxide layer. There have been many reports describing the unreliable positive charges existing in insulators [16], [17]. We proposed a model and illustrated the mechanism of SI-LDD and degradation in terms of positive charges migration. Figure 11(a) shows an original distribution of positive charges incorporated in both the gate oxide and the passivation layer above the offset region after hydrogen plasma treatment. Owing to the existance of positive charges in the passivation layer, beneath it a lightly doped N^- layer in the offset region was easily generated. Thus the TFT device with an equivalently lightly-doped offset region could effectively reduce the anomalous leakage current and achieve a high ON/OFF current ratio.

When a positive stress-bias was applied to the gate electrode, the high electric field under the gate electrode with the fringing fields at the edge of the gate electrode could make the positive charges migrate. The positive charges in the gate oxide under the gate electrode, as shown in Fig. 11(b), were

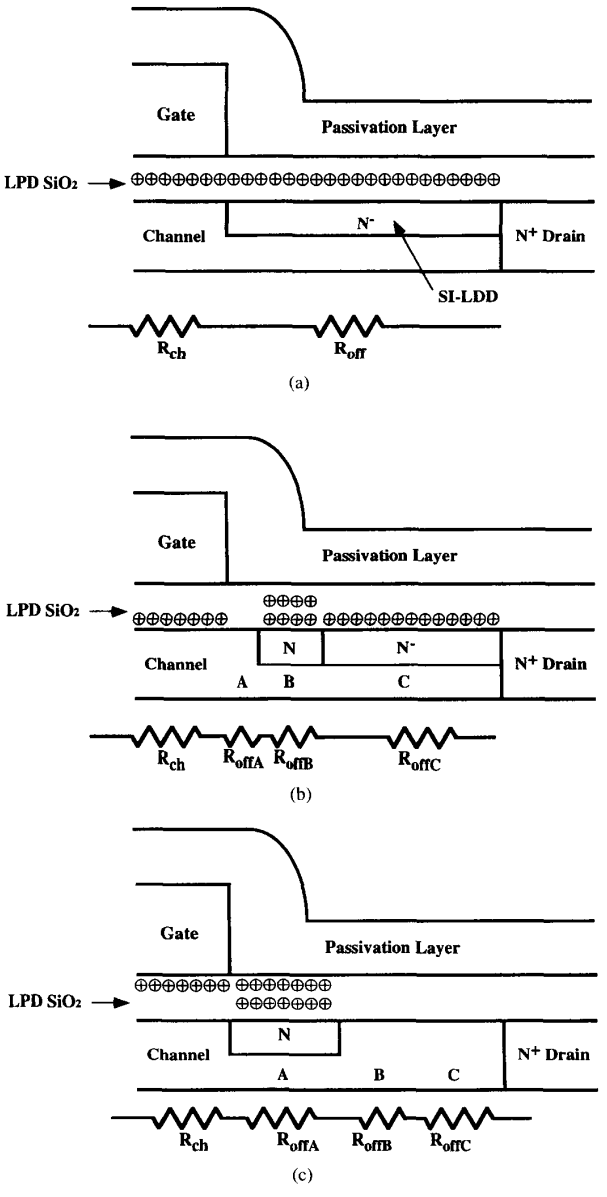

Fig. 11. A proposed model about the distributions of positive charges in the passivation layer above the offset region (a) before stress, (b) after V_{GS} =20 V stress, (c) after $V_{GS} = -20$ V stress.

forced closer to the Si/SiO_2 interface, therefore the transfer curve at ON state (as shown in Fig. 9) parallelly shifted a little. In addition, the fringing fields will be significant for only a small portion of L_{off}, a small portion of the positive charges in the passivation layer were also piled up a short distance away from the gate as shown in Fig. 11(b). It can thus be concluded that the positive charges above offset region A were depleted, while those were accumulated above offset region B. Above offset region C, the positive charges were only slightly affected. Therefore, the equivalent resistance ($R_{off\,A}$) at region A increased due to low electron induction; while the equivalent resistance ($R_{off\,B}$) at region B decreased due to higher electron induction. The increase in total offset resistance resultantly caused a reduction in the minimun OFF-state current (hole current) and a current-pinching phenomenon in the output characteristics. In addition, the lateral electric field along offset region B also changed with the redistribution of the positive charges. These changes thus caused an increase with $|V_{GS}|$ in OFF-state current [15]. Therefore the change of transfer curve at OFF state became much different from the simply parallel shift on the conventional device.

On the other hand, when a negative stress-bias was applied to the gate electrode, a high electric field made the distribution of positive charges under the gate electrode and above the offset region change as shown in Fig. 11(c). Owing to the negative electrical field, positive charges easily accumulated above the offset region A, while those were depleted above the offset region B and C. Thus, $R_{off\,A}$ easily decreased due to more electrons induced, while $R_{off\,B}$ and $R_{off\,C}$ increased greatly due to fewer electrons induced. Therefore, after negative stress the minimun of OFF-state current (hole current) increased with the reduction of total offset resistance. Because the redistribution of positive charges could affect the distribution of the lateral electric field along the offset region, the electric field near offset region A was enhanced. In addition, since these TFTs have been hydrogenated and hydrogen is only weakly bounded to the defect sites, we can see an increase in trap formation as the hydrogen breaks away from weakly passivated defect sites and migrates to the gate electrode. Thus the increase of OFF-state current with $|V_{GS}|$ was mainly due to the increase of effective trap state density and the lateral electric field along the offset region [15]. At the same time, the ON-state current was limited by the high series resistance in the offset region and effective trap state density.

The drain voltage could also play an important role in the degradation of SI-LDD poly-Si TFT. When the drain bias was applied during stress, the carrier-induced metastable midgap states were created within the poly-Si active layer due to the presence of high carrier densities in the channel [21], [23]. However, the enhancement of the high carrier densities on degradation would become dominant only in the case of long stress time.

IV. Conclusion

For reducing OFF-state current and achieving high ON/OFF current ratio, a novel and simple SI-LDD poly-Si TFT with LPD-oxide as both gate insulator and passivation layer has been newly developed using LTP technologies. The 3-hour hydrogenation treatment effectively incorporated positive charges in the passivation layer, and achieved significant improvements in device performance, for example, excellent turn-on characteristics without kink effect. The driving currents were increased over two orders of magnitude, while the OFF-state current become independent of $|V_{GS}|$ (if $L_{off} > 2$ μm). Besides, the SI-LDD poly-Si TFTs with 30 nm-thick active-layer and 2 μm of L_{off}, having an I_{ON}/I_{OFF} ratio of 2.08×10^7 at V_{DS} =5 V, a μ_{FE} of 22.4 cm^2/V·sec, a S of 425 mV/dec, a V_{th} of 3.37 V, and a N_t of 3.0×10^{12} cm^{-2} exhibited sufficient performance for pixel transistors of AMLCDs. This new SI-

LDD poly-Si TFT was rather stable during storage. However, degradation in electrical characteristics owing to migration of positive charges was found.

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Ching-Fa Yeh was born in Hsinchu, Taiwan, on September 20, 1948. He received the B.S. degree from National Oceanic University, Keelung, Taiwan, ROC, in 1971, the M.S. and Ph.D. degrees from the University of Tokyo, Tokyo, Japan, in 1979 and 1982, respectively, all in electrical engineering.

From 1982 to 1988, he was with the Fuji Xerox's Electronic Technology Laboratories, Ebina, where his work has been concerned with the research and development of semiconductor process technologies and devices, particularly on Dry Process technology and Contact Amorphous-Si Image Sensor, and High-Voltage MOSFET.

Currently, he is an Associated Professor at the Department of electronics Engineering & Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. His current research interests include thin-film transistor, power devices, silicon-wafer directly bonding technologies, and low-temperature processed materials and devices.

Dr. Yeh is a member of Japanese Journal Applied Physics Society, and he also as an oversea member of program committee of the international Conference on Solid State Devices and Materials.

Tzung-Zu Yang was born in Pingtung, Taiwan, on July 11, 1969. He received the B.S. and M.S. degrees in electronics engineering from National Chiao-Tung University in 1991 and 1993, respectively.

Currently, he is working with the Electronic Research and Service Organization, Industrial Technology Research Institute, Hsinchu, Taiwan, ROC, where he is engaged in the research of field emission display.

Tai-Ju Chen was born in Tainan, Taiwan, on September 13, 1970. He received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, ROC, in 1992. He is currently working towards the Ph.D. degree in electronics engineering at National Chiao-Tung University.

His current research interest is in the fabrication of polysilicon thin-film transistors.