Base Current Reversal Phenomenon in a CMOS Compatible High Gain n-p-n Gated Lateral Bipolar Transistor

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***Abstract*—Base current reversal phenomenon is newly observed in a CMOS compatible high gain n-p-n gated lateral bipolar transistor. We attribute this phenomenon to avalanche generation as verified experimentally and by two-dimensional device simulation. Detailed investigation reveals that: i) the multiplication ratio increases exponentially with the collector voltage or equivalently the peak field at the surface collector corner; and ii) the multiplication ratio is independent of not only the low level base-emitter forward biases applied but also the base width of the transistors fabricated by the same process. Design guideline for suppression of the base current reversal has been established such as to fully realize the potential of the gated lateral bipolar transistors, i.e., a very high current gain of 11,600 can be maintained as long as the power supply voltage is less than the critical value of 1.78 V. On the other hand, new application directly employing this phenomenon has been suggested. Comparisons between the base current reversal phenomenon in the gated lateral bipolar transistor and that in the vertical bipolar transistor have also been performed and significant differences between the two have been drawn and have been adequately explained.**

I. Introduction

In 1975, Hart and Barker [1] studied the hybrid-mode operation of a MOS transistor with source-substrate junction forward biased. Later in 1983, Vittoz [2] investigated the gated lateral bipolar transistor in a MOSFET structure, from which basic circuit blocks were realized with advantages of good matching and low $1/f$ noise. However, this type of bipolar transistors needed an extra bias applied at the gate and is indeed a four-terminal device. Recently, Vandebroek *et al.* [3]–[5] have published a series of the work on the three-terminal gated lateral bipolar transistors in the submicrometer MOSFET structures. Such gated lateral bipolar transistors have exhibited new features in terms of high current gain, high cut-off frequency, and improved low-temperature operation, and thus can further be utilized for cost effective mixed-mode BiCMOS applications [3]–[5]. High current gains measured are considerably due to three factors [3]–[5]: i) the short base width; ii) the SiO_2/Si interface of MOS quality; and iii) the gate-assisted barrier lowering, i.e., the surface emitter-base junction barrier height is lowered under gate modulation and thus most of the minority carriers injected from the emitter are limited to the surface depletion region while the base current is not affected. The channel implant energy and dosage are two important parameters to determine the degree of the gate-assisted barrier lowering [3]–[5]. Very recently, Huang and Chen [6] have reported a study of a CMOS compatible high-gain n-p-n gated lateral bipolar transistor along with experimental separation and modeling of different current components.

In this paper we will report an anomalous phenomenon newly observed in a high-gain n-p-n gated lateral bipolar transistor: the base current direction is reversed in the low level injection regime even at a small collector voltage, which is not reported in [3]–[6]. The mechanism responsible for this phenomenon, as identified experimentally and by two-dimensional device simulation, will also be reported. Important design considerations concerning the base current reversal will be presented such as to fully realize the potential of the gated lateral bipolar transistors. Note that the same phenomenon in a vertical n-p-n bipolar transistor has been originally observed by Sakui *et al.* [7] and Lu and Chen [8], and has been extensively studied by Lu and Chen [8] and Liu *et al.* [9]. However, our observed results are significantly different from those reported in [7]–[9], which will be addressed in this paper.

II. Experimental Observations

The devices under study as schematically shown in Fig. 1 were based on an n-channel LDD MOSFET structure fabricated using a 0.8 μm n^+ polycide-gate twin-well CMOS process. Boron (4.5×10^{12} cm^{-2}, 80 KeV) was implanted to form the p-well region. Boron (1.9×10^{12} cm^{-2}, 25 KeV) was applied for adjusting the threshold voltage to about 0.7 V. The gate oxide was grown in dry O_2 at 920°C to a thickness of 185 Å as determined by C-V method. After gate polysilicon deposition and phosphorus doping, a layer of WSi_2 (2500 Å) was deposited and annealed at 920°C to form the n^+ polycide gate. Phosphorus (2.0×10^{13} cm^{-2}, 60 KeV) was implanted to form the low-doped source/drain region. Arsenic (3.0×10^{15} cm^{-2}, 80 KeV) was implanted to form the highly-doped source/drain region. By using a spreading resistance probe, the junction depth and surface doping concentration of the p-well were about 3.0 μm and 6.0×10^{16} cm^{-3}, respectively; and the junction depth and surface doping concentration of the highly doped source/drain

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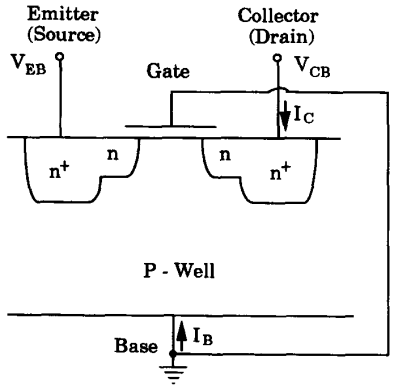


Fig. 1. The schematic cross section view of the test device in common-base configuration.

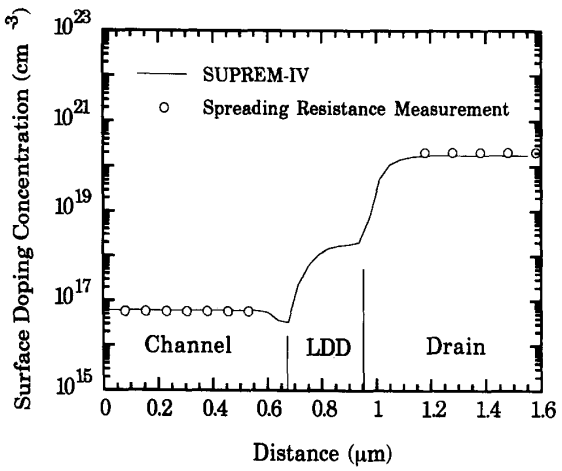


Fig. 2. The surface impurity concentration distribution from the mid-channel region to the drain created by SUPREM-IV. Also shown are the data from the spreading resistance measurement.

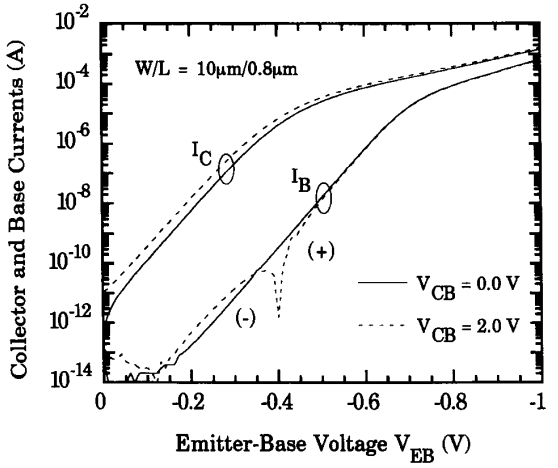
were about 0.25 μm and 2.0×10^{20} cm^{-3}, respectively. The n-channel LDD MOSFET structures with the gate width to length ratio (W/L) of 10 μm/0.8 μm, 100 μm/1.0 μm and 100 μm/1.5 μm were utilized. Fig. 2 depicts the surface impurity concentration distribution from the mid-channel region to the drain, obtained from two-dimensional process simulation program SUPREM-IV [10], in agreement with that based on spreading resistance measurement. As demonstrated in Fig. 1, the n-MOSFET structure can be employed as a gated lateral n-p-n bipolar transistor by transferring the role of source as emitter, drain as collector, and well as base. In our work the gate and well have been tied together.

The test devices mentioned above have been characterized in common-base configuration. Fig. 3 shows the Gummel I-V characteristics of the test devices with W/L =10 μm/0.8 μm and 100 μm/1.5 μm. From Fig. 3 it can be seen that at V_{CB} = 0 V we have ideal exponential I-V characteristics for $-V_{EB} \leq$0.45 V with peak current gains of about 11,600 for W/L = 10 μm/0.8 μm and 760 for W/L =100 μm/1.5 μm. These measured current gains have high values compatible with those in [3], [4]. Our high current gains obtained in the low level injection regime can be attributed to the gate-assisted barrier lowering, which enhances electron injection into the surface depletion region such that the surface electron diffusion current is by three to four orders of magnitude greater than not only the pure lateral bipolar collector current but also the base current [6]. Also note that the peak current gain increases with decreasing the base width, in agreement with that in [4]. Again from Fig. 3 we can observe that for the case of W/L =10 μm/0.8 μm at V_{CB} =2.0 V and W/L =100 μm/1.5 μm at V_{CB} =3.0 V, the base current direction is reversed over the low-level injection regime (i.e., $-V_{EB} \leq$ 0.4 V) and the dip where the base current drops to zero almost occurs at $V_{EB} \approx -0.4$ V. The effect of changing the collector voltage on the I-V characteristics for fixed emitter-base biases has also been measured. Fig. 4 shows such effect for W/L =10 μm/0.8 μm with low-level V_{EB} ranging from -0.2 V to -0.6 V. From Fig. 4 we can observe that the collector current increases slightly with increasing the collector voltage while the base current is considerably unchanged until the collector voltage approaches the critical point V_{cr} as labeled in the figure. As the collector voltage further goes across this point, the base current is reversed. The critical value, at which the base current drops to zero, is 1.78 V at $V_{EB} = -0.2$ V and is shifted up to 3.8 V for $V_{EB} = -0.6$ V, indicating that the critical collector voltage V_{cr} increases with increasing the injection level. The above new observations concerning the base current reversal phenomenon in the gated lateral bipolar transistors have not been reported in [3]–[6]. The same phenomenon has also been observed in the vertical n-p-n bipolar transistors [7]–[9]; however, our observation results are significantly different from those in [7]–[9], as will be demonstrated later.

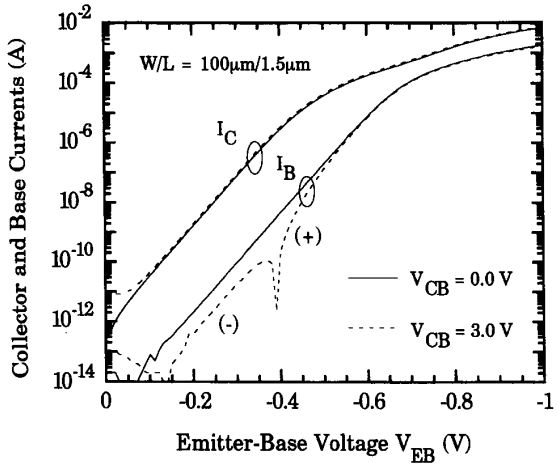
III. Detailed Investigation

A. Temperature Dependent Measurement

We attribute the above base current reversal phenomenon to the avalanche generation prevailing over the normal base current. This can be identified by the temperature-dependent measurement results as shown in Fig. 5, where the multiplication ratio ξ versus V_{CB} characteristics at a fixed injection level of $V_{EB} = -0.4$ V for two different temperatures of 25 and 85°C are depicted. The definition of the multiplication ratio ξ is given later. From Fig. 5 it is clearly seen that the multiplication ratio ξ exhibits a negative temperature coefficient for a given collector voltage, i.e., the ξ decreases with increasing the temperature, suggesting avalanche generation via impact ionization as the origin of the measured base current reversal. Therefore, we can conclude that under low level injection, the major part of the electrons injected from the emitter flows through the surface depletion region and arrives at the high-field collector corner where electron-hole pairs are generated via impact ionization. These electron-hole pairs created are separated by the electric field and the holes are swept into the quasi-neutral base region, contributing to an additional base current component with the direction opposite to the normal base current. Essentially, the amount of electron-hole pairs



(a)



(b)

Fig. 3. The Gummel plot of the n-p-n gated lateral bipolar transistor with (a) $W/L = 10$ μm/0.8 μm at V_{CB} =0.0 V and 2.0 V; and (b) W/L =100 μm/1.5 μm at V_{CB} =0.0 V and 3.0 V.

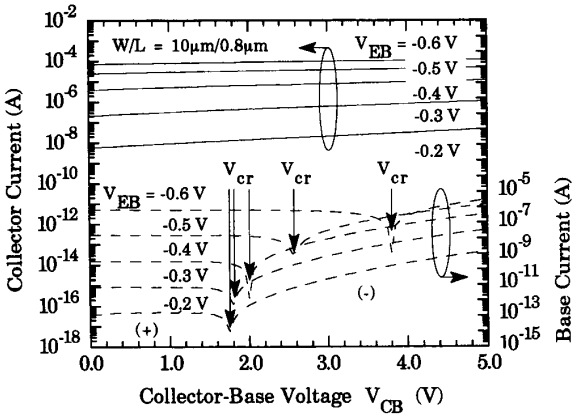


Fig. 4. The collector and base currents versus the collector voltage for five different values of V_{EB}. W/L =10 μm/0.8 μm.

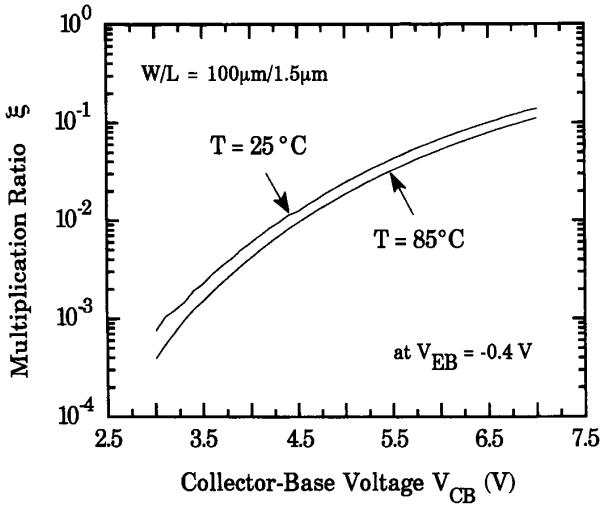


Fig. 5. The multiplication ratio versus the collector-base voltage for two different temperatures of 25°C and 85°C. W/L =100 μm/1.5 μm.

created depends on both the field strength and the injection current. It is worth noting that the device operating in the MOS mode exhibits breakdown voltage larger than 5 V due to the LDD type structure utilized while the avalanche-induced base current reversal is observed even at a low V_{CB} down to 1.8 V if the mode is transferred to the bipolar action.

B. Multiplication Ratio

According to the work of Lu and Chen [8], the base generation current $\Delta I_B(V_{CB})$ can be extracted from the terminal base current $I_B(V_{CB})$ by employing the expression $\Delta I_B(V_{CB}) = I_B(V_{CB} = 0\ V) - I_B(V_{CB})$. Based on this expression, the measured base current versus collector voltage curves in Fig. 4 for W/L =10 μm/0.8 μm at three different V_{EB} values of -0.2, -0.4 and -0.6 V have been separated into two distinct components: the base generation current and the base recombination current, as plotted in Fig. 6. The latter has been represented by $I_B(V_{CB}$ =0 V) since it is considerably independent of the collector voltage. Fig. 6 clearly reveals that for a fixed V_{BE} initially the base recombination current dominates; however, the generation current exponentially increases until a critical point is encountered where both components are identical but with opposite signs. Starting from this point, the dominant component of the terminal base current is due to avalanche generation. Also from Fig. 6 we can observe that for a fixed collector-base voltage the base generation current increases about exponentially with the forward bias V_{BE}, implying the contribution of the collector current which initiates impact ionization.

To normalize the contribution due to the collector current, the following expression for the multiplication ratio ξ has been applied [8]:

$$\xi = \frac{\Delta I_B(V_{CB})}{I_C(V_{CB}) - \Delta I_B(V_{CB})} \tag{1}$$

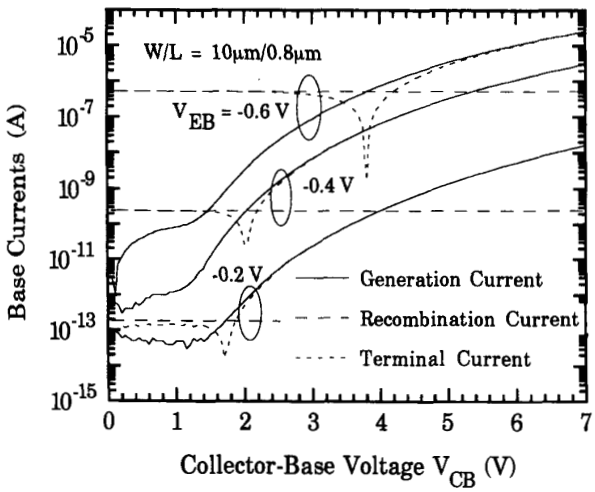


Fig. 6. The base generation current, base recombination current, and base terminal current versus the collector voltage corresponding to Fig. 4 for three different V_{EB} values of −0.2, −0.4, and −0.6 V.

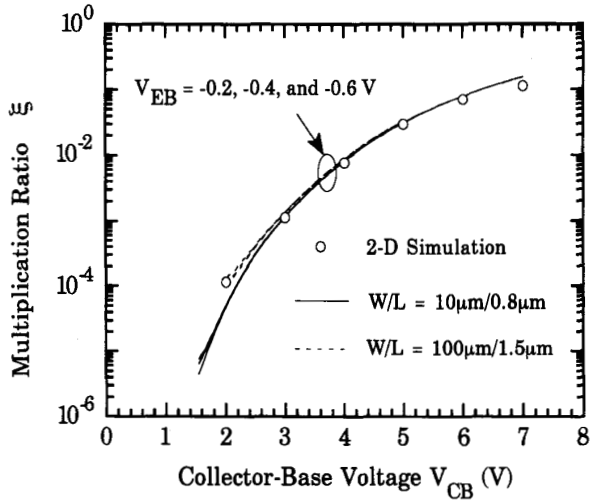


Fig. 7. The multiplication ratio versus the collector voltage from two different structures with V_{EB} as parameter. The two-dimensional simulation results are also marked.

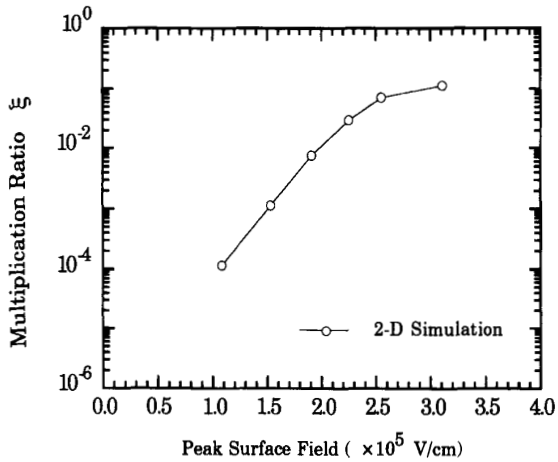


Fig. 8. The multiplication ratio versus the peak electric field extracted from the two-dimensional simulation results in Fig. 7.

By substituting the measured collector current in Fig. 4 and the separated base generation current in Fig. 6 both into (1), the multiplication ratio for W/L =10 μm/0.8 μm with three different V_{BE} values has been calculated with respect to the V_{CB}, as depicted in Fig. 7. The case of W/L =100 μm/1.5 μm is also plotted in Fig. 7. Fig. 7 clearly exhibits that i) the multiplication ratio increases exponentially as the V_{CB} increases from 1.5 V; and ii) the multiplication ratio is considerably a constant, independent of not only the base-emitter forward biases applied at low level injection but also the base width of the transistors fabricated by the same process. Apparently, the multiplication ratio depends on only the collector junction reverse bias or equivalently the surface field at the collector corner. This has further been proved by two-dimensional device simulation results as demonstrated in Figs. 7 and 8. Two-dimensional simulation has confirmed the calculated results as depicted in Fig. 7. Then from the simulated field distribution the peak field appearing at the surface collector corner has been extracted, leading to the establishment of Fig. 8. The detailed description of two-dimensional simulation utilized as well as its validity is given below.

C. Two-Dimensional Device Simulation

To further obtain an in-depth investigation on the base current reversal phenomenon in the gated lateral bipolar transistor, a two-dimensional device simulation program MEDICI [11] has been utilized. The surface impurity concentration distribution for the device under simulation is shown in Fig. 2. The important physical models, such as concentration- and field-dependent mobility, Shockley-Read-Hall recombination, Auger recombination, bandgap narrowing, impact ionization, etc., are considered. The avalanche generation rate G_{AV} modeled in MEDICI [11] is described by

$$G_{AV} = \alpha \cdot \frac{|\vec{J_n}|}{q} + \beta \cdot \frac{|\vec{J_p}|}{q} \tag{2}$$

where α and β are the impact ionization rates of electrons and holes, respectively; and $|\vec{J_n}|$ and $|\vec{J_p}|$ are the magnitudes of electron and hole current density, respectively. The impact ionization rates of electrons and holes can be expressed as [12]

$$\alpha = a_n \cdot \exp\left(-\frac{b_n}{|\vec{E_{J_n}}|}\right) \quad \text{and} \quad \beta = a_p \cdot \exp\left(-\frac{b_p}{|\vec{E_{J_p}}|}\right) \tag{3}$$

where $|\vec{E_{J_n}}|$ and $|\vec{E_{J_p}}|$ are the magnitudes of the local electric field strength along the direction of electron and hole current flowlines, respectively; a_n and a_p are the ionization coefficients of electrons and holes, respectively; and b_n and b_p are the critical fields of electrons and holes, respectively. After careful calibration to the experimental data, a series of I-V characteristics from the structure with W/L =100 μm/1.0 μm have been reasonably reproduced. The calibration

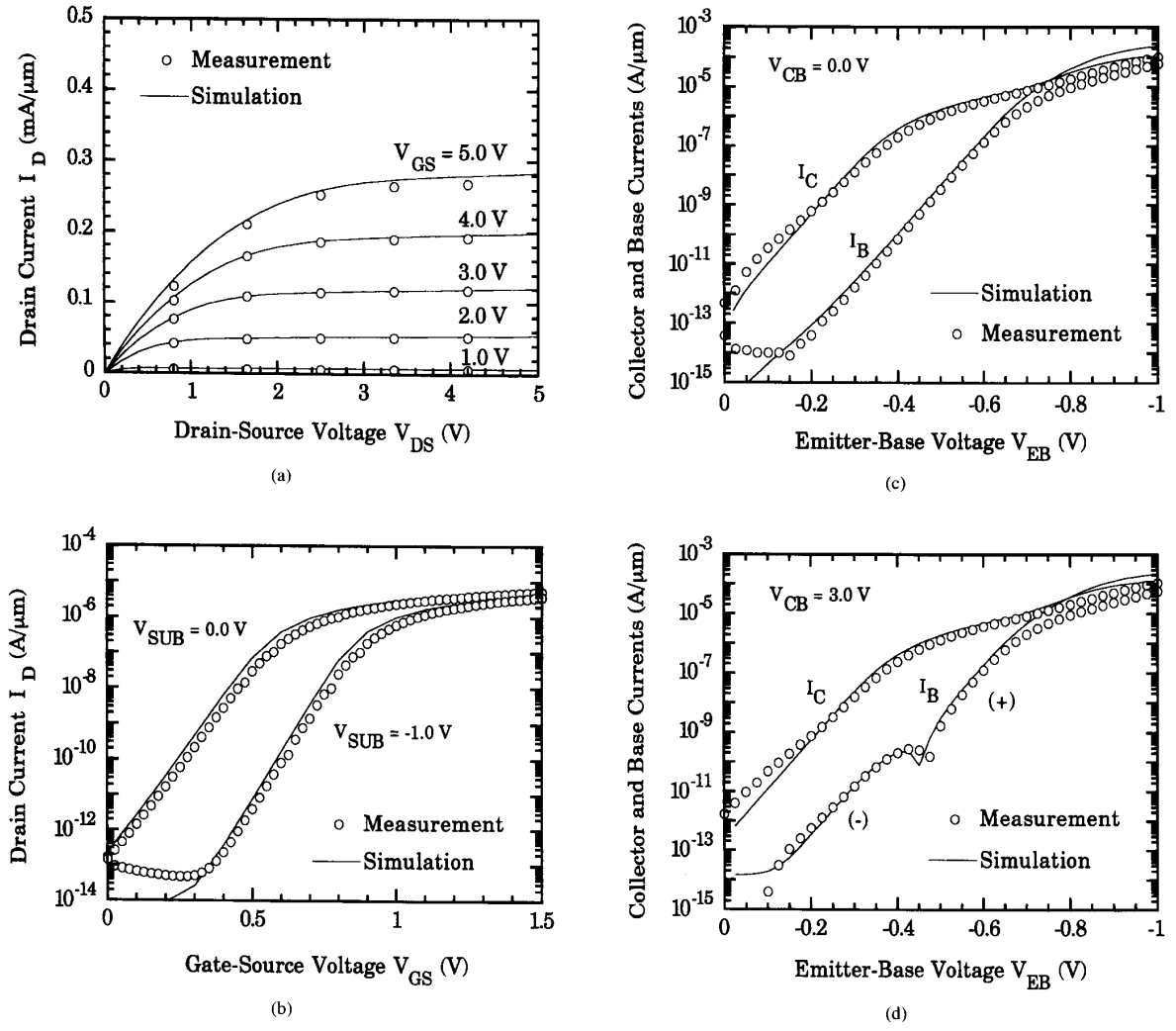


Fig. 9. The comparisons between the measured and simulated I-V characteristics of (a) the MOS output characteristics; (b) the MOS subthreshold I-V characteristics; (c) the Gummel plot at V_{CB} =0.0 V; and (d) the Gummel plot at V_{CB} =3.0 V. W/L =100 μm/1.0 μm.

results as compared with the measurement data are given in Figs. 9(a)–(d). From Figs. 9(a)–(d) we can observe that i) excellent agreements in both MOS and gated lateral bipolar I-V characteristics have been achieved; and ii) the base current reversal phenomenon has been successfully reproduced. The values of a_n and b_n after calibration are 7.73×10^5 cm^{-1} and 1.73×10^6 V/cm, respectively; and the values of a_p and b_p are 6.71×10^5 cm^{-1} and 1.69×10^6 V/cm, respectively. These values are reasonably close to the experimental data provided in [13].

Fig. 10 demonstrates the simulated electron current flow-lines and electric field contours inside the gated lateral bipolar transistor for two different V_{CB} values of 0 V and 3.0 V under the low-level injection condition as represented by $V_{EB} = -0.4$ V. Owing to the gate-assisted barrier lowering, most of the electron current flows along the surface depletion region, as clearly observed from Fig. 10. If the collector voltage is raised to 3.0 V, the collector junction electric field increases to above 1.0×10^5 V/cm and the impact ionization occurs remarkably. The vector plot of the hole current density is also depicted in Fig. 10. This vector plot yields the magnitude of the hole current density and its direction. It is clearly observed that at $V_{CB} = 0$ V the hole current flow is toward the emitter junction. At V_{CB} =3.0 V, however, a significant amount of electron-hole pairs is created at the collector junction corner and the holes are swept into the base contact. This causes the base current reversal as depicted in Fig. 9(d). Therefore, one can conclude that the base current reversal is due to avalanche generation at the high-field collector junction corner.

IV. Some Impacts

The base current reversal phenomenon has also been observed in the vertical n-p-n bipolar transistors [7]–[9]. However, there exist significant differences between our observation results and those in [7]–[9]. First, in the gated lateral BJT the base current reversal appears in the low level regime

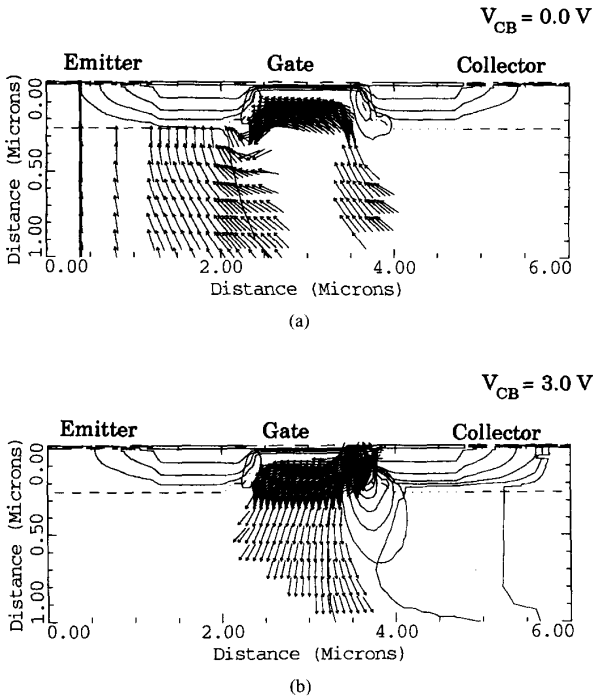


Fig. 10. The two-dimensional plot of the electron current flowlines, the electric field contours, and the hole current vectors in the gated lateral bipolar transistor under the low-level injection condition ($V_{EB} = -0.4$ V) for two different collector voltages of 0.0 V and 3.0 V.

of 0.15 V $< V_{BE} <$ 0.4 V as depicted in Fig. 3 while for the vertical BJT the same phenomenon occurs only for $V_{BE} >$ 0.4 V [7]–[8]. This difference is essentially due to the gate-assisted barrier lowering in the gated lateral BJT [3]–[5], which effectively increases the surface base-to-emitter forward bias. The other example is the different behavior of the multiplication ratio at high collector current as shown in Fig. 11. In this figure the multiplication ratio ξ versus the current I_C comes from the two gated lateral $n-p-n$ bipolar transistors and from a submicrometer vertical bipolar transistor as cited from [9]. From Fig. 11 we can observe that in the low-level injection regime of $I_C < 0.1$ mA, the multiplication ratio is considerably independent of the collector current for both the vertical and gated lateral BJT's. However, as we increase the collector current from 0.1 mA the multiplication ratio in the vertical BJT is decreased while in the gated lateral BJT the multiplication ratio is increased. This difference can be appropriately interpreted by the following reasons: i) in the vertical BJT the field redistribution occurs at the base-to-collector junction under the influence of base push-out (Kirk effect [14]), which reduces the field strength at high current [8], [9]; and ii) for the gated lateral BJT operated at high current, an inversion layer is formed near the emitter and the drift component dominates the collector current [6], which causes the pinch-off region narrowed with increasing the base-to-emitter forward bias and thus the surface field strength at the collector corner is increased.

The base current reversal phenomenon not only spoils the normal bipolar action but also may cause malfunction in the

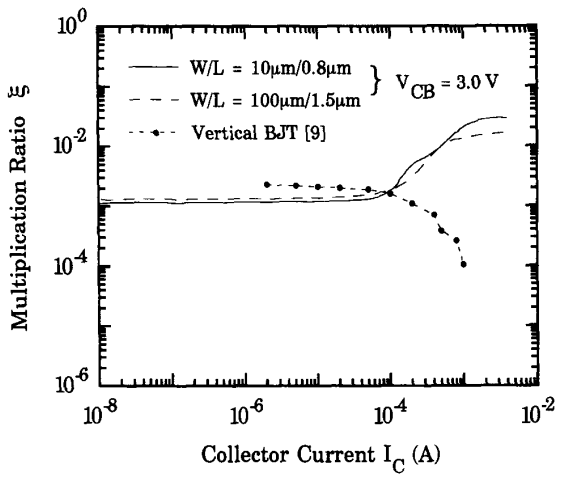


Fig. 11. The multiplication ratio of the two test devices as function of the collector current at $V_{CB} = 3.0$ V. Also depicted are the experimental data of the submicrometer vertical bipolar transistor cited from [9].

nearby circuitry. Therefore, design guideline for suppression of this phenomenon must be drawn such as to fully realize the potential of the gated lateral BJT. To achieve this purpose we employ the minimum critical collector voltage as measure of the immunity against the base current reversal. This can be clearly understood by observing the measured results in Fig. 4 for the case of W/L =10 μm/0.8 μm. From Fig. 4 it can be ensured that if the power supply voltage is less than the minimum critical collector voltage of 1.78 V, the base current reversal can be completely eliminated and a very high current gain of 11,600 can be maintained. For the case of W/L =100 μm/1.5 μm having peak current gain of 760, the minimum critical collector voltage is 2.95 V. Consequently, there exists a tradeoff between peak current gain and minimum critical collector voltage with respect to base current reversal. Note that the submicrometer vertical BJTs have exhibited the critical collector voltage less than 3 V [8], considerably close to that measured in our work.

On the other hand, the base current reversal phenomenon can directly be utilized to find new applications. One of such applications is the new static memory cell with two stable states ("0" for V_{BE} =0 V and "1" for V_{BE} =0.7 V) by employing the base current reversal in the vertical n-p-n BJT [7]. Following the work of Sakui, *et al.* [7], we propose a new static memory cell based on the same phenomenon in the gated lateral n-p-n BJT, i.e., the vertical n-p-n BJT in [7] is replaced by our gated lateral n-p-n BJT. Fig. 12 demonstrates schematically such proposal in terms of the cross section. The operation principle as described in detail in [7] can be applied accordingly. The our proposal is thus expected to work with two stable states of V_{BE} =0 V for low-level logic and V_{BE} =0.4 V for high-level logic.

V. Conclusion

The base current reversal phenomenon has been newly observed in a high-gain gated lateral n-p-n bipolar transistor

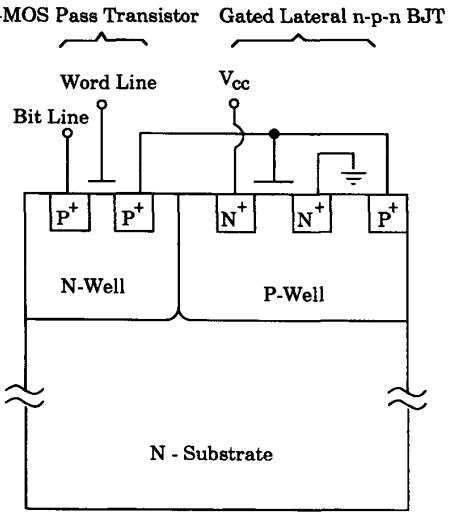


Fig. 12. Schematic cross section of the proposed new static memory cell employing the base current reversal phenomenon in the gated lateral n-p-n BJT.

based on an n-channel LDD MOSFET structure with the gate and well tied together. Temperature-dependent measurement attributes the observed base current reversal to avalanche generation and we can conclude that under low level injection, the gate-assisted barrier lowering makes most of electrons injected from the emitter to flow through the surface depletion region toward the high-field collector corner where electron-hole pairs are created via impact ionization. This has further been judged by two-dimensional device simulation. The dependencies of the multiplication ratio on the collector voltage, the peak field strength, the injection level, and the structure, have been extensively studied. Comparisons of the base current reversal phenomenon between the vertical and gated lateral BJT's have been performed and significant differences between the two have been drawn and have been adequately interpreted. To fully realize the potential of the gated lateral BJT, not only design guideline for suppression of the base current reversal has been established but also new application directly employing this phenomenon has been suggested.

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REFERENCES

[1] B. L. Hart and R. W. J. Barker, "First-order theory of MOSFET hybrid-mode operation," *Int. J. Electronics*, vol. 38, no. 5, pp. 625–630, 1975.
[2] E. A. Vittoz, "MOS transistor operated in the lateral bipolar mode and their application in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 18, pp. 273–279, 1983.
[3] S. Verdonckt-Vandebroek, S. S. Wong, and P. K. Ko, "High gain lateral bipolar transistors," *IEEE IEDM Tech. Dig.*, pp. 406–409, 1988.
[4] S. Verdonckt-Vandebroek, S. S. Wong, J. C. S. Woo, and P. K. Ko, "High-gain lateral bipolar action in a MOSFET structure," *IEEE Trans. Electron Devices*, vol. 38, pp. 2487–2496, 1991.
[5] S. Verdonckt-Vandebroek, J. You, J. C. S. Woo, and S. S. Wong, "High-gain lateral p-n-p bipolar action in a p-MOSFET structure," *IEEE Electron Device Letters*, vol. 13, pp. 312–313, 1992.
[6] T. H. Huang and M. J. Chen, "Empirical modeling for collector current of gated lateral bipolar transistors in an n-MOSFET structure," to appear in *Solid-State Electronics*.
[7] K. Sakui, T. Hasegawa, T. Fuse, S. Watanabe, K. Ohuchi, and F. Masuoka, "A new static memory cell based on reverse base current (RBC) effect of bipolar transistor," *IEEE IEDM Tech. Dig.*, pp. 44–47, 1988.
[8] P. F. Lu and T. C. Chen, "Collector-base junction avalanche effects in advanced double-poly self-aligned bipolar transistors," *IEEE Trans. Electron Devices*, vol. 36, pp. 1182–1188, 1989.
[9] T. M. Liu, T. Y. Chiu, V. D. Archer, III, and H. H. Kim, "Characteristics of impact-ionization current in the advanced self-aligned polysilicon-emitter bipolar transistor," *IEEE Trans. Electron Devices*, vol. 38, pp. 1845–1851, 1991.
[10] TMA TSUPREM-IV: Two-Dimensional Process Simulation Program, version 5, Technology Modeling Association, Inc., Nov. 1991.
[11] TMA MEDICI: Two-Dimensional Device Simulation Program, version 1.1, Technology Modeling Association, Inc., March 1993.
[12] A. G. Chynoweth, "Ionization rates for electrons and holes in silicon," *Phys. Rev.*, vol. 109, no. 5, pp. 1537–1540, 1958.
[13] R. Van Overstraeten and H. Deman, "Measurement of the ionization rates in diffused silicon p-n junction," *Solid-State Electronics*, vol. 13, pp. 583–608, 1970.
[14] C. T. Kirk, "A theory of transistor cutoff frequency (f_T) fall-off at high current density," *IEEE Trans. Electron Devices*, vol. 9, pp. 164–174, 1962.

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